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Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

Application Note

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1 Introduction

In today's highly competitive markets, efficient ESD protection has became an integral part of IC/ASIC design for system reliability. Field failures due to ESD will be perceived as poor quality by disappointed customers and will increase the number of warranty returns. Overlooking the ESD problem can seriously impact company's image and its profitability.

Reliable circuit protection following IEC61000-4-2 industry's standard is usually accomplished by the implementation of ESD protection devices at critical pins. However, some traditional approaches still rely on trial-and error practices to design for ESD protection. This can require several re-design loops until the ESD problem is finally solved, for instance during compliance testing, practice that increases costs and delay the time-to market of new electronic products.

The introduction of Very-Fast Transmission Line Pulse (vf-TLP) as support method is of utmost importance in the selection of appropriate ESD protection devices and makes the trial and error practices not longer justified. The Very Fast Transmission Line Pulse employs high current testing to determine the behaviour of devices and circuits in the current and time domain of ESD events. This strategy implemented at an early circuit design stage delivers a faster, precise and least costly approach to improve ESD robustness at system level while responding to today's market dynamics.

The purpose of this application note is to provide the guidelines for optimized selection of protection devices with the support of vf-TLP. Chapter 1 provides an introduction to electrostatic discharge standards typically used in the industry. Chapter 2 describes the characteristics of TLP equipment as well as measurement set up and testing capabilities. Section 2.6.2 explains the typical I/V characteristic curves of unidirectional and bidirectional protection devices. Chapter 3 displays a benchmark comparison of ESD protection devices based on different technologies, namely Multilayer Varistor (ceramic technology) and TVS diode (silicon based technology).

1.1 Definition of Electrostatic Discharge and Electrical Overstress

Electrostatic Discharge (ESD) is known as transfer of electrostatic charge between bodies or surfaces at different electrostatic potential. ESD can happen due to sudden discharge of a charged body, tribo-electric and induced charging. ESD is a high current event in the typical range of 0.1 to 30 A_{peak} in a very short period of time from 1 ns to 200 ns.

Electrical Overstress (EOS) is considered as the exposure of a device or an integrated circuit (IC) to a current or voltage beyond its absolute maximum ratings. EOS can occur due to voltage overshoots resulting in high destructive currents.

ESD is considered as a subset of EOS. But EOS may caused also by a wrong application of the IC beyond its absolute maximum voltage or current ratings. In this case the damage of the IC may not happened due to an ESD event.

The International Electrotechnical Commission (IEC) has developed transient immunity standards which have become minimum requirements for original equipment manufacturers. The basic standards for immunity testing are known as the IEC 61000-4-X standards. Three of the IEC standards deal with transient immunity:

- IEC 61000-4-2 : Electrostatic Discharge (ESD)
- IEC 61000-4-4 : Electrical Fast Transient/Burst (EFT)
- IEC 61000-4-5 : Surge Immunity

IEC 61000-4-2 is related to ESD immunity [1]. IEC 61000-4-4 and IEC 61000-4-5 are related to transient immunity [2, 3].

1.2 The IEC61000-4-2 ESD Standard

The IEC 61000-4-2 standard [1] addresses ESD transients in electronic systems. It defines immunity requirements for ESD which can be coupled into the equipment, systems or system boards directly or through radiation (air discharge). Direct coupling includes any user accessible entry points such as connectors, I/O ports, switches, computer keyboards, panel displays, touch screens and equipment housings.

Radiated coupling results from the spark discharge between two bodies which are external to the system. Because the human body is one of the most common ESD generators, the IEC standard defines a test set up which simulates an ESD event from a human body.
The Human Body Model is considered as a valid representation of worst case ESD stress. Discharge into equipment may be through direct contact (contact discharge method) or just prior to contact (air discharge method). Contact discharge is the usually preferred test method, but air discharge is used where contact discharge cannot be applied.

The ESD threat is divided into four threat levels depending on material and ambient humidity, as shown in Tab. 1. Threat level 1 is considered the least severe while threat level 4 is the most severe. Levels 1 & 2 are reserved for equipment which is installed in a controlled environment and in the presence of antistatic materials. Level 3 is used for equipment which is sparsely but not continuously handled. Level 4 is required for any equipment which is continuously handled.

Class	Relative Humidity (as low as)	Antistatic Material	Synthetic Material	Maximum Charge Voltage	Test Voltage (Contact-Discharge)	Test Voltage (Air-Discharge)
1	35 %	x		2 kV	2 kV	2 kV
2	10 %	x		4 kV	4 kV	4 kV
3	50 %		x	8 kV	6 kV	8 kV
4	10 %		x	15 kV	8 kV	15 kV

Table 1: IEC 61000-4-2 severity levels and test voltages.

Level	Indicated Voltage	First Peak Current of Discharge (±10 %)	Risetime with Discharge Switch	Current at 30 ns (±30 %)	Current at 60 ns (±30 %)
1	2 kV	7.5 A	0.7 ns to 1 ns	4 A	2 A
2	4 kV	15 A	0.7 ns to 1 ns	8 A	4 A
3	6 kV	22.5 A	0.7 ns to 1 ns	12 A	6 A
4	8 kV	30 A	0.7 ns to 1 ns	16 A	8 A

Table 2: IEC 61000-4-2 ESD current waveform parameters.

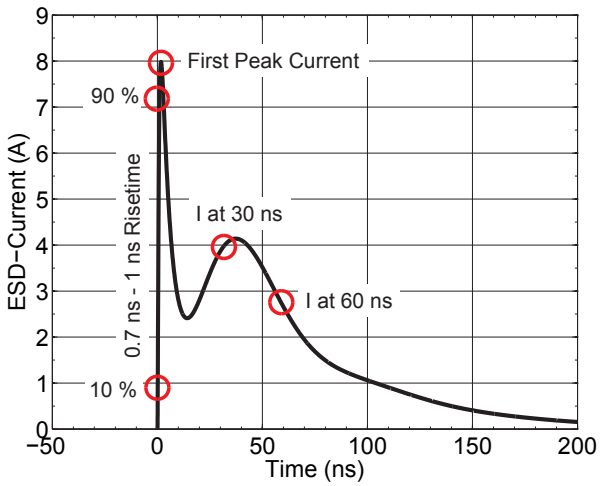


Figure 1: 2 kV ESD current pulse waveform according IEC 61000-4-2 (R=330Ω, C=150 pF) [1]

Fig. 1 shows a 2 kV ESD current pulse waveform according IEC 61000-4-2 with a R=330Ω and C=150 pF discharge circuitry. The ESD current waveform at a certain indicated discharge voltage is specified with 4 parameters (Tab. 2):

1. rise time 0.7 - 1 ns
2. first peak current of discharge (±10 %)
3. Current at 30 ns (±30 %)
4. Current at 60 ns (±30 %)

1.3 The IEC 61000-4-5 Surge Immunity Standard

IEC 61000-4-5 addresses the most severe transient conditions on both power and data lines. These are transient caused by lightning strikes and switching. Switching transients may be the result of power system switching, load changes in power distribution systems, or short circuit fault conditions. Lightning transients may result from a direct strike or induced voltages and currents due to an indirect strike.

The IEC 61000-4-5 standard defines a transient entry point and a set of installation conditions. The transient is defined in terms of a generator producing a given waveform and having a specified open circuit voltage and source impedance. Two surge waveforms are specified: the 1.2 x 50 µs open-circuit voltage waveform and the 8 x 20 µs short-circuit current waveform (Fig. 2 and Fig. 3).

Transient stress levels for each entry point into the system are defined by installation class. The six classes are defined as:

Class 0: well protected environment

Class 1: partially protected environment

Class 2: well separated cables

Class 3: cables run in parallel

Class 4: multi - wire cables for both electronic and electrical circuits

Class 5: connection to telecommunications cables and overhead power lines (low density populated areas)

Class		Power Supply		Unsym. Lines (Long Distance Bus)		Sym. Lines	Data Bus (Short Distance)
		Coupling Mode		Coupling Mode		Coupling Mode	Coupling Mode
		Line-Line Zs= 2 Ω	Line-GND Zs=12 Ω	Line-Line Zs=42 Ω	Line-GND Zs=42 Ω	Line-GND Zs=42 Ω	Line-GND 42 Ω
0	voltage current	No Requirement					
1	voltage current	(n/a)	0.5 kV 42 A	(n/a)	0.5 kV 12 A	1 kV 24 A	(n/a)
2	voltage current	0.5 kV 250 A	1 kV 83 A	0.5 kV 12 A	1 kV 24 A	1 kV 24 A	0.5 kV 12 A
3	voltage current	1 kV 500 A	2 kV 167 A	1 kV 24 A	2 kV 48 A	2 kV 48 A	(n/a)
4	voltage current	2 kV 1000 A	4 kV 333 A	2 kV 48 A	4 kV 95 A	(n/a)	(n/a)
5	voltage current	Note[1]	Note[1]	2 kV 48 A	4 kV 95 A	4 kV 95 A	
Wave-forms	voltage current	1.2 x 50 µs 8 x 20 µs	1.2 x 50 µs 8 x 20 µs	1.2 x 50 µs 8 x 20 µs	1.2 x 50 µs 8 x 20 µs	1.2 x 50 µs 8 x 20 µs	1.2 x 50 µs 8 x 20 µs

Table 3: IEC 61000-4-5 Severity Levels.

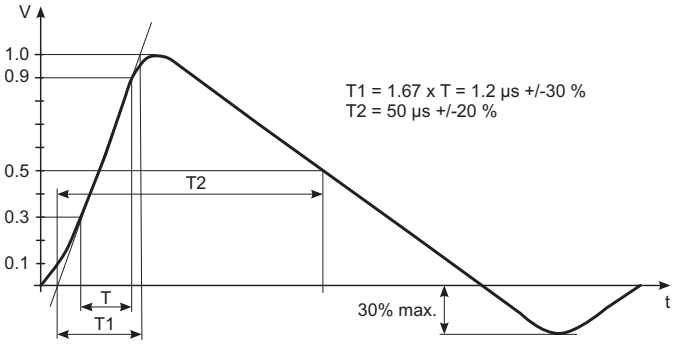


Figure 2: IEC 61000-4-5 1.2 µs / 50 µs voltage impulse.

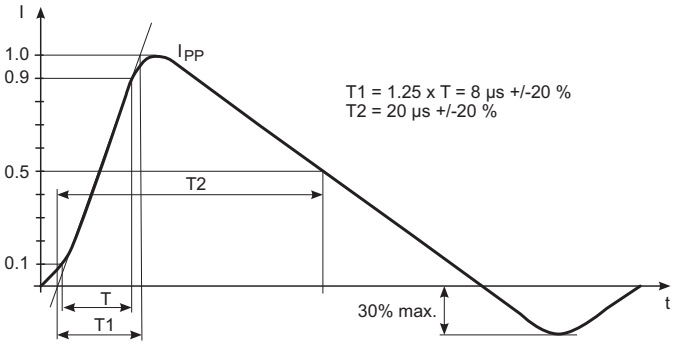


Figure 3: IEC 61000-4-5 8 µs / 20 µs current impulse.

A class 0 environment is considered the lowest threat level a has no transient stress requirements. The class 5 environment is the most severe and requires the highest transient stress level testing.

Tab. 3 summarizes threat levels as a function of installation class. Values of voltage stress using the 1.2 x 50 µs waveform are given. Corresponding current values are calculated by dividing the open-circuit voltages by the source impedances. The short-circuit current values are more useful in choosing a suppression element. The short circuit current stress levels are defined with the 8 x 20 µs waveform for power supply applications with a 2 Ω source impedance. For data lines requiring a 42 Ω source impedance, the short-circuit current waveform is defined as 8 x 20 µs. For telecommunications applications, the open-circuit voltage is defined as 10 x 700 µs and the short-circuit current is a 5 x 300 µs waveform. The source impedance is given as 40 Ω. The type of suppression element needed for IEC 61000-4-5 class surges depends upon the threat level and installation class. For power supply applications high power devices are required. A discrete device or an assembly may be required depending on the application. TVS diodes are the best choice for data line applications and secondary board level protection because of their superior clamping voltage characteristics and fast response time.

1.3.1 Surge Test Measurement Setup

Fig. 4 shows the measurement setup for the 8/20 µs surge test of TVS diodes. The amplitude of the pulse generator is adjusted for typical peak current (Fig. 3) of

[1] Depends on class of local power supply system.

Parameter	Component Level ESD Test	System Level ESD Test
Stressed pin group	All pin combinations	Few special pins
Supply	Unpowered	Powered & unpowered
Test methodology	Standardized	Application specific
Test set-up	Commercial tester & sockets	Application specific
Typical qualification goal	1 . . . 2 kV JEDEC HBM (ANSI/ESDA/JEDEC JS-001-2012, [4])	8 kV Contact (IEC 61000-4-2, [1]) 15 kV Air (IEC 61000-4-2, [1])
Corresponding peak current	0.65 . . . 1.3 A	>20 A
Junction/ambient temperature	27 °C	Application specific
Failure signature	Destructive	Functional or destructive

Table 4: Comparison of Component and System Level ESD Test.

Standard	R/C Network	Rise-Time	First Peak Current	Broad Peak Current	Decay Time
ANSI/ESDA/JEDEC JS-001-2012	R = 1.5 kΩ, C = 100 pF	2-10 ns	0.67 A/kV	-	130-170 ns
IEC 61000-4-2	R = 330 Ω, C = 150 pF	0.7-1 ns	3.75 A/kV	2 A/kV	-

Table 5: Comparison ESD current waveform parameters.

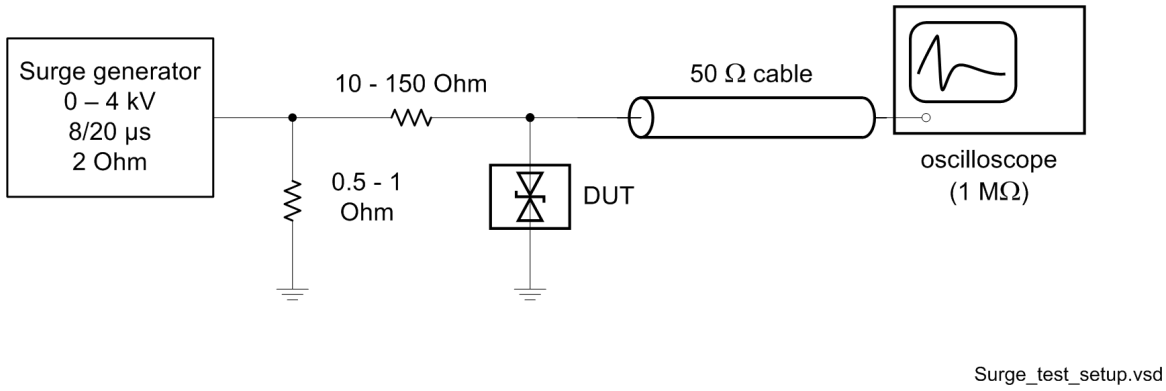


Figure 4: 8/20 µs surge test measurement setup.

I_{PP}=1 A and I_{PP}=3 A, respectively for TVS products. The peak clamping voltage at e.g. I_{PP1}=1 A and I_{PP2}=3 A is measured and presented in the data sheet. The dynamic resistance can be calculated as follows:

$$R_{dyn,surge} = \frac{V_{CL2} - V_{CL1}}{I_{PP2} - I_{PP1}} \quad (1)$$

1.4 Comparison of Component Level and System Level ESD

Component level ESD stress occurs in wafer- or component-fabrication areas caused by static charge generation and during product lifetime due to human handling electrostatic discharge [5], [6]. Normally, IC's are designed to meet 1 kV to 2 kV HBM ESD robustness according the joint JANSI/ESDA/JEDEC standard JS-001-2012 [4]. Recent investigations have shown that a level of >500 V HBM (ANSI/ESDA/JEDEC JS-001-2012) ESD robustness is sufficient for state-of-the-art fabrication technologies [7]. The recommendations therein are intended for component level safe ESD requirements and will have little or no effect on system level ESD results. Systems and system boards should continue to be designed to meet appropriate ESD threats regardless of the components in the systems that are meeting the new recommendations [7], and that all proper system reliability must be assessed through the IEC test method [1]. Tab. 4 shows a comparison of component and system level ESD test procedure for product qualification. Tab. 5 shows the

typical ANSI/ESDA/JEDEC JS-001-2012 and IEC 61000-4-2 ESD current waveform parameters. Fig. 5 compares the ESD current waveform for 1 kV component level ESD (ANSI/ESDA/JEDEC JS-001-2012) and 1 kV system level ESD (IEC 61000-4-2).

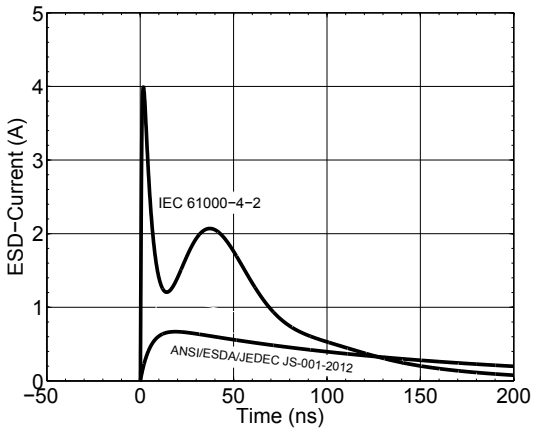


Figure 5: Comparison of a 1 kV component-level ESD pulse according HBM ANSI/ESDA/JEDEC JS-001-2012 (R=1.5 kΩ, C=100 pF) [4] and a 1 kV system-level ESD pulse according IEC 61000-4-2 (R=330Ω, C=150 pF) [1].

2 Characterization of ESD Protection Devices and Circuits with a Transmission Line Pulse System

A Transmission-Line Pulse (TLP) system is a valuable measurement equipment for circuit and device characterization in pulsed operation mode in the high power time domain [8].

The classical TLP measurement system consists of a 50 Ω high voltage pulse generator, a high speed digital oscilloscope, a Source Meter Unit (SMU) and a control computer. The typical range of the pulse waveform parameters are: output voltage amplitude in the range of up to ±4 kV, output currents up to ±80 A, pulse width in the range of 1 ns up to 1.6 µs, pulse rise time in the range from 100 ps to 50 ns. The transient voltage and currents in the device under test (DUT) are recorded using a high speed digital oscilloscope with e.g. 12 GHz bandwidth and 40 GS/s sampling rate.

Such a measurement system can be used very effective to investigate transient characteristics of semiconductor devices and circuits in the high voltage and high current time domain. For electrostatic discharge sensitivity testing two standards are available [9] and [10].

This section gives an introduction about the basic principle of a high voltage TLP generator and how it can be used effectively for device characterisation and electrostatic discharge (ESD) design.

2.1 Pulsed Device Characterisation

The characterisation of devices and circuits in pulsed mode has two major advantages: a) diminish self heating effects and b) limit the dissipated energy in the device in order to avoid destruction. Usually the pulsed mode is helpful to investigate specific device or circuit parameters in the time domain, such as:

- High current I-V characteristics
- Turn-on/off transient characteristics
- Breakdown effects
- Charge recovery effects e.g. reverse and forward recovery of diodes
- Safe Operating Area (SOA) or Wunsch-Bell characteristics
- Ruggedness of transistors (RF-LDMOS, DMOS, CMOS, BJT, . . .)
- MOS gate oxide reliability
- Packaging and handling ESD, published in the joint standard ANSI/ESDA/JEDEC JS-001-2010
- Human-Metal-Model (HMM) and system level ESD (IEC-61000-4-2)

If the pulse width and pulse rise time becomes small, impedance matched transmission lines are used to connect the DUT to the measurement system (Fig. 6).

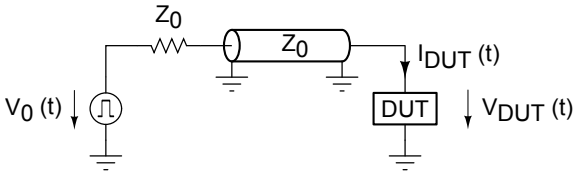


Figure 6: Simplified pulsed mode measurement setup

In this setup for a passive DUT the maximum open load output voltage is

$$V_{DUT,max} = V_0 \tag{2}$$

and the maximum short circuit DUT current is

$$I_{DUT,max} = \frac{V_0}{Z_0}. \tag{3}$$

The pulsed voltage source V_0 and the characteristic impedance of the transmission lines Z_0 limit the maximum

DUT voltage and short circuit DUT current. To achieve higher level of V_{DUT} and I_{DUT}, V_0 can be increased and Z_0 can be decreased.

Usually $Z_0 = 50\,\Omega$ is widely used as a compromise between low loss and power handling capability for coaxial cables and measurement systems [11]. Example: in order to achieve 40 A short circuit DUT current in a $Z_0 = 50\,\Omega$ system, a pulsed voltage source of 2 kV is required.

So far no commercial pulse generators based on solid-state devices or vacuum tubes are available to handle such high voltage with excellent pulse waveform quality with a dynamic range from below 1 V up to several kilo volts amplitude. The concept of using high voltage charged transmission lines to generate rectangular pulse waveforms with high quality is well known for a very long time, which has been described in [12] or even much earlier. This leads us to the classical transmission line pulse generator.

2.2 The Transmission Line Pulse Generator

Fig. 7 shows the basic concept of the classical TLP generator. It consists of a high voltage source V_0, an impedance matched transmission line TL_1, the switch S_1 and the transmission line TL_2. The necessary core elements are just two: TL_1 and S_1. In the bottom of Fig. 7 two possible circuit realisations of the TLP generator are shown. Both are based on the basic principle of an open ended transmission line TL_1 with a characteristic impedance Z_0 and a mechanical length L. TL_1 is often called charge line. For the initial condition at times $t < 0$, TL_1 has to be charged with high voltage V_0. This can be done at the open end of TL_1 using a resistor

$$R \gg Z_0 \tag{4}$$

or directly at the switch side using a single pole, double throw switch (SP2T). v is the propagation velocity in the transmission line

$$v \approx \frac{c}{\sqrt{\epsilon_r}} \tag{5}$$

with c the speed of light and ϵ_r the relative dielectric constant of the transmission line inner insulator. $v \approx 0.2$ m/ns is a good rule of thumb for polytetrafluoroethylene (PTFE or Teflon) dielectrics.

2.2.1 How the Pulse is Generated

In the general case, the amplitude of the wave reflected at the open end of the charge line is determined by the reflection coefficient ρ. The value of ρ depends on the characteristic impedance Z_0 and R, the termination resistance at the end of the line:

$$\rho = \frac{R - Z_0}{R + Z_0} \tag{6}$$

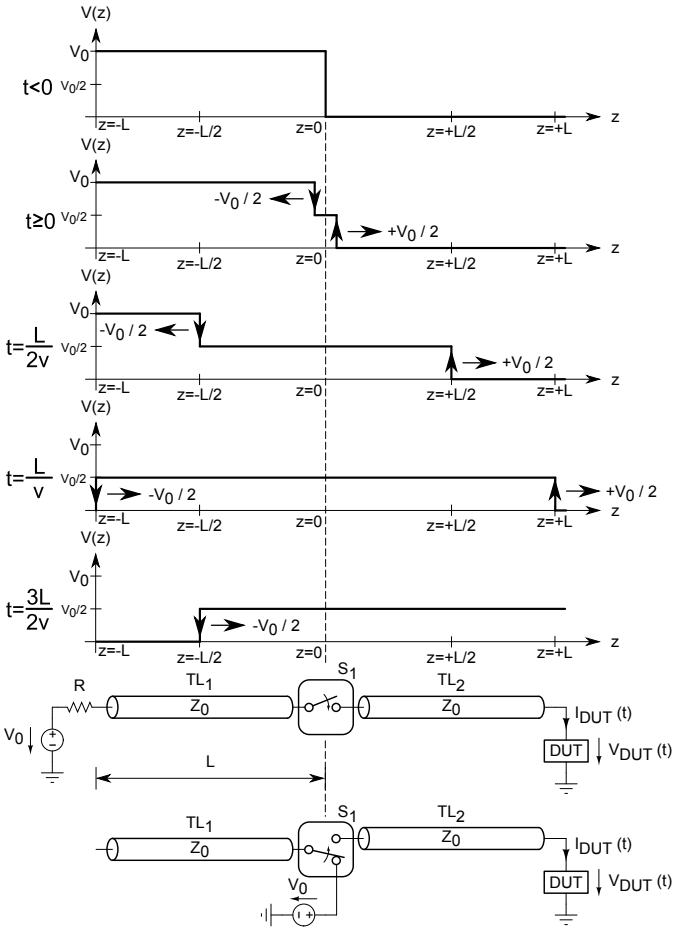


Figure 7: The classical transmission line pulse (TLP) generator

If R is very high or ∞, then $\rho = +1$. This means when a voltage wave hits the open end, the current has nowhere to go, and so a voltage wave of the same polarity propagates back up the line, adding to the original voltage. With this background we can consider the states along the charge line TL_1 in Fig. 7:

$t < 0$ This is the initial condition: the switch S_1 is open and TL_1 is charged with the high voltage V_0 constant over the length L. TL_2 has no voltage potential.

$t = 0$ S_1 switched on: after short time $t > 0$ the voltage at the switch drops down to $Z_0 \cdot V_0/(Z_0 + Z_0) = V_0/2$ because source impedance of TL_1 and load impedance of TL_2 is Z_0. At this time two voltage waves start immediately to propagate in opposite directions. One voltage wave with amplitude $+V_0/2$ starts to propagate in positive z direction. Another voltage wave with amplitude $-V_0/2$ starts to propagate in negative z direction, adding to the original voltage.

$t = \frac{L}{2v}$ At this time both voltage waves have propagated already a distance of $z = \pm L/2$.

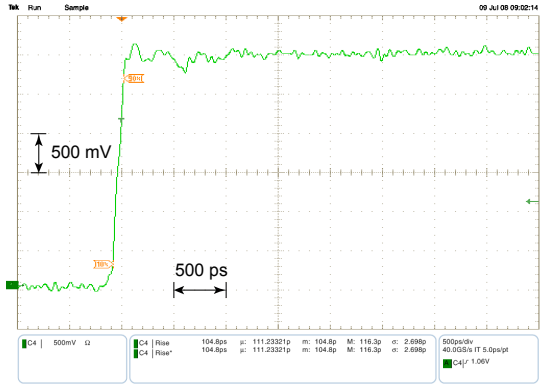


Figure 8: TLP waveform measurement result at 40 GS/s

$t = \frac{L}{v}$ The voltage wave along negative z direction with amplitude $-V_0/2$ hits the open end of TL_1. A voltage wave with same polarity propagates back up the line and adds to the original voltage $-V_0/2 + V_0/2 = 0$ which leads to cancellation.

$t = \frac{3L}{2v}$ The cancellation voltage wave propagates back up the line and has reached $z = -L/2$. At the same time the other voltage wave with $+V_0/2$ amplitude has reached the location $z = 3L/2$ (not shown in Fig. 7).

This consideration leads to the conclusion that a rectangular pulse waveform is propagating along the transmission lines. On the transmission line a mechanical distance of $2L$ is travelled by the waveform and the pulse width in the time domain is

$$t_p = \frac{2L}{v} \approx \sqrt{\epsilon_r} \cdot \frac{2L}{c} \tag{7}$$

which is the basic design equation of the classical TLP generator. Fig. 8 shows a typical pulse waveform rising edge, measured with a 12 GHz oscilloscope (Tektronix TDS6124C) at 40 GS/s sampling rate.

2.3 The TLP Measurement System

For the investigation and development of ESD protection devices T. Maloney and N. Khurana did introduce TLP in 1985 for the first time [13]. Barth Electronics introduced the first commercial TLP system in the mid-1990s including the concept and calibration of the measurement system [14], [15]. The DUT (Fig. 6) is excited with rectangular pulse waveforms with variable amplitude. The voltage waveforms $V_{DUT}(t)$ and current waveforms $I_{DUT}(t)$ at the DUT are recorded using a digital high speed oscilloscope with single shot waveform capture capability. In general, the entire waveforms are valuable for the evaluation of the transient DUT characteristics in the time domain. Especially for ESD design the pulsed IV-characteristic, also called TLP-characteristic, is important (Fig. 9). Out of

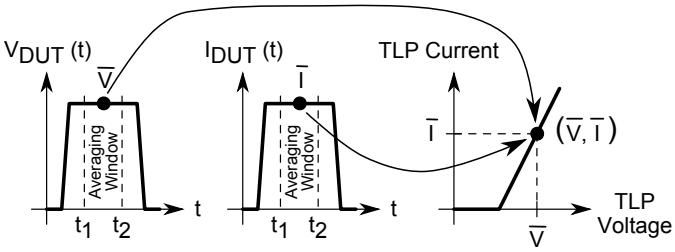


Figure 9: Extraction of the TLP characteristic

each captured voltage and current waveforms the arithmetic mean values $\overline{V}$ and $\overline{I}$ are calculated in the averaging window between t_1 and t_2. For all pulse amplitudes these mean values are collected in an IV-diagram with the so called TLP voltage $\overline{V}$ on the x-axis and the TLP-current $\overline{I}$ on the y-axis. This diagram represents the quasi-stationary IV-characteristic of the DUT. It is always necessary to specify four important measurement conditions in addition to the diagram:

1. characteristic impedance of the TLP system
2. width of the pulse
3. rise time of the pulse
4. location of the averaging window: t_1 and t_2

Usually after the caption of each pulse waveform a dc leakage measurement is done and a second plot is added to the TLP-characteristic: bottom x and left y axis remain as the traditional TLP voltage and current, and on top x and left y the evolution of leakage current (top x) versus TLP current (left y) is added [14], [15], as shown in Fig. 10.

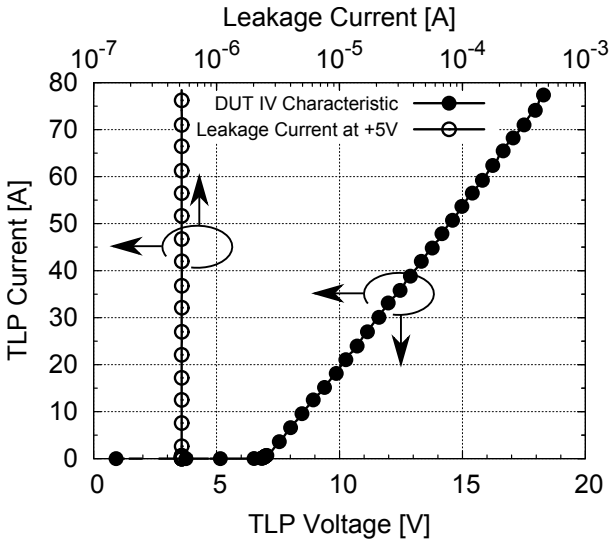


Figure 10: Measured TLP characteristic of a 5 V TVS diode

2.3.1 Discrete Voltage and Current Sensors

Fig. 11 shows a pulsed mode measurement setup with discrete sensors for current and voltage. The sensors should be located as close as possible to the DUT.

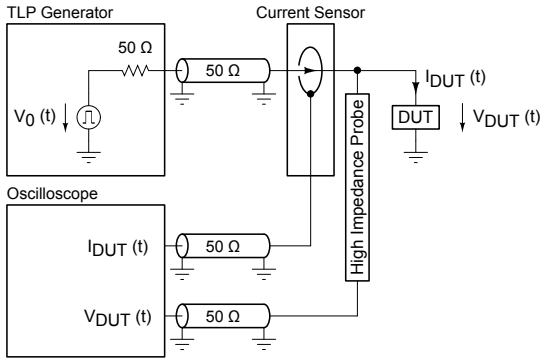


Figure 11: Pulsed mode measurement setup with discrete sensors

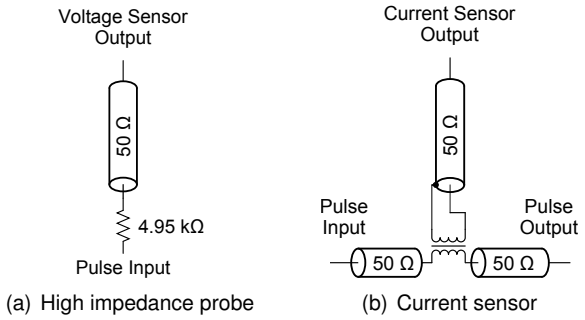


Figure 12: Discrete voltage and current sensors

Fig. 12 show practical realisations for discrete voltage and current probes. Voltage probes can be realised easier for higher bandwidth than current probes. The high impedance V-probe shown in Fig. 12(a) has an input impedance of 5 kΩ and a sensitivity (or voltage division ratio) of $50/(4950 + 50) = 0.01$ V/V. The voltage sensor output must be terminated with 50 Ω. GGB [16] offers probe tips with such integrated resistors (Model 10) for wafer-level testing up to 11 GHz.

Discrete I-probes for pulse waveforms are often based on transformers, as shown in Fig. 12(b). The Tektronix CT-1 and CT-2 current sensors [17] have become an industry standard for TLP applications up to 100 A, depending on the pulse width t_p.

Tab. 6 summarises the typical specifications of the Tektronix CT-1 and CT-2 current sensors. The maximum current depends on the pulse width and is limited by the L/R time constant and the amp x second rating. If the product (current x pulse width) exceeds the maximum rating, the core saturates and the output drops to zero.

Sensor	Sensitivity [V/A]	Bandwidth [GHz]	Rise Time [ns]	A x µs Rating
CT-1	5	1	< 0.35	1
CT-2	1	0.2	< 0.5	50

Table 6: Comparison of current sensor parameters [17]

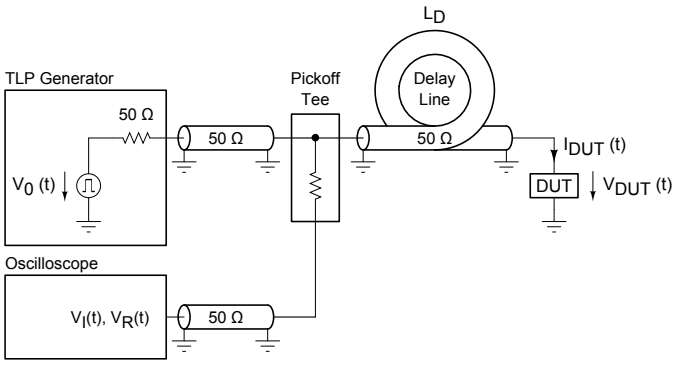


Figure 14: Simplified VF-TLP measurement setup

2.3.2 Remote Voltage and Current Sensing

The voltage $V_{DUT}(t)$ and current $I_{DUT}(t)$ can be calculated out from incident and reflected waves, far away from the DUT. This becomes indispensable if the pulse width becomes very small and the overlapping region of incident and reflected pulses is inadequate to take an I-V measurement directly at the DUT using discrete sensors. Usually this is the case at pulse width $t_p \leq 10$ ns. The adequate measurement setup, shown in Fig. 14, is called very-fast TLP (VF-TLP) [18], [19] based on time-domain reflectometry (TDR).

The voltage probe (pickoff tee) is placed so far away from the DUT that incident and reflected waveforms appear separated. This can be achieved by inserting a delay line between the probes and DUT of mechanical length

$$L_D > \frac{t_p \cdot v}{2} \approx t_p \cdot \frac{c}{2\sqrt{\epsilon_r}} \tag{8}$$

With separated pulses the response at the DUT can be calculated by numerically overlapping the incident and reflected pulses according to following equations:

$$V_{DUT}(t) = V_I(t) + V_R(t) \tag{9}$$

$$I_{DUT}(t) = I_I(t) - I_R(t) \tag{10}$$

$V_I(t)$, $V_R(t)$ are incident and reflected voltage waveforms. $I_I(t)$, $I_R(t)$ are incident and reflected current waveforms. Since incident and reflected pulses appear separate, there is a correlation between the current and voltage on the transmission line defined by its characteristic impedance Z_0 according to:

$$I_I(t) = \frac{V_I(t)}{Z_0} \tag{11}$$

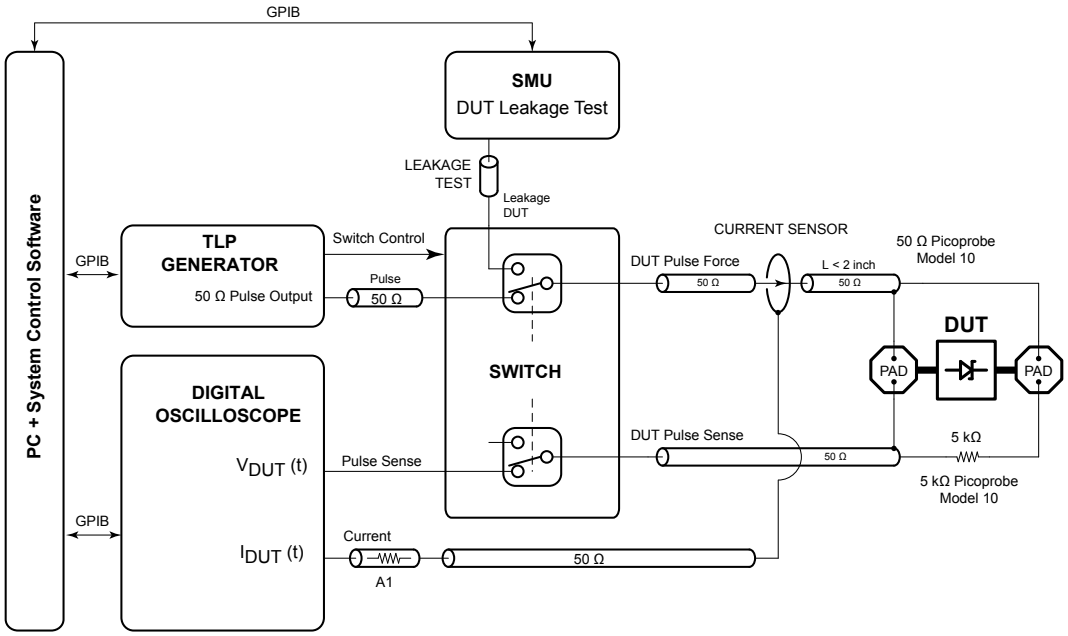


Figure 13: Four point Kelvin TLP method including dc leakage measurement

$$I_R(t) = \frac{V_R(t)}{Z_0} \tag{12}$$

By combining Eqn. 11, Eqn. 12 and Eqn. 10, the following equation is obtained

$$I_{\mathrm{DUT}}(t) = \frac{V_I(t) - V_R(t)}{Z_0} \tag{13}$$

with $Z_0 = 50\ \Omega$. Thus, $V_I(t)$ and $V_R(t)$ gives enough information to calculate $V_{\mathrm{DUT}}(t)$ and $I_{\mathrm{DUT}}(t)$. In order to refine the results and to improve the accuracy, the frequency response of all components have to be included in the calculations by calibration and deembedding.

2.3.3 Error Sources

In order to achieve high resolution and high accuracy in the time domain, proper compensation of the non-ideal characteristics of the components in the measurement system is required. Major contribution come from interconnection cables (lossy transmission lines), voltage probes, current sensors and parasitic contact resistance in case of wafer measurements with probes.

2.4 Measurement Techniques

2.4.1 Four Point Kelvin TLP Method

To eliminate the error from non-zero contact resistance at high currents, a four point Kelvin method is preferred to measure the differential voltage directly at the device (Fig. 13) [20].

On the pulse force line a standard 50 Ω ground-signal (GS) type RF probe tip is used. The discrete current sensor should be located as close as possible to the DUT, typically not more than 5 cm far away. Thus, the setup is suitable for pulse with of $t_p > 5$ ns.

The sense probe tip has an integrated resistive divider, which enables the voltage to be measured with minimal parasitic loading (1-5 kΩ). The bandwidth of the high impedance probe is 7 to 11 GHz depending on the probe tip model.

To ensure differential voltage measurement directly at the device sheath waves should be suppressed on the transmission lines with ferrite cores and the ground of the probe tip holder should be isolated from the chuck and DUT fixture surrounding grounds.

The switch configuration with the source meter unit (SMU) is used to perform a dc (spot) leakage measurement in the pA to mA range after each high current pulse, in order to check if the DUT is already damaged or starts degrading. This method can be used for wafer-level as well as for component- or circuit level measurements.

2.4.2 Four Point Kelvin Very Fast TLP Method

For very fast TLP measurements (VF-TLP) with pulse widths < 10 ns, incident and reflected signals are recorded separately with a wide-band pickoff tee in the pulse-force line (see Fig. 15). The transient device response is calculated by combining the incident and reflected pulse signals numerically according Eqn. 9 (DUT voltage) and Eqn. 13 (DUT current).

But the DUT voltage is preferably measured directly

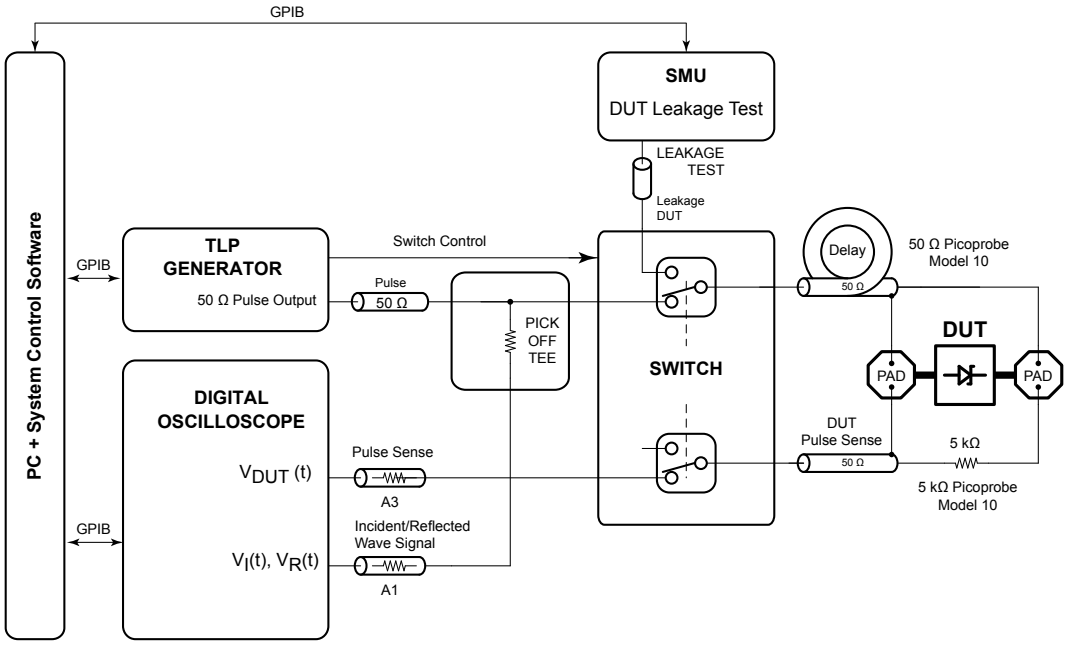


Figure 15: Four point Kelvin VF-TLP method including dc leakage measurement

with a second Picoprobe Model-10 with integrated voltage dividing resistor. This assures high bandwidth and minimizes the voltage error due to parasitic contact resistance. It also eliminates the digital noise that is typical for voltage measurements of low-ohmic devices with this method. In addition precise de-embedding of cable loss (amplitude and phase) enables accurate pulse measurements in the time-domain.

2.4.3 Reverse Recovery Time of Diodes

Reverse recovery measurements are becoming more and more important to determine the ESD robustness of circuits during operation. The recovery times can be measured extremely fast and efficient with TLP in the range from about 200 ps up to 1 µs. The DUT is mounted in a 50 Ω test fixture. When a diode is conducting current in the forward direction, a significant amount of charge is injected into the resistivity region and the PN junction of the diode. When reverse voltage is applied the extraction of this charge leads to the reverse recovery phenomenon [21], [22].

A diode reveals an excessive transient forward voltage when it is switched rapidly into the forward conduction region. The amplitude and time duration of this voltage peak is representing the forward recovery characteristic [23].

In the literature the reverse recovery time t_{rr} of diodes is defined multiple with different procedures of extraction (Fig. 17) and with different impedance conditions 50 Ω and 100 Ω [24], [25], [22].

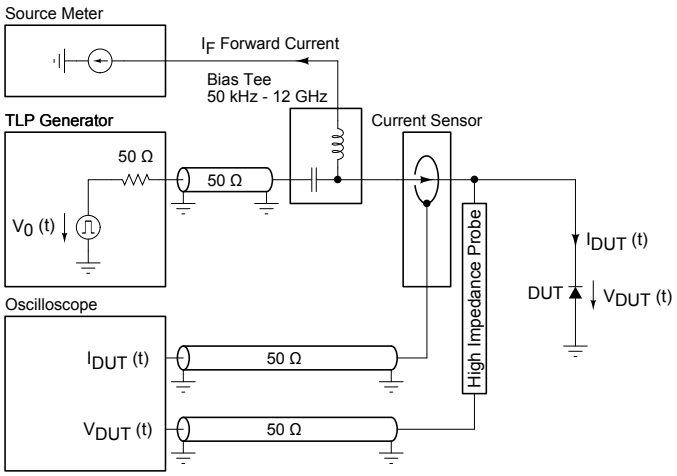


Figure 16: 50 Ω reverse recovery measurement setup

Reverse Recovery Definition - I: 25 % of nominal peak reverse current achieved This definition is used by commercial reverse recovery equipment manufacturers [24].

Reverse Recovery Definition - II: 10 % of nominal peak reverse current achieved This definition is recommended by the standard MIL-STD-750D, method 4031.3 for diodes with $t_{rr} < 6$ ns [22].

Reverse Recovery Definition - III: 90 % of reverse voltage achieved Michael Reisch propose in his book [25], Section 14.2.3, page 629, to use 90 % settling time of the

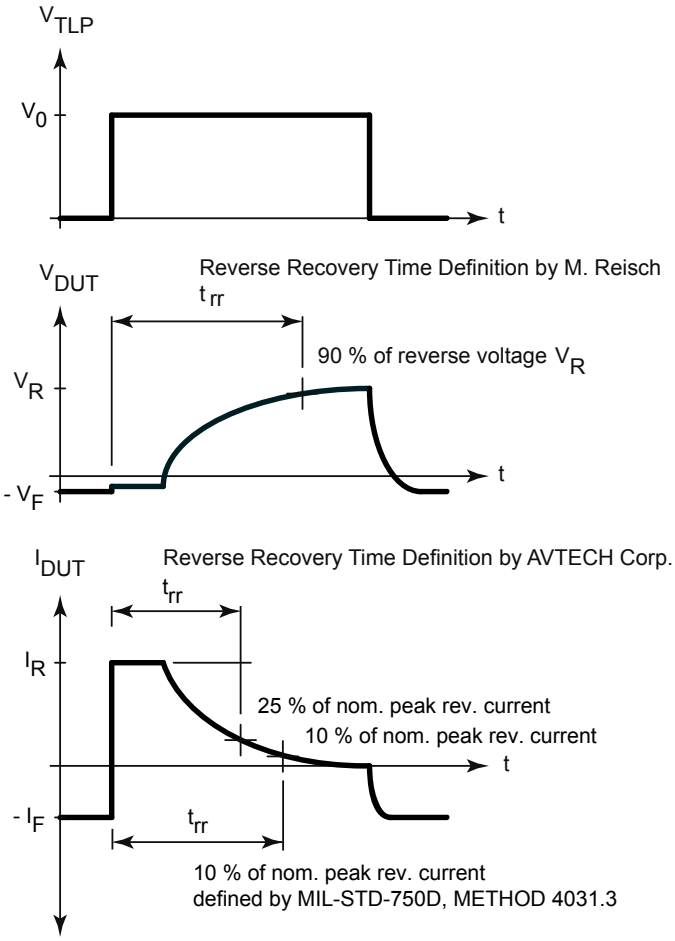


Figure 17: Typical reverse recovery waveforms with setup Fig. 16

reverse voltage. This definition gives a more worst case value of the reverse recovery time.

Reverse Recovery Definition - IV: reverse recovered charge A more general approach to evaluate the reverse recovery phenomenon is to plot the reverse recovered charge versus rate of rise of reverse current for different values of forward bias current [21].

If we follow [24] or the MIL-STD we can extract the reverse recovery time as follows:

- Set the pulse parameters to minimum available rise time (e.g. 100 ps) and a pulse width which is approximately two to three times the expected reverse recovery time.
- Operate diode in forward mode with a defined forward bias current I_F.
- Apply a reverse mode TLP pulse with a defined reverse voltage $V_R = V_{TLP} - |V_F|$. The pulse width of the TLP has to be increased until the voltage V_R remains steady state.
- Measurement of the nominal peak reverse current.
- Extract 25 % (or 10 % according MIL-STD) of the nominal peak reverse current.
- The time where the current I_{DUT} decreases down to 25 % (or 10 % according MIL-STD) of the nominal peak reverse current, is the reverse recovery time.

Fig. 16 shows the block diagram of a 50 Ω reverse recovery time measurement setup. The DUT is operated with 50 Ω source resistance. The DUT voltage and currents are measured with discrete sensors. Therefore the setup is useful for $t_{rr} >$ several ns.

Fig. 18 shows a typical result of a silicon diode, measured with setup Fig. 16 and extraction of 25 % of the nominal peak reverse current. For each forward current density just only one TLP sweep is required. Postprocessing of the captured TLP waveforms has been done using Matlab [26].

Fig. 19 shows a 100 Ω reverse recovery measurement setup. In contrast to Fig. 16 no current sensor is necessary, because $I_{DUT}(t) = V_A(t)/50\,\Omega$. The pickoff-tee is used to measure the voltage at the cathode $V_C(t)$. The interconnection between pickoff tee and the DUT results in a separation of incident and reflected waves. Therefore, the setup is useful for $t_{rr} >$ several ns.

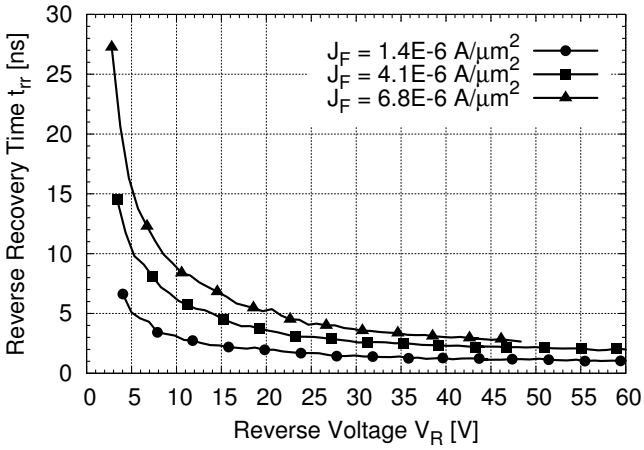


Figure 18: Reverse recovery measurement result of a silicon diode

For extremely small recovery times in the sub-ns range the setup in Fig. 20 is based on TDR remote sensing. The DUT voltage and current can be calculated as follows:

$$V_{DUT}(t) = V_I(t) + V_R(t) - V_A(t) \quad (14)$$

$$I_{DUT}(t) = \frac{V_A(t)}{Z_0} = \frac{V_I(t) - V_R(t)}{Z_0} \quad (15)$$

where $Z_0 = 50\,\Omega$, $V_I(t)$ is the incident voltage wave, $V_R(t)$ is the reflected voltage wave and $V_A(t)$ is the voltage at the anode of the DUT.

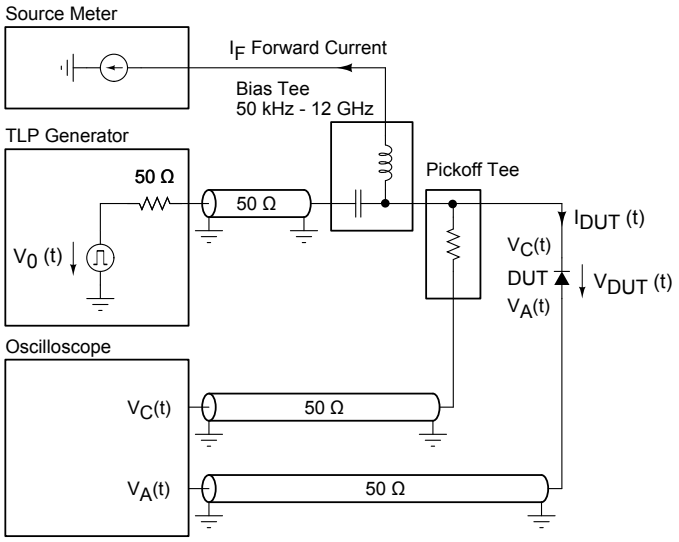


Figure 19: 100 Ω reverse recovery measurement setup

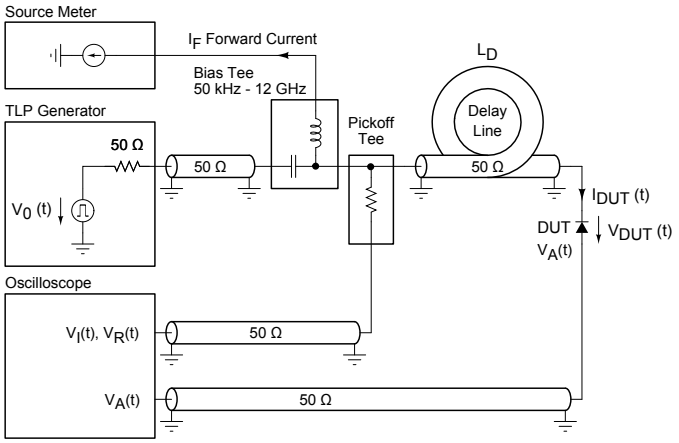


Figure 20: 100 Ω recovery measurement setup with TDR

2.4.4 Safe Operating Area

The Safe Operating Area (SOA) for ESD and pulsed electrical overstress (EOS) of active and passive devices can be easily measured using a TLP test system with variable pulse widths in the full range from about 1 ns to 1.5 µs.

2.4.5 System Level ESD Test (HMM)

State of the art TLP systems also offers a Human Metal Model (HMM) pulse waveform as an alternative test method to IEC 61000-4-2 with significant improved reproducibility of the test results.

2.5 Typical TLP Parameter

The following parameters are necessary to specify a TLP measurement:

TLP System Impedance: 50 Ω source impedance TLP systems are widely used. However, sometimes for specific snapback measurements and evaluation of the holding voltage a higher source impedance e.g. 500 Ω is recommended.

Pulse Width: The standard TLP pulse width is 100 ns because the total pulse energy is similar to ESD pulses according to the ANSI/ESDA/JEDEC JS-001-2012 HBM. The variable pulse width of commercial TLP measurement systems is in the range from 1 ns up to 1000 ns.

Pulse Rise-Time: Standard TLP systems have a pulse rise-time of 10 ns. VF-TLP systems offer rise times down to 100 ps to investigate turn-on characteristic of the DUT.

Averaging Window: The averaging window t_1 and t_2 has to be specified according Sect. 2.3, Fig. 9.

Spot Leakage and Curve Tracing: The test method for evaluation of the device failure must be defined. DC-presweep, spot leakage measurement and dc curve tracing are widely used.

2.6 Typical TLP Measurement Results

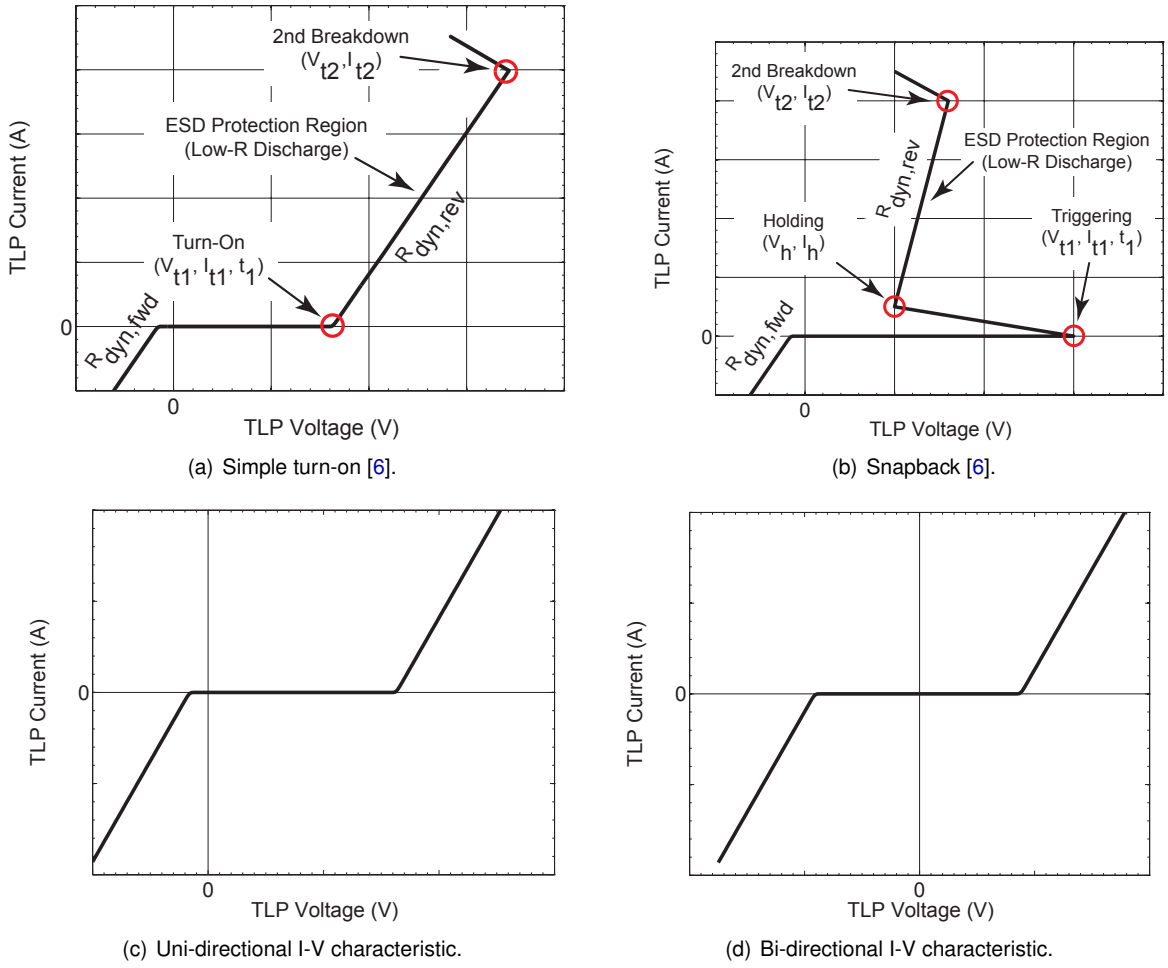
2.6.1 DC Sweep and Spot Leakage Measurement

The DUT ist characterized with a DC measurement procedure before, during and after TLP measurement. DC I-V characteristics or single spot measurements with forced currents or voltages can be used to monitor device dc drifts or damage during the TLP measurements.

2.6.2 TLP Characteristic

Fig. 21 illustrates typical TLP characteristics which are discussed in general ESD protection concepts [6].

In Fig. 21(a) the protection device has a simple turn-on at a threshold point (V_{t1}, I_{t1}) with t1 being the triggering time to form a low-impedance channel to discharge ESD transients. In the reverse direction the dynamic resistance $R_{dyn,rev}$ can be observed. In the forward direction the device shows the forward dynamic resistance $R_{dyn,fwd}$. Fig. 21(b) shows a snapback device where it turned on at a triggering point (V_{t1}, I_{t1}, t1), then driven into a snapback region with low holding (V_h, I_h) to create a low impedance discharge path. Again in the reverse direction the dynamic resistance $R_{dyn,rev}$ can be observed. In the forward direction the device shows the forward on-resistance $R_{dyn,fwd}$. The second breakdown or irreversible destruction of the device can be observed at the point (V_{t2}, I_{t2}). Fig. 21(c) shows a uni-directional characteristic. For negative voltages the device shows a forward PN-junction. In Fig. 21(d) a bi-directional characteristic is



(a) Simple turn-on [6].

(b) Snapback [6].

(c) Uni-directional I-V characteristic.

(d) Bi-directional I-V characteristic.

Figure 21: Typical TLP I-V characteristics used for ESD protection design.

presented. The device has a symmetrical transfer characteristic.

2.6.3 Definition of the Dynamic Resistance

The dynamic resistance of a device can be evaluated as the derivation dV/dI at a certain point on its high current I-V characteristic:

$$R_{\text{dyn}}(V, I) = \frac{dV}{dI} \tag{16}$$

If the I-V characteristic is constant in a wide range, as shown in e.g. Fig. 21(a) in reverse mode between turn-on and 2nd break down, then the dynamic resistance can be extracted with two points:

$$R_{\text{dyn}} = \frac{V_{t2} - V_{t1}}{I_{t2} - I_{t1}} \tag{17}$$

$$= \frac{V_{t2} - V_h}{I_{t2} - I_h} \tag{18}$$

(19)

for non-snapback and snapback devices. However, it is recommended to calculate the least squares fit out of the TLP characteristic between two TLP currents I_{TLP2} and I_{TLP1} as shown in Fig. 22. In general the dynamic resistance is dependent on:

- the location on the I-V characteristic of the device
- the pulse width
- the location and length of the averaging window to extract the mean of the voltage and current (Fig. 9)

For longer pulse width, like the 8 µs / 20 µs surge immunity test, increased self heating of the device is expected. The dynamic resistance can extracted as presented in Sect. 1.3.1.

2.6.4 Transient Overshoot and Clamping Voltage

The mystery about ESD protection is gone. Advanced TLP tester show that the first nanosecond can determine whether a chip will live or die. In essence sometimes chip

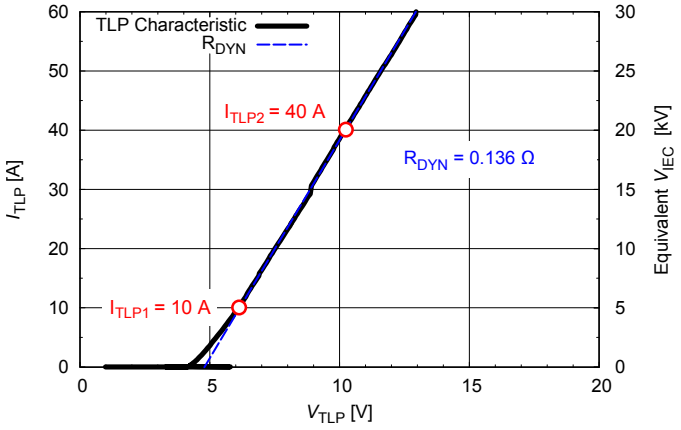


Figure 22: Extraction of the dynamic resistance using a least squares fit between two TLP currents I_{TLP2} and I_{TLP1}. The value of I_{TLP2} and I_{TLP1} can be defined in order to cover the interesting ESD current region.

manufacturers look at failure at voltages too late in the ESD event. Investigation of transient turn on and overshoot in the picosecond range makes the difference between protecting or not. In Sect. 3 two state of the art ESD protection device technologies will be compared.

2.7 How TLP fits to IEC 61000-4-2 ?

In general there is no correlation between standards and TLP measurement results allowed, because generation of the test signal is different and also the DUT sensitivity against waveform parameters (e.g. rise time) is most likely different. TLP generates a rectangular voltage waveform with 50 Ω source resistance. IEC61000-4-2 generates a different waveform shown in Fig. 1 at different time variant source impedance. However, the big advantage of TLP is the well defined and exact controllability of the waveform parameters such as source impedance, pulse width, rise time, amplitude.

In general the energy per pulse can be calculated as

$$E_{\text{pulse}} = \int_0^T p(t)\,dt \tag{20}$$

where $p(t)$ is the instantaneous power of the DUT. If the ESD protection device has turned on and has a very low resistance in order to shunt the ESD current the pulse energy of pulse waveforms according IEC 61000-4-2 (R=330Ω, C=150 pF) can be calculated as shown in Tab. 7.
Based on the broad peak currents shown in Tab. 5 a TLP impulse with 2 A amplitude, 63.4 ns pulse width, $<$ 600 ps rise time gives a pulse energy of 0.508 µJ which correlates very well to a 1 kV pulse according IEC 61000-4-2 (R=330Ω, C=150 pF). In general TVS diodes are not

IEC 61000-4-2 (R=330Ω, C=150 pF)	Pulse Energy
1 kV	0.5 µJ
2 kV	2.03 µJ
4 kV	8.1 µJ
8 kV	32.5 µJ
15 kV	114.5 µJ

Table 7: Pulse energy of ESD pulses according IEC 61000-4-2 (R=330Ω, C=150 pF).

sensitive to the first peak of the IEC pulse. In most cases the pulse energy is the performance limiting parameter. Therefore, a correlation with 2 A/kV can be used (Fig. 22, right y-axis).

2.7.1 TLP Parameter Set Recomendation

Using a TLP equipment to measure the dynamic resistance, turn-on characteristic and maximum fail current of TVS diode the following TLP parameters are recommended (Tab. 8):

Parameter	Value	Comment
TLP source impedance	50 Ω	
Maximum TLP current	up to ±80 A	2 A/kV IEC broad peak value (30 ns)
Pulse width	65 ns	worst case 100 ns
Pulse rise time	0.6 ns	correlates well with commercial IEC ESD tester.
Averaging window	30-60 ns	

Table 8: Typical TLP parameter for IEC 61000-4-2 (R=330Ω, C=150 pF) performance evaluation.

2.8 ESD Design

For packaging and handling ESD [4], TLP techniques up to 20 A have been used for the development of protection devices for more than 25 years. But recent developments are focused more on the development of system level ESD [1] protection solutions in two directions:

1. TLP characterisation of the ESD protection device
2. TLP characterisation of the device/circuit/system to be protected

With this information the ESD protection solutions can be designed and optimized in a systematic way, in contrast to the widely used try-and-error approach in the past.

15 kV air discharge, according IEC-61000-4-2 [1], is a common standard for original equipment manufacturers (OEM) of e.g. mobile phones.

15 kV contact discharge is used by the component suppliers to guarantee the performance (clamping characteristic) and quality (minimum 1000 pulses to withstand at maximum ratings) of the ESD protection devices (Fig. 23).

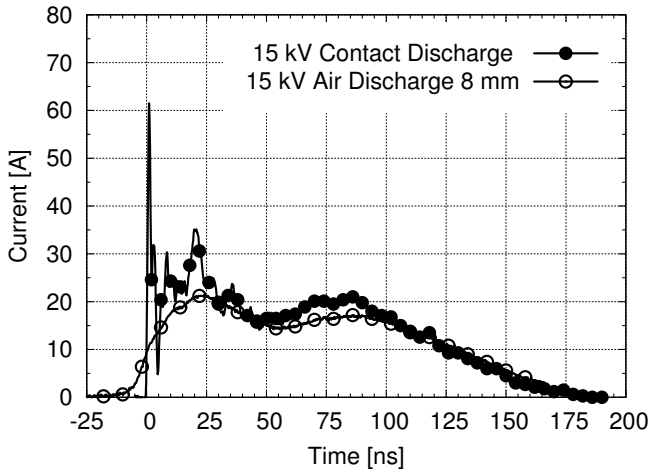


Figure 23: Comparison of 15 kV contact and air discharge current.

The first peak current at 15 kV contact discharge exceeds 60 A. Thus, a TLP system with 80 A capabilities is suitable to develop 15 kV system level ESD protection solutions.

2.8.1 Design Consideration

Fig. 24 shows an example where the clamping voltage of the TVS diodes is lower than the fail voltage V_{PIN} and fail current I_{PIN} of the IC. In this case the protection is sufficient and the improvement of the protection results in $I_{ESD} - I_{PIN}$.

In Fig. 25 the TVS is not able to protect the IC because the clamping voltage of the TVS is higher than the fail voltage of the IC. In this case an additional resistor can close the gap and can be calculated as follows:

$$R \geq \frac{(I_{ESD} - I_{PIN}) \cdot R_{DYN} + V_{t1} - V_{PIN}}{I_{PIN}} \qquad (21)$$

2.8.2 PCB Layout Consideration

ESD design results in a combination of four basic fields of knowledge: high frequency (RF), high voltage, high current and device physics. In the PCB design the following items have to be addressed:

- Clear definition of the ESD current path
- Solid GND and terminal connections

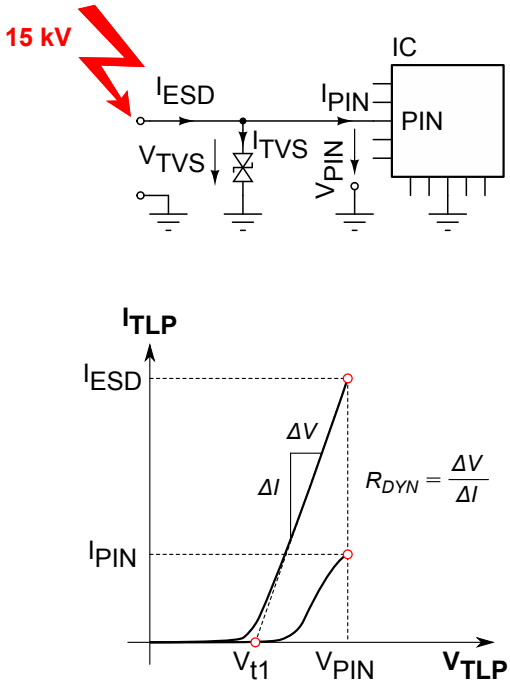


Figure 24: ESD protection: TVS is sufficient

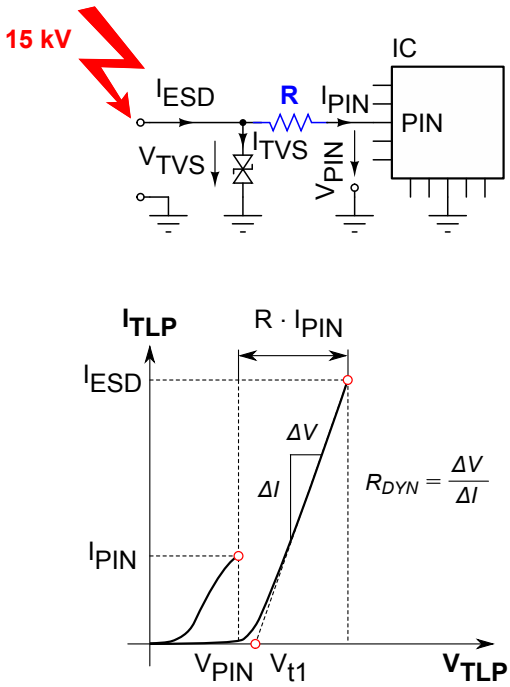


Figure 25: ESD protection: TVS is not sufficient. Additional resistor is required to close the gap.

- Low wiring parasitics
- Solid thermal connection of the protection device (especially necessary for surge applications)

2.9 Conclusion

The characterisation in pulsed mode is heavily used in the development of semiconductor devices and circuits including ESD. Pulse generators are required which can deliver pulse waveforms up to several kilo volts in 50 Ω. The TLP generator is still state of the art in handling such high dynamic range.

The basic principle of the classical TLP generator has been reviewed. TLP measurement systems based on discrete voltage and current sensors, and the TDR based remote sensing (VF-TLP) method for measurements in the sub-ns range have been presented.

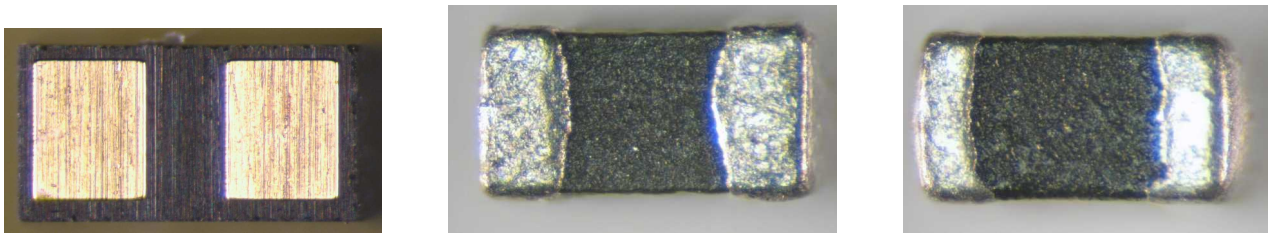
The four point Kelvin technique for TLP and VF-TLP is preferred for improved measurement accuracy at high currents.

Reverse recovery measurements are important to determine the ESD robustness of circuits during operation. Different measurement configurations, especially for the sub-ns region, are explained.

Finally, ESD design can be done in a very systematic way first time right such as RF design using advanced TLP techniques.

3 Comparison of ESD Protection Technologies: Silicon Transient Voltage Suppressor (TVS) Diodes versus Multilayer Varistors (MLV)

Fig. 26 shows a photograph of 3 devices for performance comparison. All devices have been measured with 400 µm pitch wafer-level RF-probes contacted directly at its pads. This is a significant advantage because no 50 Ω test fixture and no deembedding is necessary. The transient waveforms are measured directly on the pads of the devices which reflects exactly the application on the PCB.



(a) Infineon TVS ESD08V0R1B-02LS and ESD206-B1-02LS (0201).

(b) MLV-1 (0201).

(c) MLV-2 (0201).

Figure 26: Comparison of ESD protection devices: Transient Voltage Suppressor diodes (TVS, silicon technology) and Multi-Layer Varistors (MLV, ceramic technology).

3.1 DC Sweep

In comparison to best-in-class 0201 MLV in ceramic technology the 0201 TVS diode in silicon technology has much lower DC leakage current. This results in significant improvement in battery life time of mobile handsets using silicon TVS diodes. In Fig. 27 the leakage current of the TVS diode ESD8V0R1B-02LS is even lower than the measurement limit of the equipment. Breakdown is well defined and sharp.

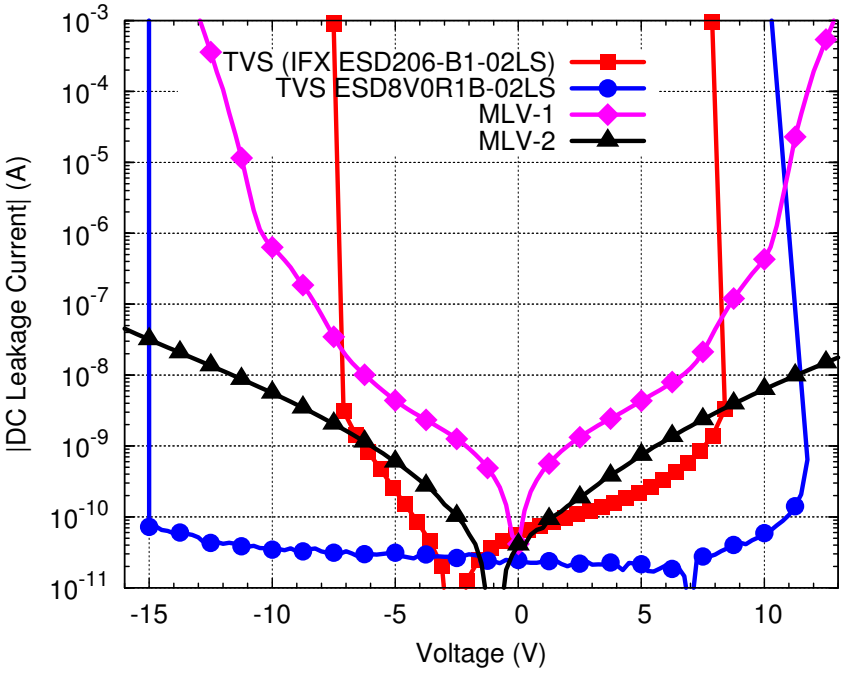


Figure 27: DC characteristic comparison.

3.2 Dynamic Resistance

Fig. 28 presents the TLP characteristics of ceramic MLVs compared to silicon TVS. At 25 A the clamping voltage of the MLVs are 2.5 times and 5.5 times higher compared to the silicon TVS. The TVS has 0.77 Ω compared to 2 Ω and 5 Ω of the MLVs, respectively. Fig. 29 gives a detailed view at lower current levels. The TVS ESD206 shows lowest dynamic resistance and steepest turn-on characteristic.

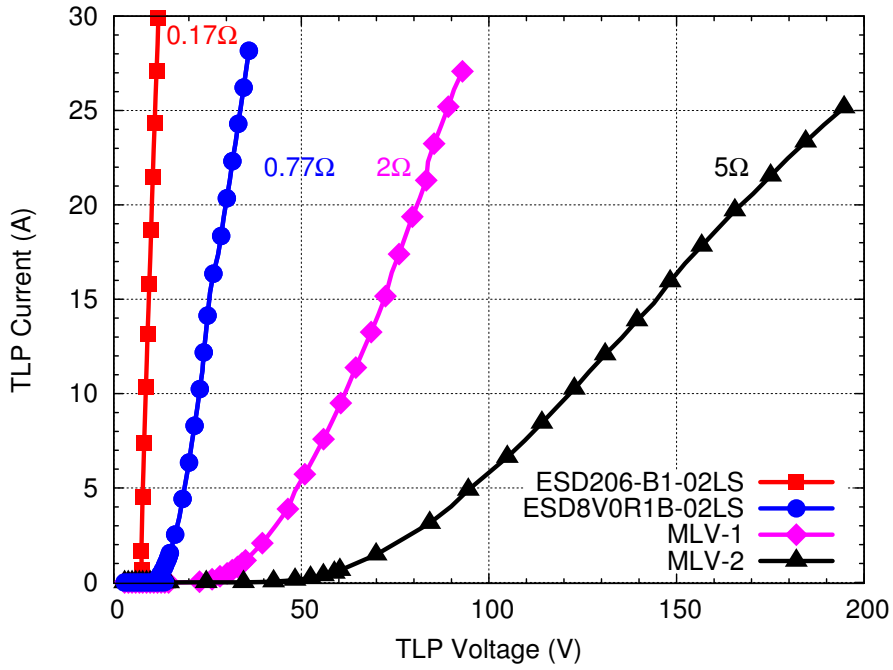


Figure 28: I/V characteristic comparison. TLP-parameter: 50 Ω, 100 ns pulse width, 290 ps rise time.

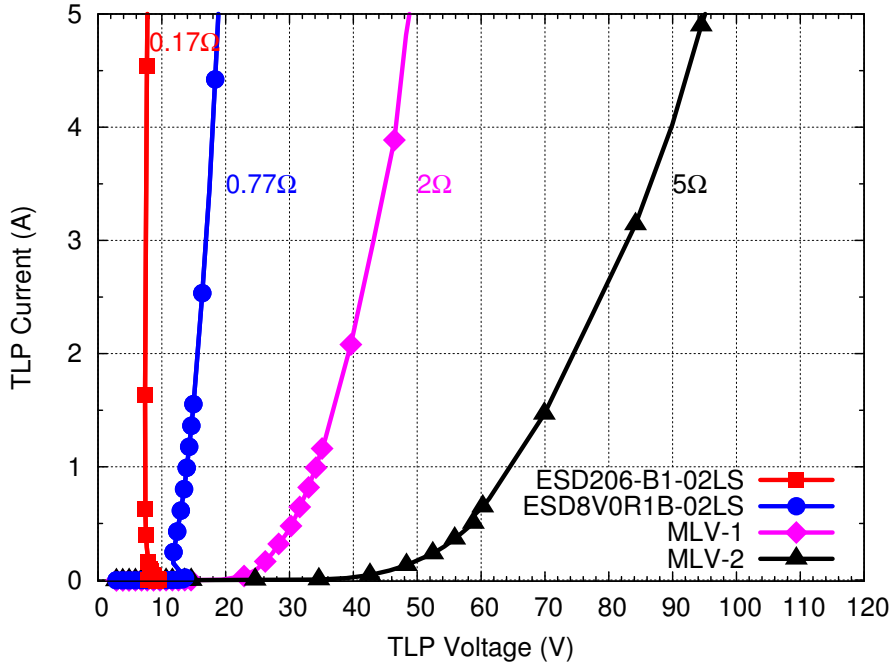


Figure 29: I/V characteristic comparison: detail view.

3.3 Transient Overshoot and Clamping Voltage

In Fig. 30 the transient overshoot of MLV-2 is 250 V at 16 A TLP current, which relates to approximately 8 kV according IEC-61000-4-2. The overshoot of 250 V is too high for sensitive sub-100 nm CMOS technologies. The TVS diode results in much lower clamping voltage at same ESD current level. In general the TVS diode shows the lowest clamping voltage. Fig. 31 shows the turn-on in detail at 25 ps sampling interval. The TVS has also very low overshoot.

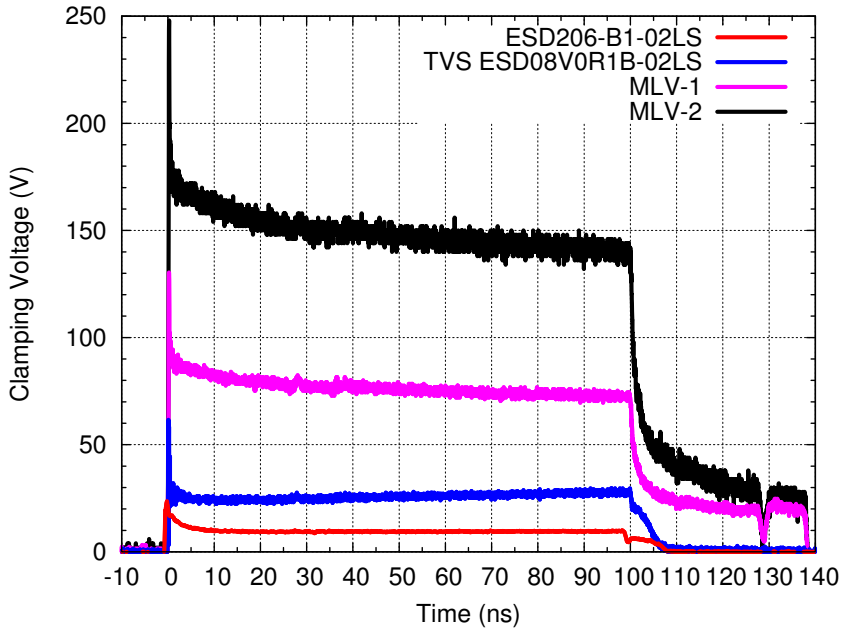


Figure 30: Clamping voltage comparison at 16 A TLP current. TLP-parameter: 50 Ω, 100 ns pulse width, 290 ps rise time. Scope: Tektronix TDS6124C, 12.5 GHz bandwidth, 40 GS/s sampling rate.

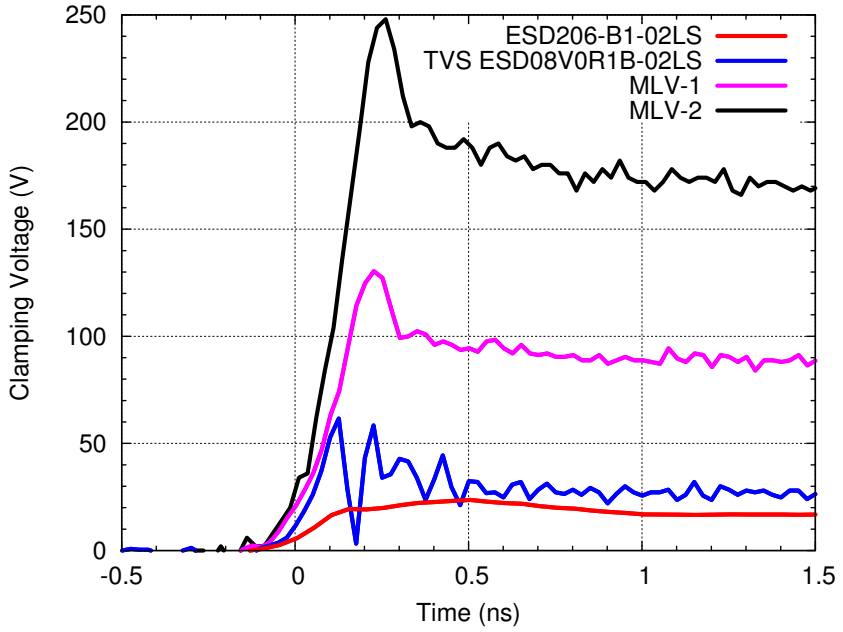


Figure 31: Turn-on comparison at 16 A TLP current. TLP-parameter: 50 Ω, 100 ns pulse width, 290 ps rise time. Scope: Tektronix TDS6124C, 12.5 GHz bandwidth, 40 GS/s sampling rate.

3.4 Spot Leakage Drift

Fig. 32 shows the DC spot leakage drift at 5 V reverse working voltage during a single TLP sweep up to >25 A. MLV-1 and MLV-2 show significant drift in leakage current. The TVS diode has extremely low leakage and zero drift.

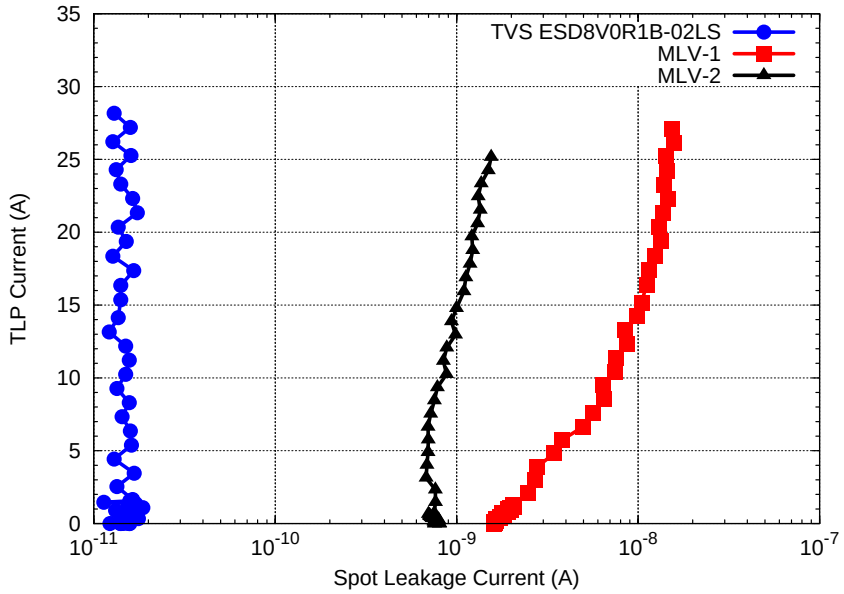


Figure 32: DC spot leakage drift at 5 V reverse working voltage. TLP-parameter: 50 Ω, 100 ns pulse width, 290 ps rise time.

3.5 Breakdown Voltage Drift

Fig. 33 shows the breakdown voltage drift at 1 mA force current during a single TLP sweep up to >25 A. MLV-2 has slight drift. ML-1 has significant drift. TVS shows zero drift which means no pulse-to-pulse degradation.

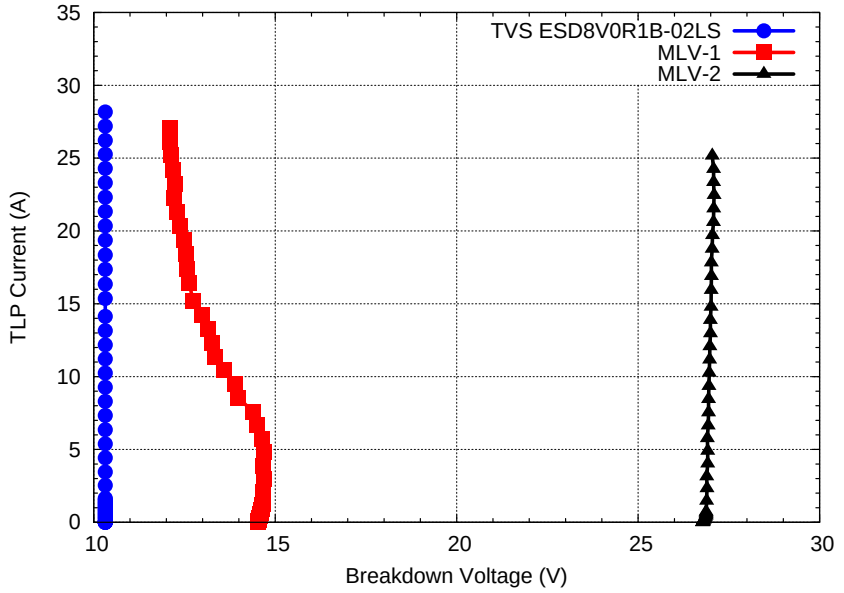


Figure 33: Breakdown voltage drift at 1 mA force current. TLP-parameter: 50 Ω, 100 ns pulse width, 290 ps rise time.

3.6 Degradation due to Multi-Pulse Stress

In this test the device is stressed with multiple pulses at a certain current level: 100 pulses at about 5 A, 100 pulses at about 10 A, and so on, up to about 25 A to 30 A . The spot leakage drift is recorded for each stress pulse. In the first experiment the DC leakage current at 5 V reverse working voltage is recorded and in the second experiment the breakdown voltage drift at 1 mA force current is recorded using a fresh device. Each group of dots is representing 100 pulses. In total each device is stressed with about 500 to 600 pulses up to >25 A.

3.6.1 Spot Leakage Drift

Fig. 34 shows the multi-pulse DC spot leakage current drift at 5 V reverse working voltage. MLV-1 shows extremely high drift and was destroyed at 25 A and about 100 pulses. MLV-2 shows significant multi-pulse drift. The TVS is extremely stable and shows no multi-pulse degradation. The variation is due to the measurement limits of the source meter at low currents (noise).

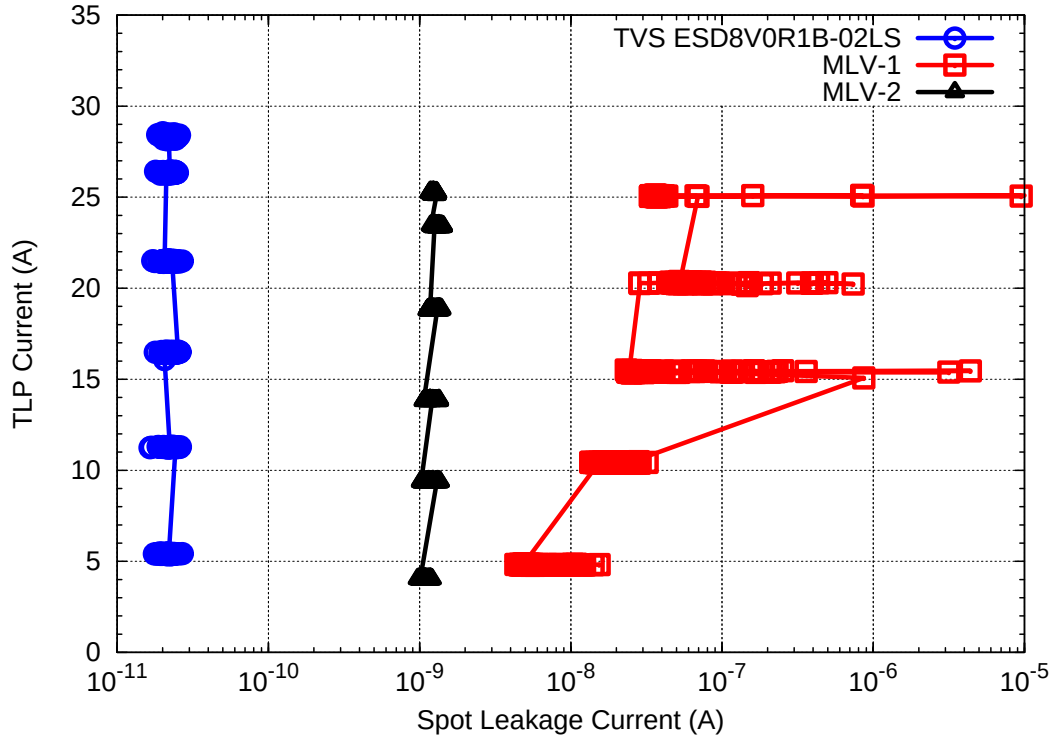


Figure 34: Multi-pulse DC spot leakage current drift at 5 V reverse working voltage. TLP-parameter: 50 Ω, 100 ns pulse width, 1 ns rise time.

3.6.2 Breakdown Voltage Drift

Fig. 35 shows the multi-pulse breakdown voltage drift at 1 mA force current. MLV-1 and MLV-2 show significant multi-pulse degradation. The TVS has zero drift in breakdown voltage at each group of 100 stress pulses up to >25 A (total 600 stress pulses).

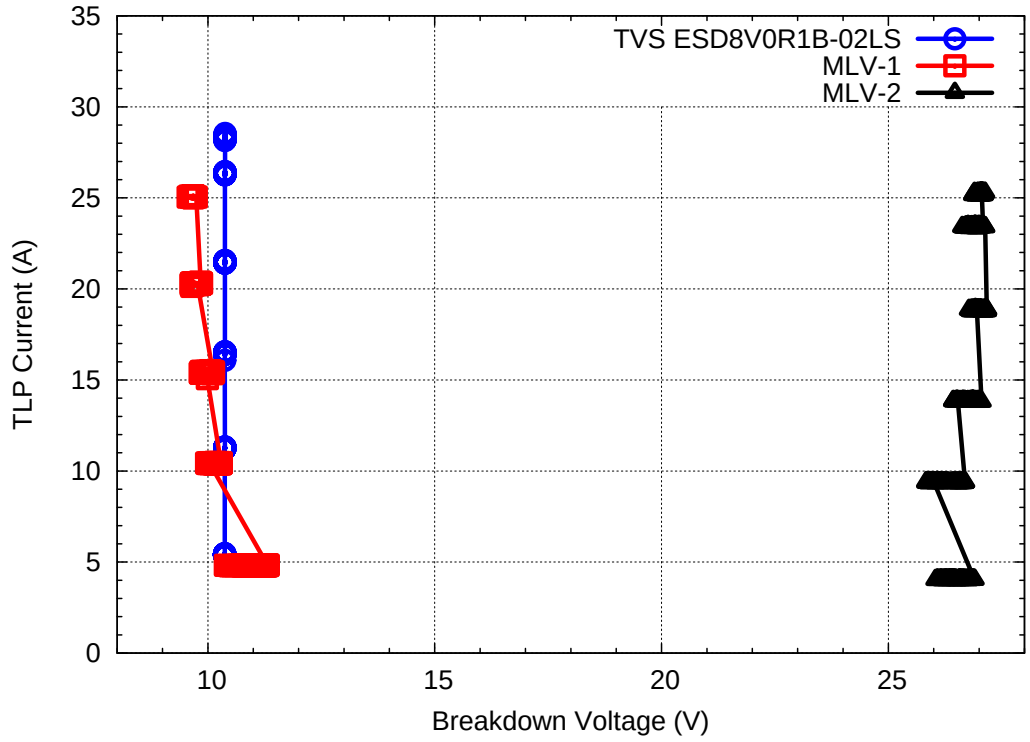


Figure 35: Multi-pulse breakdown voltage drift at 1 mA force current. TLP-parameter: 50 Ω, 100 ns pulse width, 1 ns rise time.

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