

Product Overview

The TQP7M9105 is a high linearity, high gain 1 W driver amplifier in industry standard, RoHS compliant, SOT-89 surface mount package. This InGaP/GaAs HBT delivers high performance across 0.05 to 1.5 GHz while achieving +47 dBm OIP3 and +30 dBm P1dB at 940 MHz while only consuming 220 mA quiescent current. All devices are 100% RF and DC tested.

The TQP7M9105 incorporates on-chip features that differentiate it from other products in the market. The amplifier has a dynamic active bias circuit that enable stable operation over bias and temperature variations and can provide a high linearity at back-off operation

The TQP7M9105 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device an excellent candidate for transceiver line cards and high power amplifiers in current and next generation multi-carrier 3G/4G base stations.

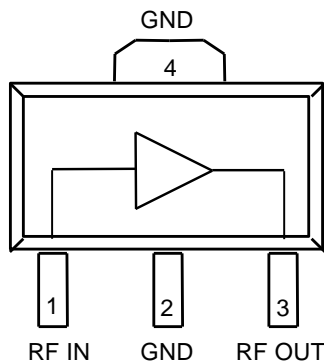


3-pin SOT-89 Package

Key Features

- 50 – 1500 MHz
- +30 dBm P1dB at 940 MHz
- +47 dBm Output IP3 at 940 MHz
- 19.5 dB Gain at 940 MHz
- +5 V Single Supply, 220 mA Current
- Internal RF Overdrive Protection
- Internal DC Overvoltage Protection
- On Chip ESD Protection
- SOT-89 Package

Functional Block Diagram



Top View

Applications

- Repeaters
- BTS Transceivers
- BTS High Power Amplifiers
- CDMA / WCDMA / LTE
- General Purpose Wireless
- ISM Equipment

Ordering Information

| Part No. | Description |
|------------------|------------------------------|
| TQP7M9105 | 1 W High Linearity Amplifier |
| TQP7M9105-PCB900 | 920–960 MHz Evaluation Board |

Standard T/R size = 1000 pieces on a 7" reel

Absolute Maximum Ratings

| Parameter | Rating |
|------------------------------------|---------------|
| Storage Temperature | -65 to 150 °C |
| RF Input Power, CW, 50 Ω, T=+25 °C | +30 dBm |
| Device Voltage (V _{CC}) | +8 V |

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|--|-----|------|-------|-------|
| Device Voltage (V _{CC}) | | +5.0 | +5.25 | V |
| T _{CASE} | -40 | | +105 | °C |
| T _j for >10 ⁶ hours MTTF | | | +170 | °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

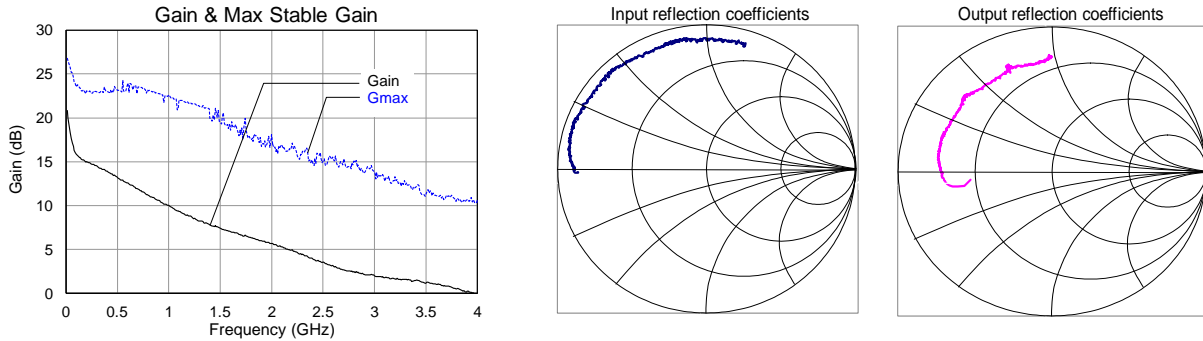
Test conditions unless otherwise noted: V_{CC} = +5.0 V, Temp= +25 °C

| Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------------|---|-------|-------|------|-------|
| Operational Frequency Range | | 50 | | 1500 | MHz |
| Test Frequency | | | 940 | | MHz |
| Gain | | 17.5 | 19.4 | 20.5 | dB |
| Input Return Loss | | | 14 | | dB |
| Output Return Loss | | | 15 | | dB |
| Output P1dB | | +28.7 | +30 | | dBm |
| Output IP3 | P _{out} = +15 dBm/tone, Δf = 1 MHz | +43.5 | +47 | | dBm |
| WCDMA Output Power | -50 dBc ACLR ⁽¹⁾ | | +20.5 | | dBm |
| Noise Figure | | | 6.3 | | dB |
| Quiescent Current, I _{CC} | | 195 | 220 | 245 | mA |
| Thermal Resistance, θ _{jc} | Module (junction to case) | | 27.3 | | °C/W |

Notes:

ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

Device Characterization Data



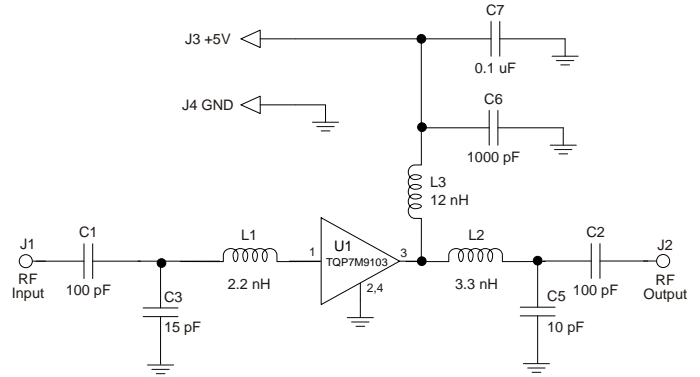
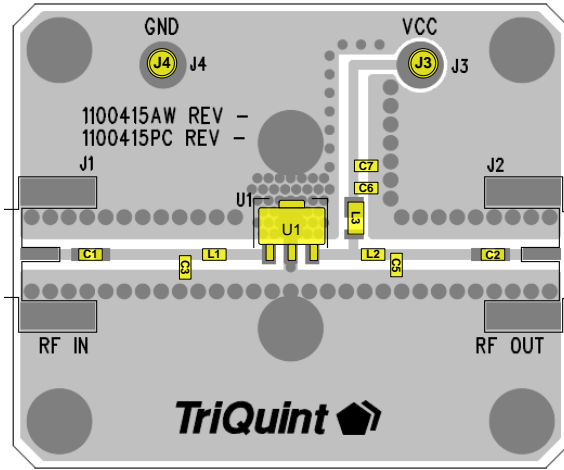
Note: The gain for the unmatched device in 50 ohm system is shown as the trace in black color, [gain (S(21))]. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown as the blue trace [Gmax]. The impedance plots are shown from 0.01– 4 GHz.

S-Parameters

Test Conditions: $V_{CC}=+5$ V, $I_{CQ}=220$ mA, $T=+25^{\circ}$ C, unmatched 50 ohm system, calibrated to device leads

| Freq (GHz) | S11 (dB) | S11 (ang) | S21 (dB) | S21 (ang) | S12 (dB) | S12 (ang) | S22 (dB) | S22 (ang) |
|------------|----------|-----------|----------|-----------|----------|-----------|----------|-----------|
| 0.05 | -1.06 | -178.68 | 17.88 | 154.59 | -36.95 | 1.89 | -3.39 | -171.92 |
| 0.1 | -1.08 | -179.98 | 16.04 | 154.96 | -37.20 | 3.77 | -3.00 | -176.29 |
| 0.2 | -1.01 | 179.18 | 15.20 | 150.91 | -37.52 | 7.85 | -2.91 | -179.66 |
| 0.4 | -0.75 | 176.01 | 14.04 | 134.55 | -36.48 | 11.27 | -2.73 | 176.91 |
| 0.6 | -0.57 | 171.34 | 12.73 | 120.33 | -35.65 | 11.92 | -2.52 | 173.48 |
| 0.8 | -0.51 | 166.55 | 11.29 | 108.35 | -35.14 | 9.35 | -2.51 | 169.15 |
| 1.0 | -0.51 | 163.55 | 10.11 | 98.59 | -34.89 | 11.74 | -2.50 | 165.78 |
| 1.2 | -0.54 | 161.26 | 8.87 | 90.63 | -34.56 | 11.00 | -2.52 | 163.07 |
| 1.4 | -0.57 | 157.96 | 7.85 | 82.50 | -34.07 | 10.99 | -2.61 | 160.70 |
| 1.6 | -0.62 | 154.88 | 7.10 | 75.78 | -33.47 | 10.29 | -2.57 | 158.17 |
| 1.8 | -0.66 | 150.04 | 6.35 | 67.47 | -33.19 | 11.13 | -2.66 | 155.39 |
| 2.0 | -0.60 | 144.26 | 5.75 | 59.82 | -32.84 | 4.95 | -2.64 | 151.03 |
| 2.2 | -0.56 | 139.27 | 4.95 | 51.93 | -32.47 | 3.98 | -2.59 | 146.61 |
| 2.4 | -0.75 | 135.92 | 3.91 | 45.80 | -32.62 | 1.55 | -2.57 | 141.55 |
| 2.6 | -0.58 | 132.79 | 3.16 | 40.57 | -32.36 | 2.07 | -2.28 | 139.39 |
| 2.8 | -0.55 | 132.30 | 2.52 | 36.55 | -32.25 | 2.62 | -2.33 | 138.20 |
| 3.0 | -0.64 | 129.89 | 2.01 | 31.75 | -31.94 | 0.51 | -2.37 | 136.78 |
| 3.2 | -0.69 | 126.19 | 1.69 | 26.65 | -31.44 | 1.40 | -2.40 | 135.83 |
| 3.4 | -0.84 | 121.41 | 1.48 | 20.86 | -30.84 | -2.57 | -2.54 | 133.06 |
| 3.6 | -0.93 | 115.44 | 1.06 | 12.97 | -30.84 | -4.71 | -2.68 | 126.60 |
| 3.8 | -0.85 | 110.18 | 0.51 | 5.81 | -30.20 | -10.30 | -2.63 | 119.65 |
| 4.0 | -0.80 | 106.76 | -0.04 | -0.51 | -30.40 | -11.85 | -2.51 | 114.02 |

Evaluation Board 615 – 655 MHz Reference Design



Notes:

1. Components shown on the silkscreen but not on the schematic are not used.
2. 0 Ω resistor can be replaced with copper trace in the target application layout.
3. All components are of 0603 size unless stated on the schematic.
4. The recommended component values are dependent upon the frequency of operation.
5. Critical component placement locations:
 - Distance between U1 Pin 1 Pad left edge to L1 (right edge): 100 mil
 - Distance between U1 Pin 1 Pad left edge to C3 (right edge): 200 mil
 - Distance between U1 Pin 3 Pad right edge to C5 (left edge): 210 mil
 - Distance between U1 Pin 3 Pad right edge to L2 (left edge): 120 mil

Bill of Material 615 – 655 MHz

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|---------|--------------------------------|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | |
| U1 | n/a | 1 W High Linearity Amplifier | Qorvo | TQP7M9105 |
| C3 | 15 pF | CAP, 0603, ± 0.05 pF, 50V, NPO | AVX | 06032U150J |
| C5 | 10 pF | CAP, 0603, ± 0.05 pF, 50V, NPO | AVX | 06032U100J |
| C1, C2 | 100 pF | CAP, 0603, 5%, 50V, NPO/COG | various | |
| C6 | 1000 pF | CAP, chip | various | |
| C7 | 0.1 uF | CAP, 0603, 10%, X5R , 10V | various | |
| L1 | 2.2 nH | IND, 0603, +/-0.3nH | TOKO | LL1608-FSL2N2S |
| L2 | 3.3 nH | IND, 0603, +/-0.3nH | TOKO | LL1608-FSL3N3S |
| L3 | 12 nH | IND, 0805, 5%, Wirewound | Coilcraft | 0805CS-120XJL |

Typical Performance 615 – 655 MHz

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 235\text{ mA}$, Temp. = $+25\text{ }^\circ\text{C}$

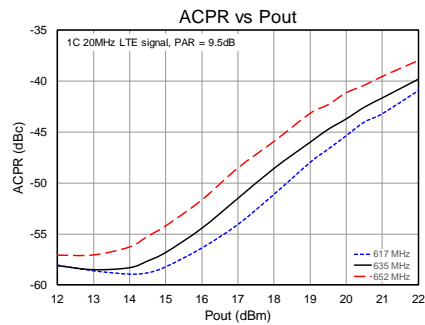
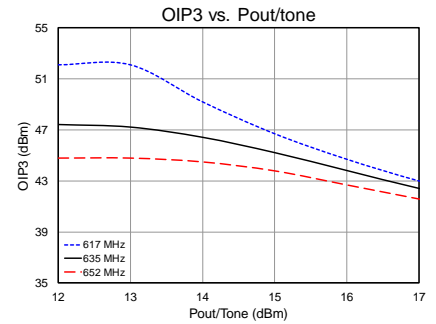
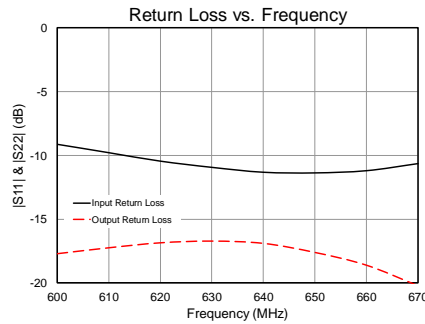
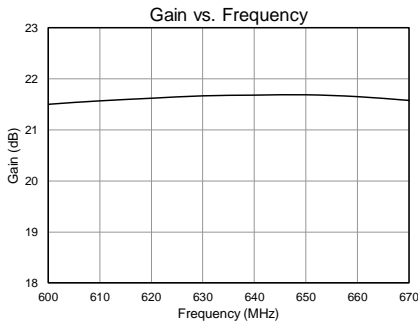
| Parameter | Conditions | Typical Value | | | Units |
|------------------------------------|--|---------------|-------|-------|-------|
| Frequency | | 617 | 635 | 652 | MHz |
| Gain | | 21.6 | 21.6 | 21.6 | dB |
| Input Return Loss | | 10.5 | 11 | 11 | dB |
| Output Return Loss | | 17 | 16.5 | 17.5 | dB |
| Output P1dB | | +30.3 | +30.5 | +30.8 | dBm |
| OIP3 | $P_{out} = +16\text{ dBm}$ / tone, $\Delta f = 1\text{ MHz}$ | +44.7 | +43.8 | +42.7 | dBm |
| WCDMA Channel Power ⁽¹⁾ | ACLR = -50 dBc | +18 | +17.5 | +16.8 | dBm |

Notes:

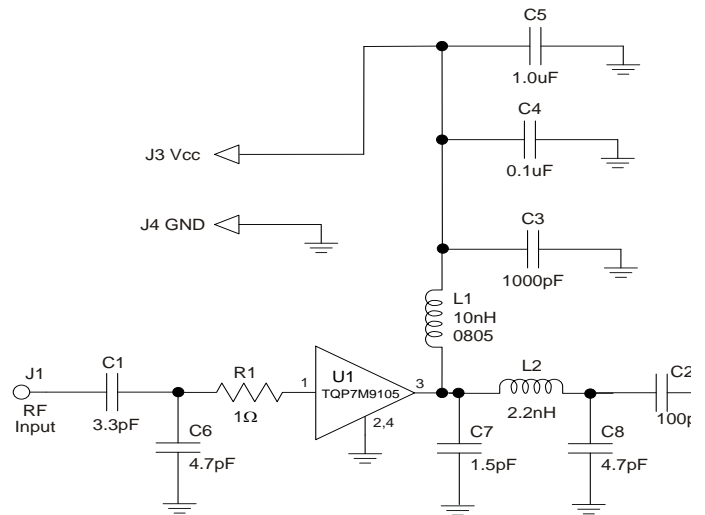
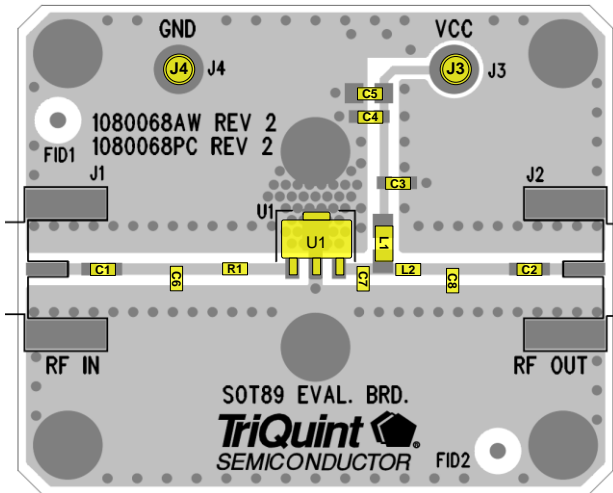
- 1C 20MHz LTE signal, PAR=9.5dB

Performance Plots 615 – 655 MHz

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 235\text{ mA}$, Temp. = $+25\text{ }^\circ\text{C}$



Evaluation Board – TQP7M9105-PCB900 (860 – 960 MHz)



Notes:

- See Evaluation Board PCB Information section for PCB material and stack-up.
- Components shown on the silkscreen but not on the schematic are not used.
- The recommended component values are dependent upon the frequency of operation.
- All components are of 0603 size unless stated on the schematic.
- Critical component placement locations:
 Distance from U1 Pin 1 Pad (left edge) to R1 (right edge): 100 Mils (4.85° at 940 MHz)
 Distance from U1 Pin 1 Pad (left edge) to C6 (right edge): 270 Mils (13.1° at 940 MHz)
 Distance from U1 Pin 3 Pad (right edge) to C7 (left edge): 40 Mils (1.94° at 940 MHz)
 Distance from U1 Pin 3 Pad (right edge) to L2 (left edge): 120 Mils (5.82° at 940 MHz)
 • Distance from U1 Pin 3 Pad (right edge) to C8 (left edge): 260 Mils (12.6° at 940 MHz)

Bill of Material TQP7M9105-PCB900

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|---------|--|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | |
| U1 | n/a | TQP7M9105 Amplifier, SOT-89 pkg. | Qorvo | |
| C1 | 3.3 pF | Cap., Chip, 0603, ±0.1 pF, 50 V, Accu-P | AVX | 06035J3R3ABSTR |
| C2 | 100 pF | Cap., Chip, 0603, 5%, 50 V, NPO/COG | various | |
| C3 | 1000 pF | Cap., Chip, 0603, 5%, 50 V, NPO/COG | various | |
| C4 | 0.1 μF | Cap., Chip, 0603, 10%, 16 V, X7R | various | |
| C5 | 1.0 μF | Cap., Chip, 0603, 10%, 10 V, X5R | various | |
| C7 | 1.5 pF | Cap., Chip, 0603, ±0.05 pF, 50 V, Accu-P | AVX | 06035J1R5ABSTR |
| C6, C8 | 4.7 pF | Cap., Chip, 0603, ±0.05 pF, 50 V, Accu-P | AVX | 06035J4R7ABSTR |
| L1 | 10 nH | Inductor, 0805, 5%, Coilcraft CS Series | Coilcraft | 0805CS-100XJLB |
| L2 | 2.2 nH | Inductor, 0603, ±0.3 nH | Toko | LL1608-FSL2N2S |
| R1 | 1 Ω | Resistor, Chip, 0603, 5%, 1/16 W | various | |

Typical Performance 860 – 960 MHz (TQP7M9105-PCB900)

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 220\text{ mA}$, Temp. = $+25\text{ }^\circ\text{C}$

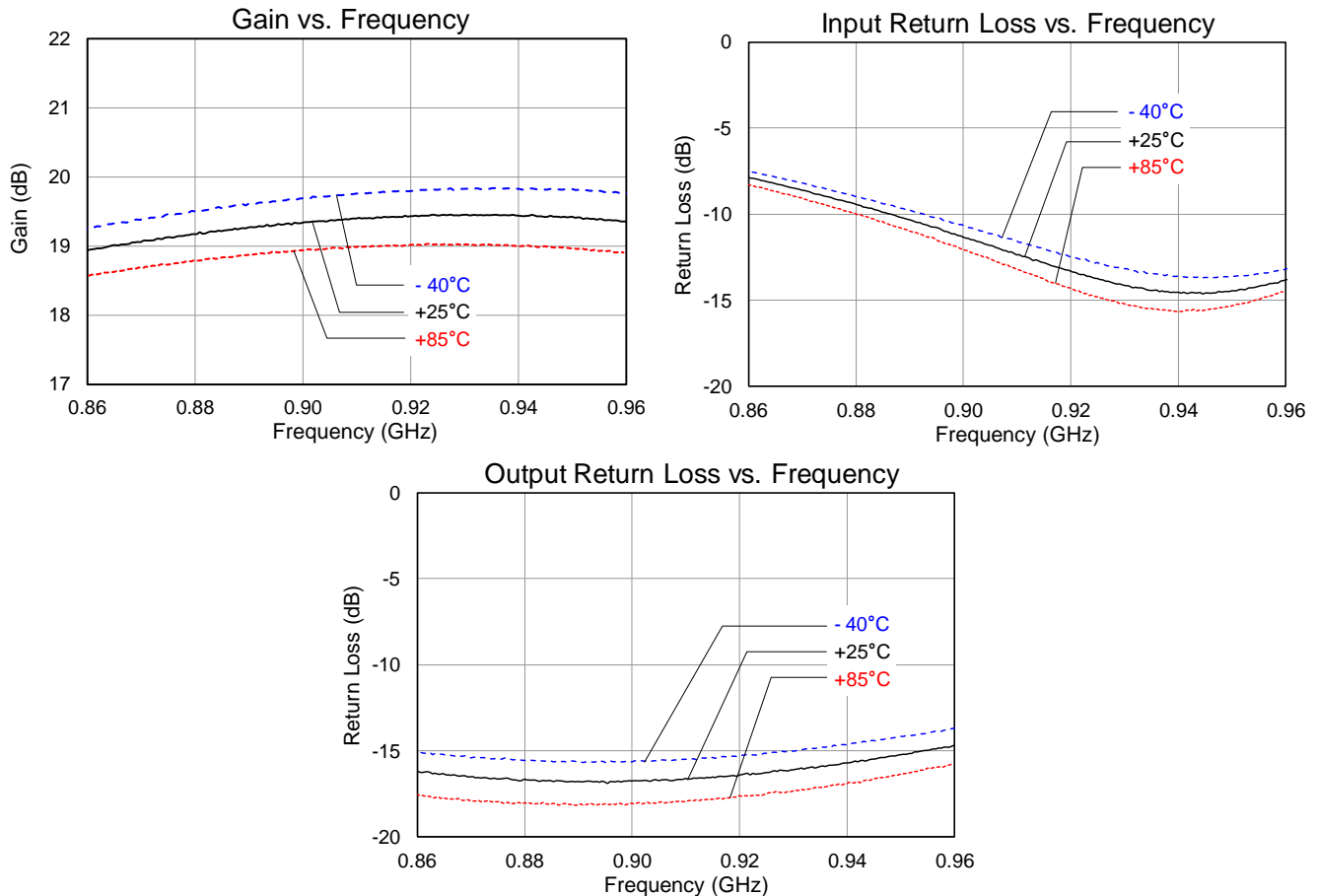
| Parameter | Typical Value | | | | | | Units |
|--------------------------------------|---------------|-------|-------|-------|-------|-------|-------|
| Frequency | 860 | 880 | 900 | 920 | 940 | 960 | MHz |
| Gain | 18.9 | 19.2 | 19.3 | 19.4 | 19.4 | 19.3 | dB |
| Input Return Loss | 7.9 | 9.5 | 11.3 | 13 | 14 | 13 | dB |
| Output Return Loss | 16.2 | 16.7 | 16.8 | 15 | 15 | 14 | dB |
| Output P1dB | +29 | +29.2 | +29.5 | +29.9 | +30.0 | +29.8 | dBm |
| Output IP3 ⁽¹⁾ | +48 | +50.2 | +50.6 | +49.5 | +49.2 | +49 | dBm |
| WCDMA Channel Power ^(2,3) | 20 | 20.2 | 20.5 | +20.5 | +20.5 | +20.5 | dBm |
| Noise figure | 6.8 | 6.6 | 6.4 | 6.4 | 6.4 | 6.3 | dB |

Notes:

- +15 dBm/tone, $\Delta f = 1\text{ MHz}$
- At -50 dBc ACLR
- 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

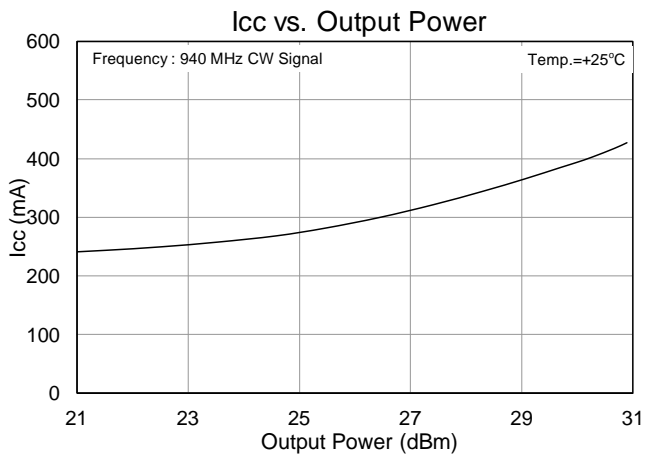
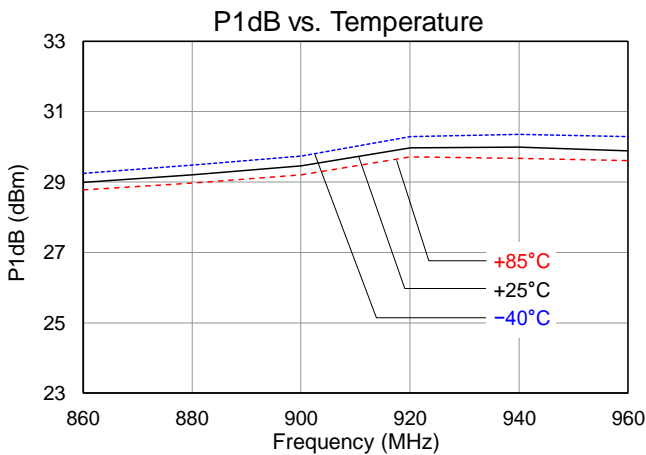
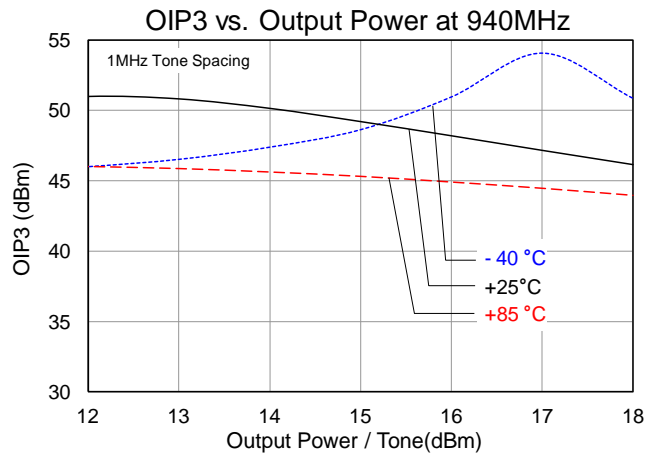
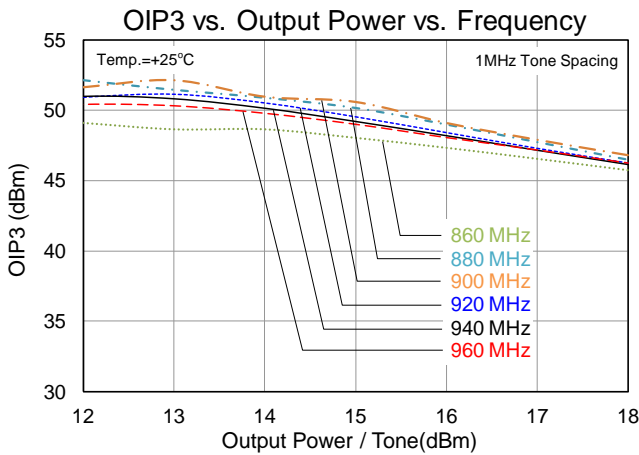
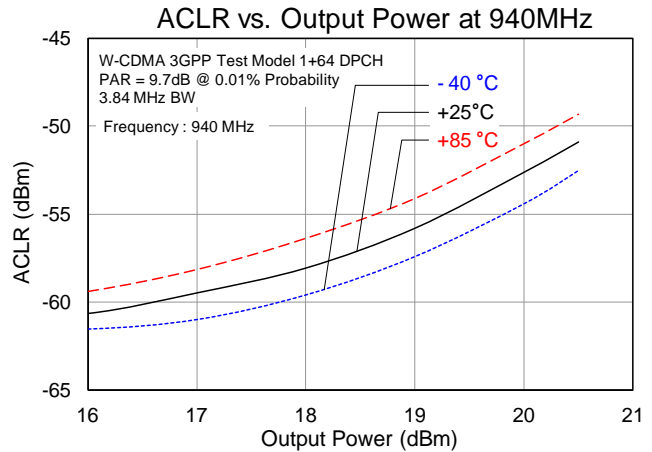
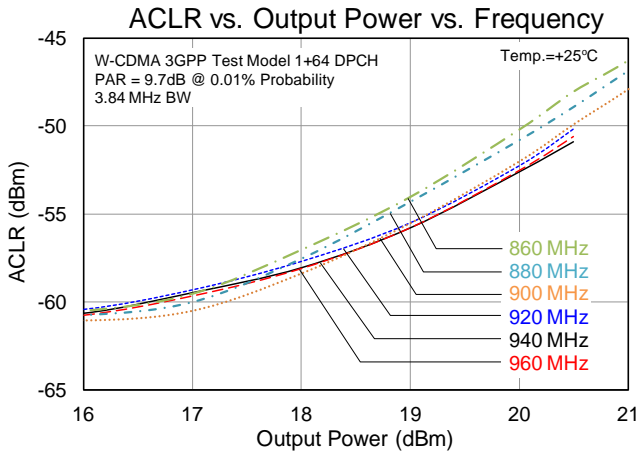
RF Performance Plots 860 – 960 MHz (TQP7M9105-PCB900)

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 235\text{ mA}$, Temp. = $+25\text{ }^\circ\text{C}$

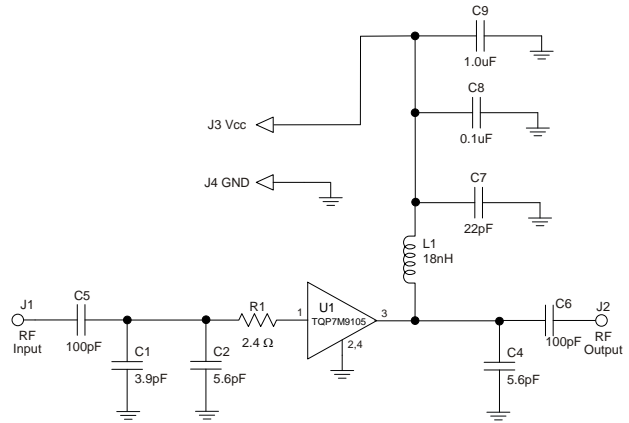
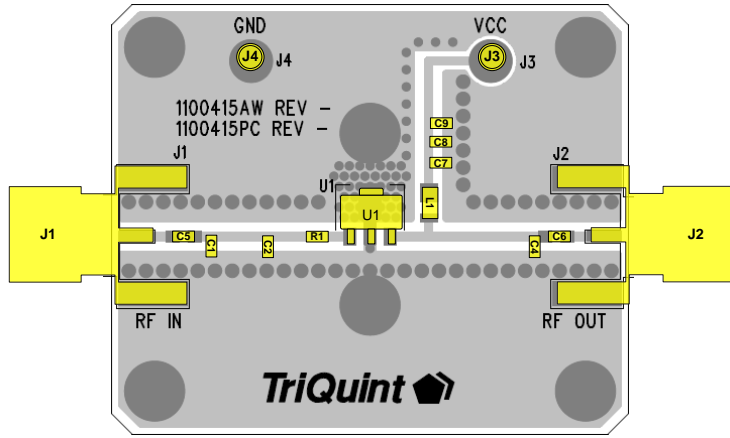


Performance Plots 860 – 960 MHz (TQP7M9105-PCB900)

Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CC} = 235\text{ mA}$, $Temp. = +25\text{ }^\circ\text{C}$



Evaluation Board 700 – 1000 MHz Reference Design



Notes:

6. Components shown on the silkscreen but not on the schematic are not used.
7. All components are of 0603 size unless stated on the schematic.
8. The recommended component values are dependent upon the frequency of operation.
9. Critical component placement locations:
 - Distance between U1 Pin 1 Pad to R1 (right edge): 45 mil
 - Distance between U1 Pin 1 Pad to C1 (right edge): 370 mil
 - Distance between U1 Pin 1 Pad to C2 (right edge): 195 mil
 - Distance between U1 Pin 3 Pad to C4 (left edge): 395 mil

Bill of Material 700 – 1000 MHz

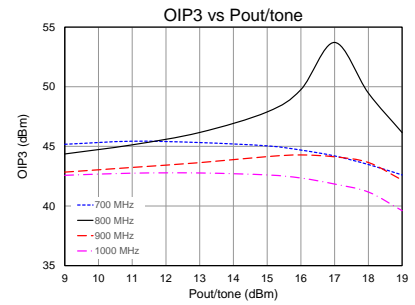
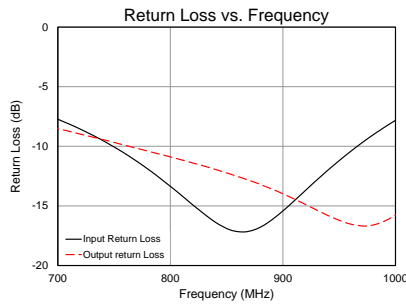
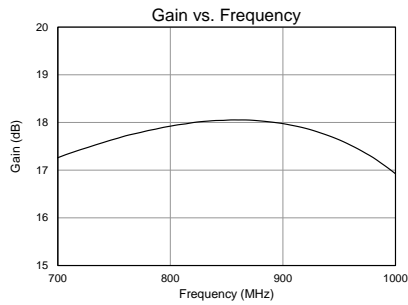
| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|--------|------------------------------------|-----------|----------------|
| n/a | n/a | Printed Circuit Board | Qorvo | 1100415 |
| U1 | n/a | 1 W High Linearity Amplifier | Qorvo | TQP7M9105 |
| C1 | 3.9 pF | CAP, 0603, ± 0.1 pF, 100V, NPO/COG | AVX | 06035J3R9ABSTR |
| C2, C4 | 5.6 pF | CAP, 0603, ± 0.1 pF, 100V, NPO/COG | AVX | 06035J5R6ABSTR |
| C5, C6 | 100 pF | CAP, 0603, 5%, 50V, NPO/COG | various | |
| C7 | 22 pF | CAP, 0603, 5%, 50V, NPO/COG | Various | |
| C8 | 0.1 uF | CAP, 0603, 5%, 50V, NPO/COG | various | |
| C9 | 1.0 uF | CAP, 0603, 10%, X5R , 10V | various | |
| R1 | 2.4 Ω | RES, 0603, 5%, 1/16W, Chip | various | |
| L1 | 18 nH | IND, 0805, 5%, Ceramic | Coilcraft | 0805CS-180XJL |

Typical Performance 700 – 1000 MHz

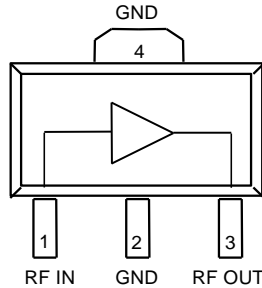
Test Conditions: $V_{CC}=+5\text{ V}$, $Temp.=+25^{\circ}\text{C}$, 50Ω System

| Parameter | Conditions | Typical Value | | | | Units |
|---------------------------------------|---|---------------|-------|-------|-------|-------|
| | | 700 | 800 | 900 | 1000 | |
| Frequency | | 700 | 800 | 900 | 1000 | MHz |
| Gain | | 17.2 | 17.9 | 18 | 16.9 | dB |
| Input Return Loss | | 7.7 | 13.3 | 15.3 | 7.8 | dB |
| Output Return Loss | | 8.5 | 10.9 | 14 | 15.7 | dB |
| Output P1dB | | +28.5 | +29.5 | +30.5 | +30.5 | dBm |
| Output IP3 | $P_{out}= +15\text{ dBm/tone}$, $\Delta f= 1\text{ MHz}$ | +45 | +47 | +44 | +42.6 | dBm |
| Quiescent Collector Current, I_{CQ} | | 225 | | | | mA |

Performance Plots 700 – 1000 MHz



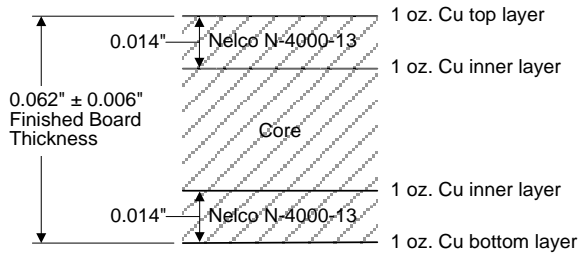
Pin Configuration and Description



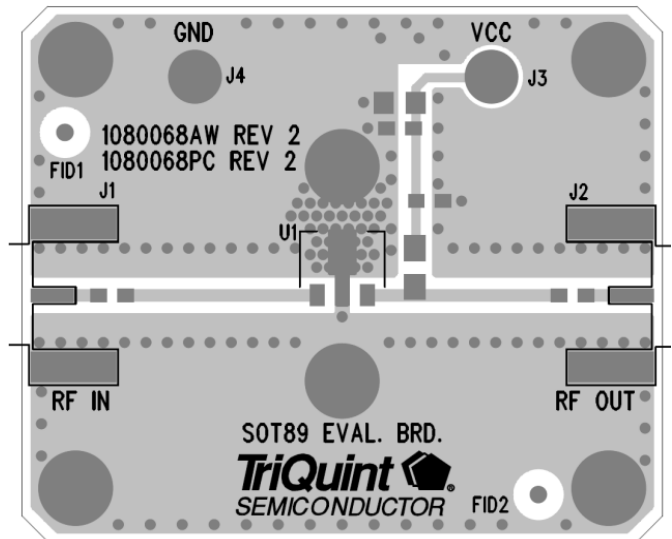
| Pin No. | Label | Description |
|---------|--------|--|
| 1 | RF IN | RF Input. Requires external match for optimal performance. External DC Block required. |
| 2, 4 | GND | RF/DC Ground Connection |
| 3 | RF OUT | RF Output and V _{CC} . Requires external match for optimal performance. External DC Block, RF chock and supply voltage is required. |

Evaluation Board PCB Information

Qorvo PCB 1080068 Material and Stack-up



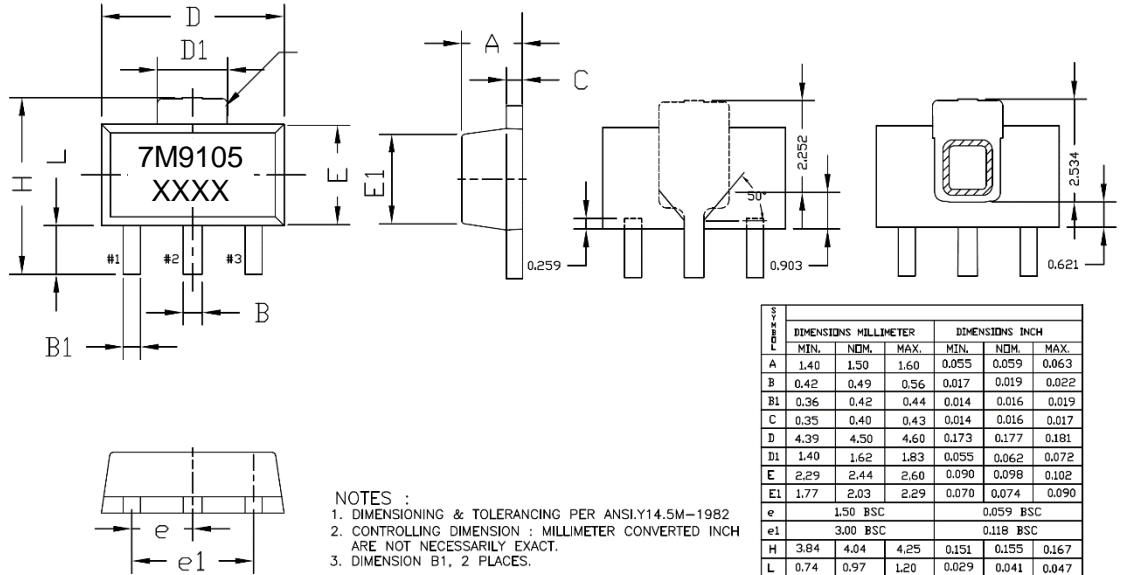
50 ohm line dimensions: width = .028", spacing = .028".



Package Marking and Dimensions

Marking:

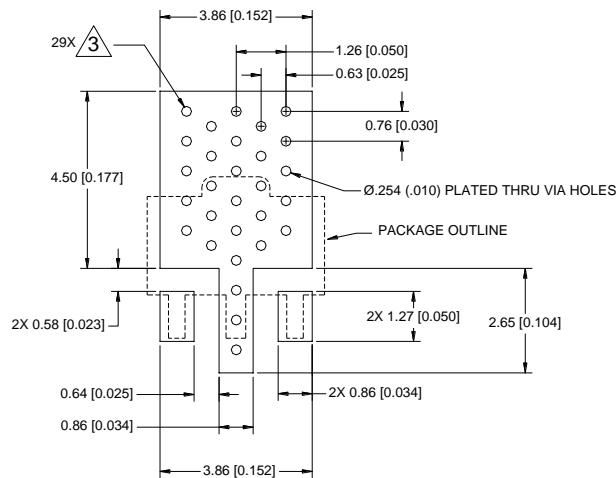
Part Number – 7M9105
Trace Code – XXXX



Notes:

1. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
2. Trace code up to 4 characters assigned by subcontractor
3. Contact plating: Annealed Matte Tin or Nickel Palladium Gold (NiPdAu)

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters [inches]. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

| Parameter | Rating | Standard |
|----------------------------------|---------|--------------------------|
| ESD – Human Body Model (HBM) | 2 | ESDA / JEDEC JS-001-2012 |
| ESD – Charged Device Model (CDM) | C3 | JEDEC JESD22-C101F |
| MSL – Moisture Sensitivity Level | Level 1 | IPC/JEDEC J-STD-020 |



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: Annealed Matte Tin or Nickel Palladium Gold (NiPdAu)

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

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