DESCRIPTION

The MT7832 is a high-PF, non-isolate LED Driver IC. The floating-ground, high-side BUCK topology makes full wave detection possible. The MT7832 works in QRM mode, which improves both of efficiency and EMI performance. Selectable maximum period control is integrated, such that flick can be eliminated while enough demagnetization time is guaranteed.

Various protections such as OVP, OCP, OTP, etc, are embedded to improve reliability. The MT7832 integrate 500V MOSFET internally, which simplifies external circuit.

The driving capability of the MT7832 is designed to be insensitive to VDD voltage and soft, with MAXIC proprietary technique. It can help to improve EMI performance greatly.

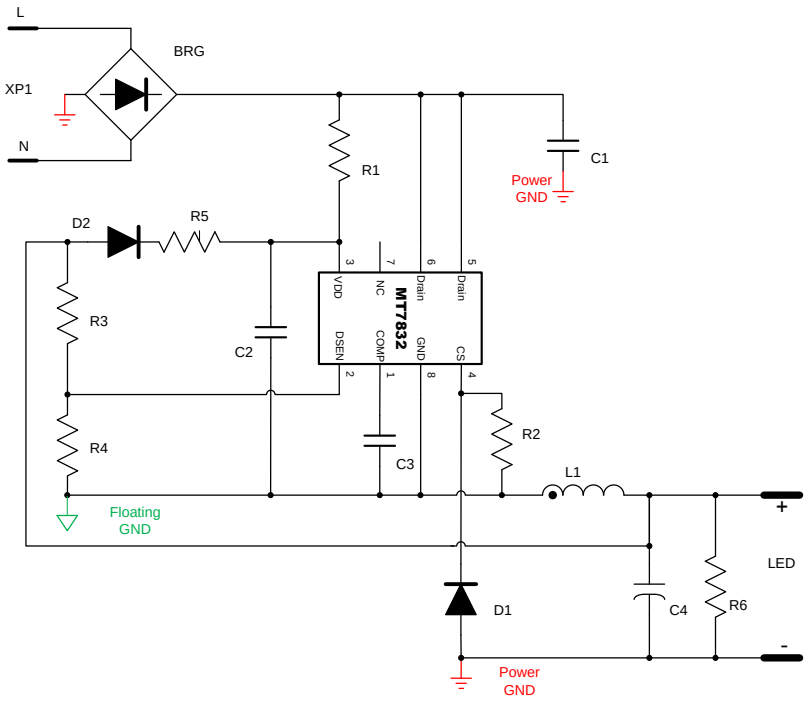
FEATURES

- Single-stage active power factor correction (PFC > 0.90)
- High accurate LED current (+/-3%)
- Good Line and Load Regulation (+/-2%)
- Quasi-Resonant mode (QRM) operation
- Various protection schemes.
- Power-on soft-start
- Compact package: SOP8

APPLICATIONS

- E14/E27/PAR30/PAR38/GU10 LED lamp
- T8/T10 LED tube
- Other LED lighting applications

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

VDD Pin Voltage	-0.3V to VDD Clamp
Drain Pin Voltage	-0.3V to 500V
COMP/CS/DSEN Pins Voltage	-0.3V to 6V
Lead Temperature (soldering, 10 sec.)	260°C
Storage Temperature	-55°C to 150°C

Recommended operating conditions

Supply voltage	9V to 28V
Operating Temperature (Environment)	-40°C to 105°C
Output Power	≤ 9W @ 90VAC~264VAC ≤ 13W @ 176VAC~264VAC

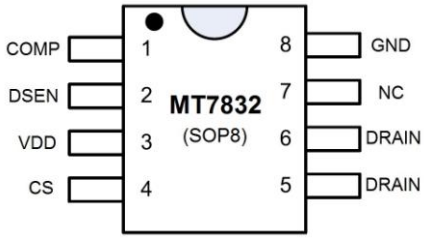
Thermal resistance①

Junction to ambient ($R_{\theta JA}$)	128°C/W

Note:

① *$R_{\theta JA}$ is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" X 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.*

PIN CONFIGURATIONS



PIN DESCRIPTION

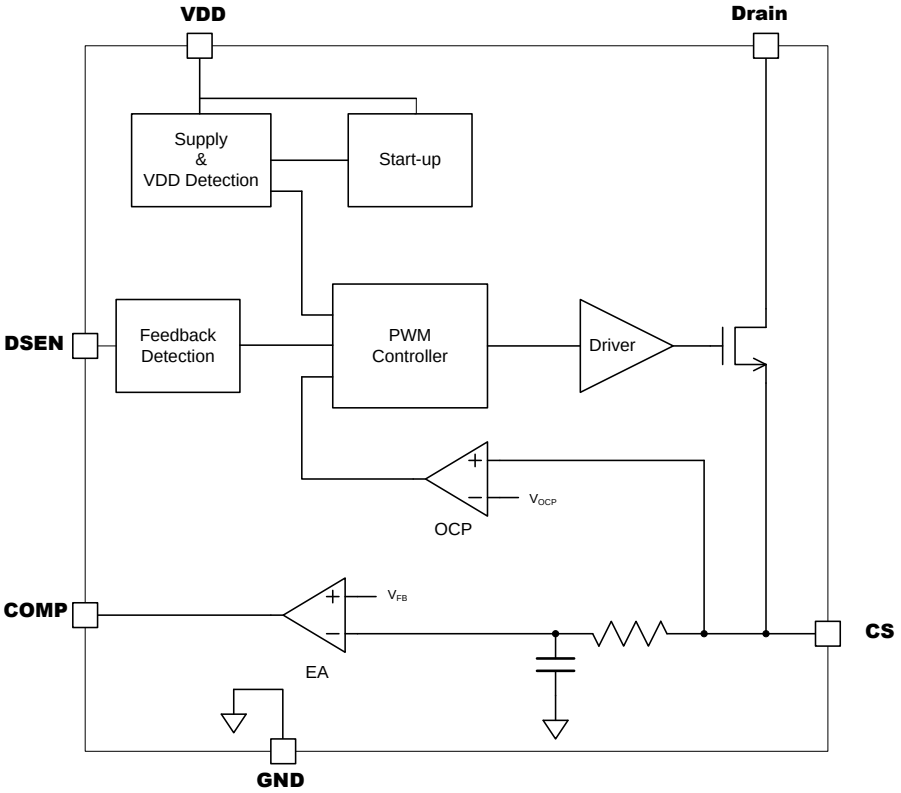
Name	Pin No.	Description
COMP	1	Internal EA's output pin. Connect a capacitor to ground for frequency compensation.
DSEN	2	Feedback pin for inductor zero current crossing detection.
VDD	3	Power Supply pin.
CS	4	Source of internal MOSFET, and Current Sense pin.
DRAIN	5,6	Drain of internal MOSFET.
NC	7	No connection pin.
GND	8	Ground pin.

ELECTRICAL CHARACTERISTICS

(Test conditions: V_{DD}=15V, T_A=25°C unless otherwise stated.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up (VDD Pin)						
V_{STP}	Start-up Voltage	VDD Ramp-up from 0V		18		V
UVLO	Under Voltage Lockout	VDD Ramp-down from (V_{STP}+1V)		9		V
I_{STP}	Start-up Current	VDD=16V		25		μA
OVP1	Over Voltage Protection of VDD			28		V
I_{CLAMP}	Sinking Current Capability to Clamp VDD			5		mA
Power Supply Current						
I_Q	Quiesent Current			1.0		mA
Control Loop						
V_{REF-FB}	Voltage Reference for Feedback Loop	Close the Feedback Loop	196	200	204	mV
SCP	Threshold of Short Circuit Protection at DSEN Pin			400		mV
LEB1	Leading Edge Blank for DSEN Pin			2		uS
MinT	Minimum Switching Period			10		uS
Current Sense Pin						
OCP	Threshold of Over Current Protection at CS Pin			1.4		V
LEB2	Leading Edge Blank for CS Pin			300		nS
Thermal Protection						
OTP	Over Temperature Protection			155		°C
Hys_{-OTP}	Hysteresis of OTP			15		°C
Internal MOSFET						
Ron				5.5		Ω
BV_{DSS}	Breakdown voltage	VGS=0V/I_{DS}=250uA	500			V

BLOCK DIAGRAM



APPLICATION INFORMATION

The MT7832 integrates power factor correction function and works in Quasi-Resonant Mode (QRM). The LED current can be accurately regulated through sensing the inductor current signal.

Averaged Current Control

The MT7832 accurately regulates LED current through sensing the inductor current signal. The LED current can be easily set by:

$$I_{LED} = \frac{V_{FB}}{R_S}$$

Where V_{FB} (=200mV) is the internal reference voltage and R_S is an external current sensing resistor (Rs is the R2 in circuit in page1).

Start Up

During start-up, the capacitor at VDD is charged through the resistor which is connected to main line voltage. The internal control logic starts to work when VDD reaches 18V. The COMP pin is, therefore, pre-charged during this process. The internal control loop is established. Once the voltage of COMP reaches 1.4V, the whole system works in normal operation mode.

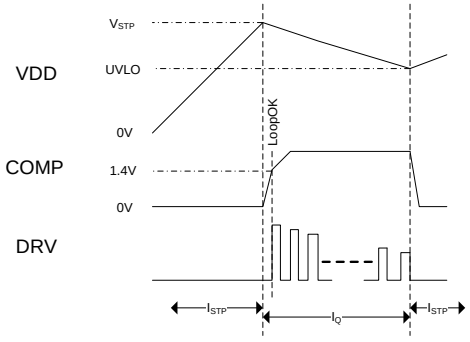


Fig.1 Start up sequence

As the VDD goes below 9V, the system is considered to be UVLO, the PWM signal of DRV goes low， and the voltage of COMP is discharged to 0V. The detailed start-up sequence is shown in Fig. 1.

Auxiliary Sensing

The voltage waveform of the inductor is sensed during PWM OFF period for switching logic control, short-circuit protection (SCP).

The DSEN senses the inductor voltage through a resistor divider. The sampling strobe window is 2us LEB (Leading Edge Blanking) time right after the DRV signal is low for better noise immunity as shown in Fig. 2.

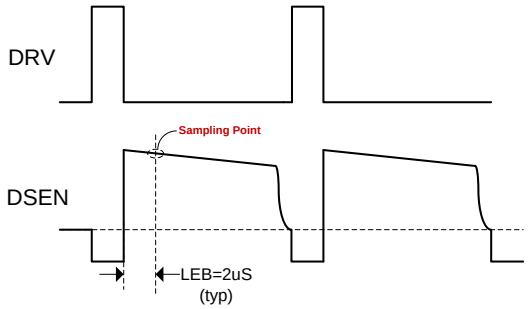


Fig.2 Auxiliary Signal Sensing

Hiccup Mode

Any detected fault conditions, such as, over-voltage (OV), short-circuit (SC) conditions, will force MT7832 into hiccup mode, and PWM signal goes low. VDD is therefore discharged by the MT7832 itself. Then VDD continues to drop below UVLO threshold. A start-up sequence is initiated. If the fault conditions are removed, the LED driver goes back to normal.

The hiccup mode keeps the system at low power dissipation state during fault conditions, enhancing system reliability.

Over-voltage Protection

If VDD exceeds 28V three times, OVP is triggered and so the MT7832 gets in Hiccup mode. It is highly recommended to set up the VDD voltage between 11V and 27V.

Short-circuit Protection

The short-circuit protection is triggered if the DSEN voltage is detected below 400mV during OFF period for a continuous time of 5 to 10ms. The MT7832 gets into hiccup mode.

Over-current Protection

The MT7832 immediately turns off the power MOSFET once the voltage at CS pin exceeds 1.4V. This cycle by cycle current limitation scheme prevents the relevant components, such as power MOSFET, inductor, etc. from damage.

Supporting Wide Output Voltage

In some application, the output voltage range is as wide as more than 2 times, such as 24V ~ 48V; or the output voltage is too high, the application circuit in page 1, VDD pin is directly powered by output terminal through D2 and R5, may cause some issues. Adopting transformer auxiliary winding to power the VDD is a better choice. Refer to Fig.3.

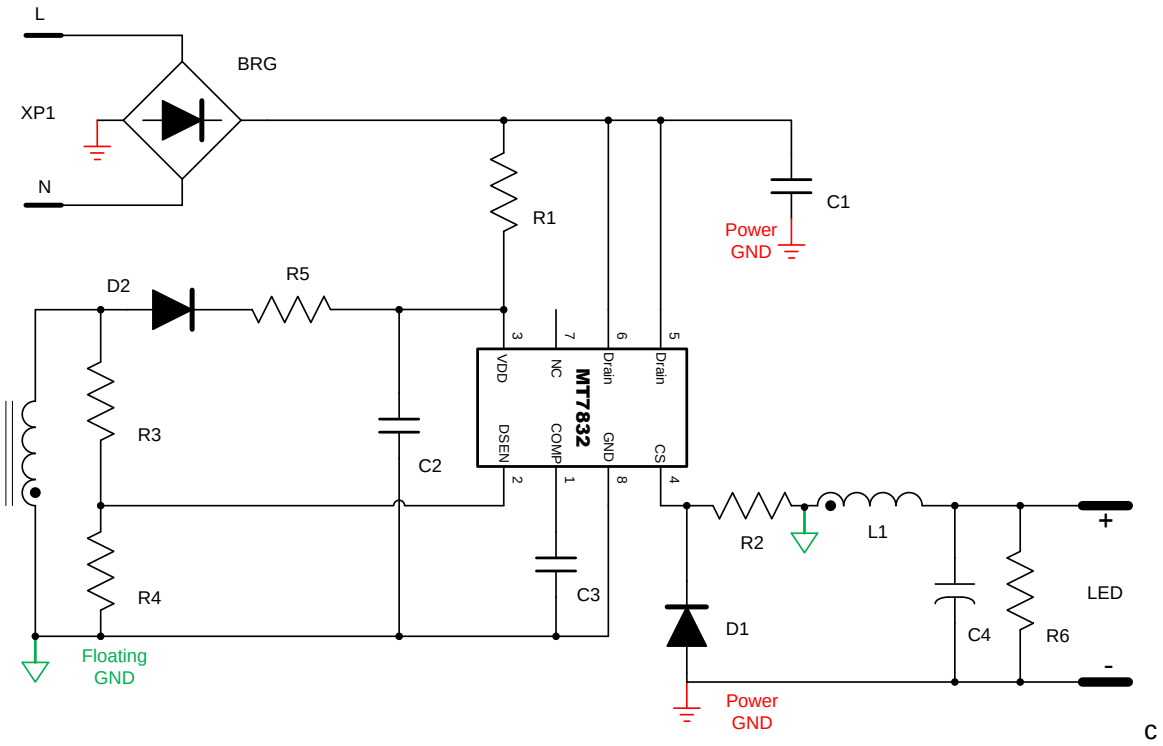
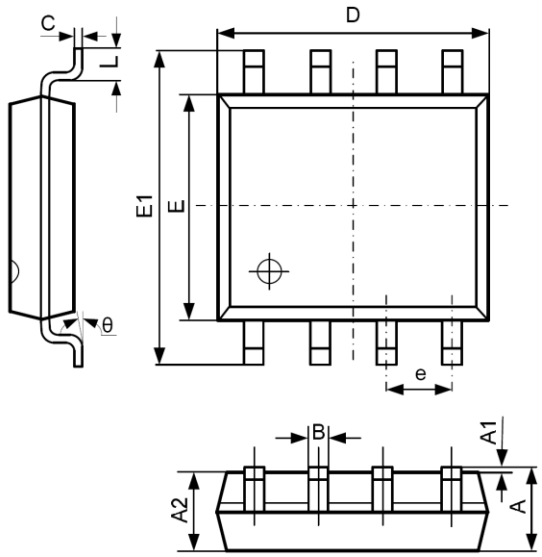


Fig.3 Transformer auxiliary winding to power the VDD

PACKAGE INFORMATION

SOP-8 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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