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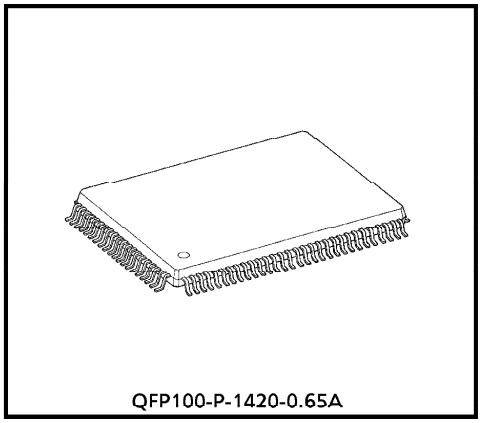
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6A39

COLUMN DRIVER FOR A DOT MATRIX LCD

The T6A39 is an 80-channel-output column driver for an STN dot matrix LCD.
The T6A39 features a 28-V LCD drive voltage and a 4-MHz maximum operating frequency. The T6A39 is able to drive LCD panels with a duty ratio of up to 1/240. It is recommended for use with the T6A40.



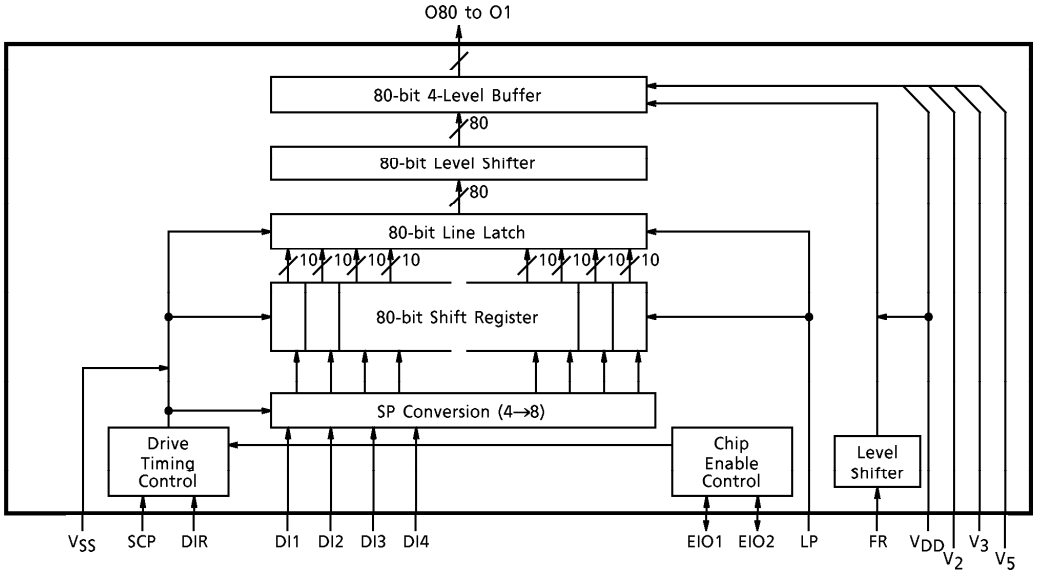
QFP100-P-1420-0.65A

Weight : 1.60g (typ.)

FEATURES

- Display duty application : to 1/240
- LCD drive signal : 80
- Data transfer : 1, 2, 4-bit bidirectional
- Operating frequency : 4 MHz
- LCD drive voltage : 8 to 28V (max 30V)
- Power supply voltage : 4.5 to 5.5V
- Operating temperature : −20 to 75°C
- LCD drive output resistance : 1.5kΩ (max) (12.8V, 1/9 bias)
- Low power consumption : Cascade connection and auto enable transfer functions are available.

BLOCK DIAGRAM



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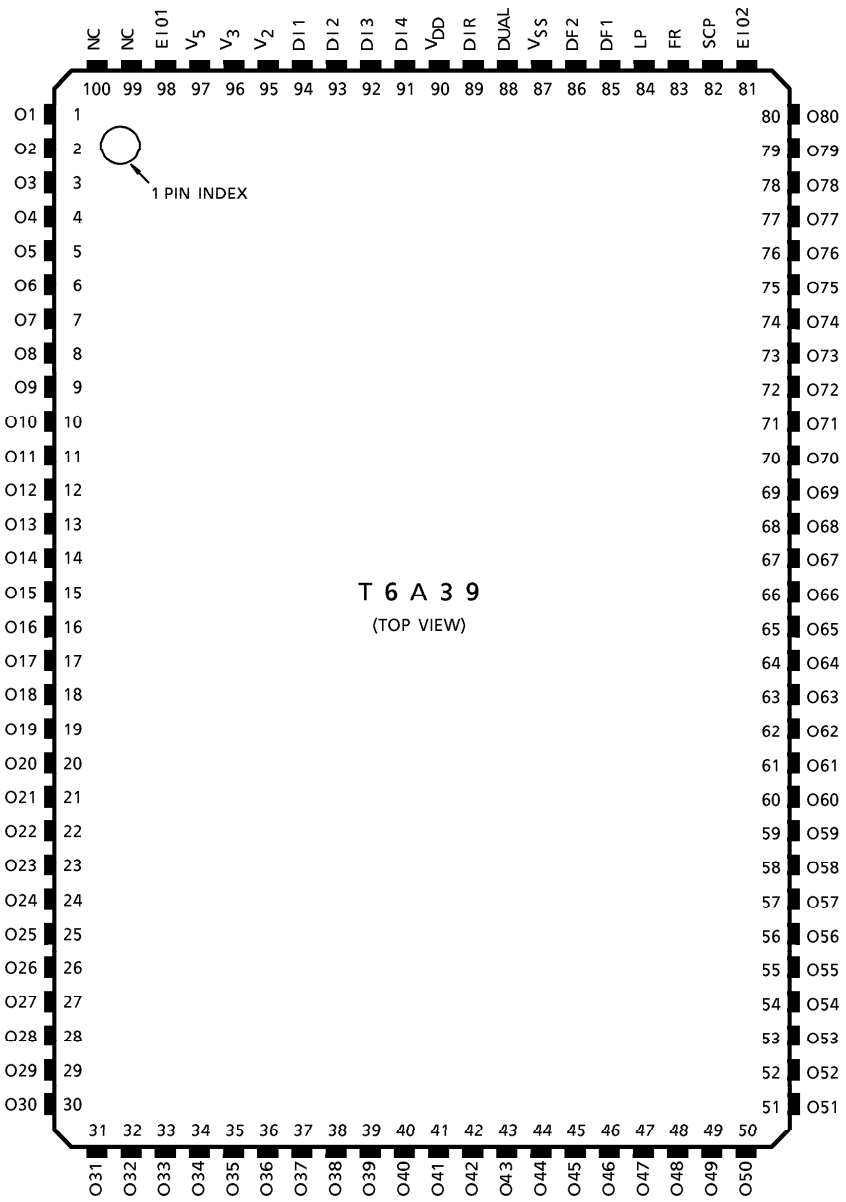
PIN ASSIGNMENT



PIN FUNCTIONS

<table>
<tr><th>PIN NAME</th><th>I/O</th><th>FUNCTIONS</th><th>LEVEL</th></tr>
<tr><td>O1 to O80</td><td>Output</td><td>Output for LCD drive signal</td><td>V_{DD} to V5</td></tr>
<tr><td>DI1 to DI4</td><td>Input</td><td>Input for shift data</td><td rowspan="9">V_{DD} to V_{SS}</td></tr>
<tr><td>SCP</td><td>Input</td><td>(Shift Clock Pulse)
Input for shift clock pulse</td></tr>
<tr><td>FR</td><td>Input</td><td>(Frame)
Input for frame signal</td></tr>
<tr><td>LP</td><td>Input</td><td>(Latch Pulse)
Input for shift clock pulse</td></tr>
<tr><td>DUAL</td><td>Input</td><td>(Dual Mode)
Terminal for dual input mode or single input mode select</td></tr>
<tr><td>DIR</td><td>Input</td><td>(Direction)
Input for data flow direction select</td></tr>
<tr><td>DF1, DF2</td><td>Input</td><td>(Data Format)
Input for selection data format (1-bit, 2-bit, 4-bit)</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>Input/output for ENABLE signal
<table>
<tr><th>DUAL</th><th>DIR</th><th>EIO2</th><th>EIO1</th></tr>
<tr><td>L</td><td>L</td><td>OUT</td><td>IN</td></tr>
<tr><td>L</td><td>H</td><td>IN</td><td>OUT</td></tr>
<tr><td>H</td><td>L</td><td>OUT</td><td>IN</td></tr>
<tr><td>H</td><td>H</td><td>OUT</td><td>IN</td></tr>
</table></td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply for internal logic (+5V)</td><td rowspan="5">—</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Power supply for internal logic (0V)</td></tr>
<tr><td>V2</td><td>—</td><td>Power supply for LCD drive circuit</td></tr>
<tr><td>V3</td><td>—</td><td>Power supply for LCD drive circuit</td></tr>
<tr><td>V5</td><td>—</td><td>Power supply for LCD drive circuit</td></tr>
</table>

RELATION BETWEEN FR, DATA INPUT AND OUTPUT LEVEL

FR	DATA INPUT (DI1 to DI4)	OUTPUT LEVEL
L	L	V2
L	H	V_{DD}
H	L	V3
H	H	V5

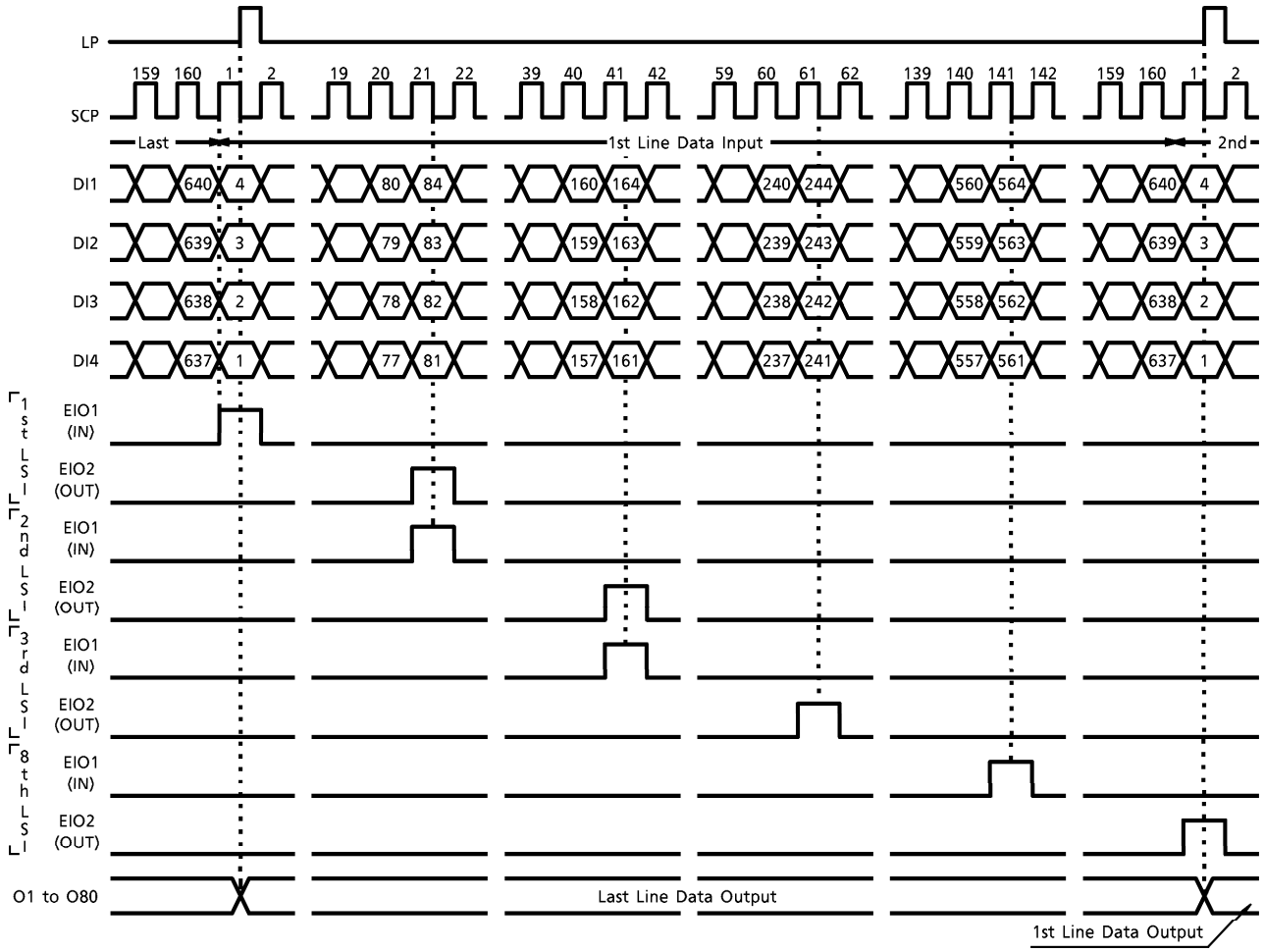
DATA INPUT FORMAT

DF1	DF2	DUAL	DIR	bits	DATA INPUT				DATA FORMAT			
					DI1	DI2	DI3	DI4	Ⓛ DI1 Ⓕ	Ⓛ DI2 Ⓕ	Ⓛ DI3 Ⓕ	Ⓛ DI4 Ⓕ
L	L	L	L	1-bit	*	*	*	IN	—	—	—	O80, O79···O2, O1
L	L	L	H		IN	*	*	*	O1, O2···O79, O80	—	—	—
L	L	H	L		*	*	*	IN	—	—	—	O80, O79···O42, O41
L	L	H	H		IN	*	*	IN	O1, O2···O39, O40	—	—	O80, O79···O42, O41
H	L	L	L	2-bit	*	*	IN	IN	—	—	O79, O77···O3, O1	O80, O78···O4, O2
H	L	L	H		IN	IN	*	*	O1, O3···O77, O79	O2, O4···O78, O80	—	—
H	L	H	L		*	*	IN	IN	—	—	O79, O77···O43, O41	O80, O78···O44, O42
H	L	H	H		IN	IN	IN	IN	O1, O3···O37, O39	O2, O4···O38, O40	O79, O77···O43, O41	O80, O78···O44, O42
*	H	L	L	4-bit	IN	IN	IN	IN	O77, O73···O5, O1	O78, O74···O6, O2	O79, O75···O7, O3	O80, O76···O8, O4
*	H	L	H		IN	IN	IN	IN	O1, O5···O73, O77	O2, O6···O74, O78	O3, O7···O75, O79	O4, O8···O76, O80
*	H	H	L		IN	IN	IN	IN	O77, O73···O45, O41	O78, O74···O46, O42	O79, O75···O47, O43	O80, O76···O48, O44
*	H	H	H	DON'T USE								

* Don't Care
Ⓛ→LAST DATA
Ⓕ→FIRST DATA

TIMING DIAGRAM

DIR = L



ABSOLUTE MAXIMUM RATINGS

(Ensure that the following conditions are maintained, $V_{CC} \geqq V_0 \geqq V_2 \geqq V_3 \geqq V_5 \geqq V_{SS}$, $V_{SS} = 0V$)

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	V_{DD}	V_{DD}	− 0.3 to 7.0	V
Supply Voltage 2	V2	V2	V_{DD} − 30 to V_{DD} + 0.3	V
Supply Voltage 3	V3	V3	V_{DD} − 30 to V_{DD} + 0.3	V
Supply Voltage 4	V5	V5	V_{DD} − 30 to V_{DD} + 0.3	V
Input Voltage	V_{IN}	(*1)	− 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	—	− 20 to 75	°C
Storage Temperature	T_{stg}	—	− 55 to 125	°C

(*1) SCP, FR, LP, DIR, DF1, DF2, DUAL, DI1 to DI4

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

TEST CONDITIONS (Unless otherwise noted, V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, V5 = (V_{DD} – 23) V ± 10%, Ta = – 20 to 75°C)

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT	PIN NAME
Supply Voltage 1		—	—	—		4.5	5.0	5.5	V	V_{DD}
Supply Voltage 2		V5	—	—		V_{DD} – 28	V_{DD} – 23	V_{DD} – 8.0	V	V5
Input Voltage	H Level	V_{IH}	—	T_{opr} = – 10 to 75°C (*2)		V_{DD} – 0.8 (*3)	—	V_{DD}	V	SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI4, DF1, DF2, DUAL
	L Level	V_{IL}		T_{opr} = – 10 to 75°C (*2)		0	—	0.8 (*4)		
Output Voltage	H Level	V_{OH}	—	—		V_{DD} – 0.3	—	V_{DD}	V	EIO1, EIO2
	L Level	V_{OL}		—		0	—	0.3		
Output Resistance (1)	H Level	R_{OH}	—	V_{OUT} = V_{DD} – 0.5V		—	—	1.0	kΩ	EIO1, EIO2
	L Level	R_{OL}	—	V_{OUT} = V_{SS} + 0.5V		—	—	1.0		
Output Resistance (2)	H Level	R_{OH}	—	V_{OUT} = V_{DD} – 0.5V (*5)		—	—	1.5	kΩ	O1 to O80
	M Level	R_{OM}	—	V_{OUT} = V2 ± 0.5V (*5)		—	—	1.5		
		R_{OM}	—	V_{OUT} = V3 ± 0.5V (*5)		—	—	1.5		
	L Level	R_{OL}	—	V_{OUT} = V5 + 0.5V (*5)		—	—	1.5		
Current Consumption (1) (*5)		I_{SS}	—	V_{DD} = 5.5V, V5 = – 22.5V, f_{FR} = 35Hz, f_{SCP} = 2.5MHz, O1 to O80 : No Load (*7)	Input Data: every bit inverted	—	1050	1400	μA	V_{SS}
					Input Data: low	—	770	1000		
Current Consumption (2) (*6)		I_{SS}	—	As mentioned above (*7)	Input Data: every bit inverted	—	260	350	μA	V_{SS}

(*2) R_L = 3kΩ, C_L = 500pF

(*3) V_{DD} – 0.7 (T_{opr} = – 20 to – 10°C)

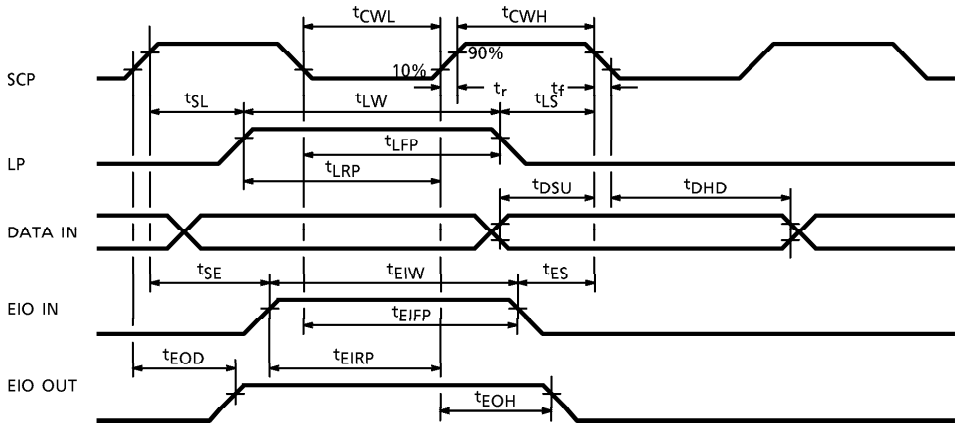
(*4) 0.7 (T_{opr} = – 20 to – 10°C)

(*5) Internal data receiver operating

(*6) Internal data receiver sleeping

(*7) V_{DD} = 5.0V, V_5 = – 7.8V, V_2 = V_{DD} – 2 / 9 (V_{DD} – V_5), V_3 = V_{DD} – 7 / 9 (V_{DD} – V_5)

AC CHARACTERISTICS



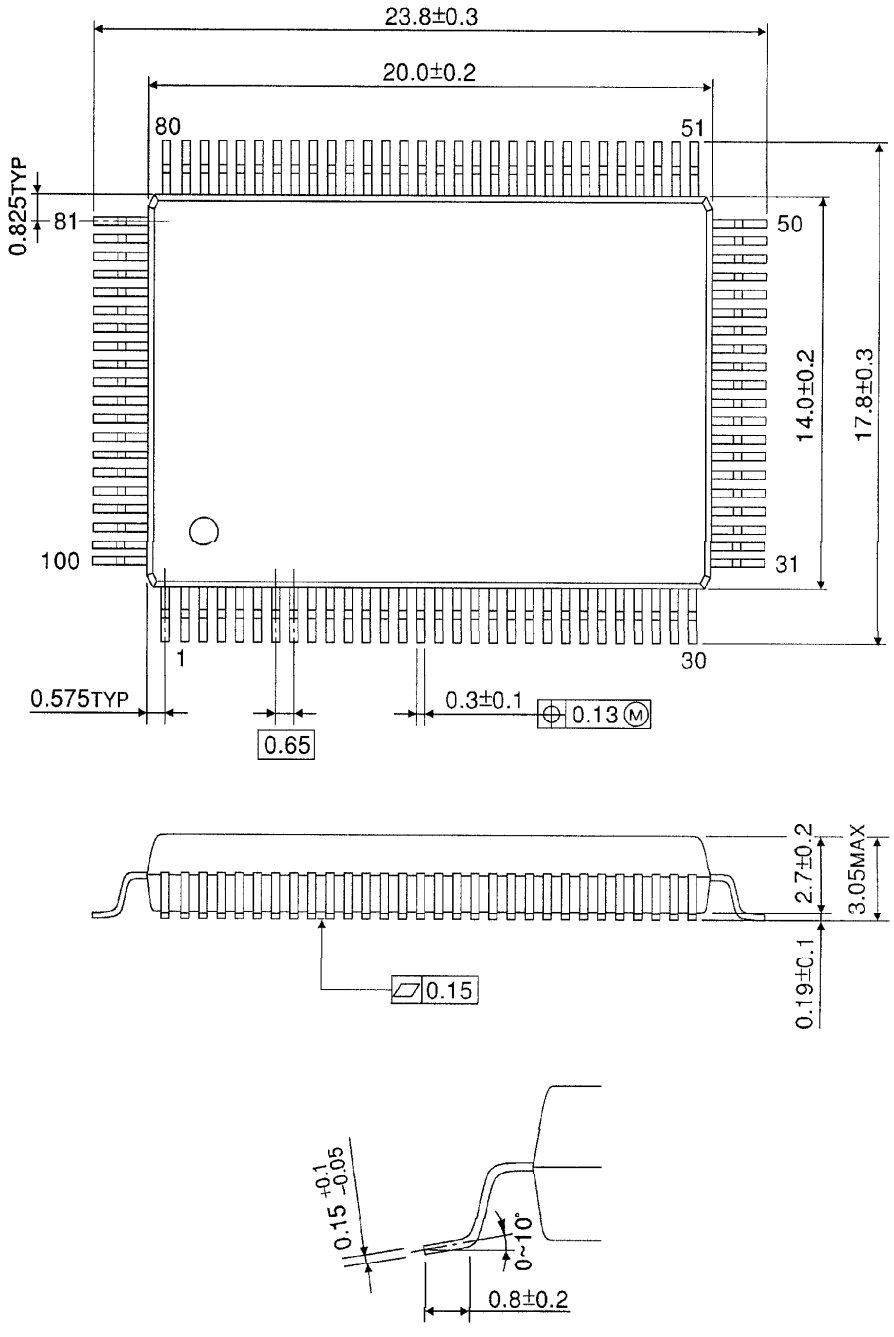
TEST CONDITIONS (V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, $V_0 = V_{DD}$, $V_5 = (V_{DD} - 23)$ V ± 10%, Ta = − 20 to 75°C)

ITEM	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Operating Frequency	t_{SCP}	—	—	4.0	MHz
SCP Pulse Width	t_{CWH}	—	95	—	ns
SCP Pulse Width	t_{CWL}	—	95	—	
Data Set-up Time	t_{DSU}	—	20	—	
Data Hold Time	t_{DHD}	—	40	—	
SCP Rise / Fall Time	t_r, t_f	—	—	30	
LP Set-up Time	t_{LRP}	—	20	—	
LP Hold Time	t_{LFP}	—	40	—	
LP Pulse Width	t_{LW}	—	40	—	
SCP-Rise-to-LP-Rise Time	t_{SL}	—	10	—	
LP-Fall-to-SCP-Fall Time	t_{LS}	—	10	—	
EIO IN Set-up Time	t_{EIRP}	—	20	—	
EIO IN Hold Time	t_{EIFP}	—	40	—	
EIO IN Pulse Width	t_{EIW}	—	40	—	
SCP-Rise-to-EIO-Rise Time	t_{SE}	(*8)	10	—	
EIO-Fall-to-SCP-Fall Time	t_{ES}	(*8)	10	—	
EIO OUT Data Delay Time	t_{EOD}	—	—	100	
EIO OUT Hold Time	t_{EOH}	—	—	95	

(*8) C_L = 10pF

PACKAGE DIMENSIONS

QFP100-P-1420-0.65A Unit: mm



Weight : 1.60g (typ.)