

HA13426

Three-Phase Motor Driver with Speed Discriminator

Description

The HA13426 power IC for driving the three-phase brushless motor of 5.25 inch-HDD (hard disk drive) includes a speed discriminator. It is possible to construct a servo system with by adding a quartz resonator and few external components.

Because it uses a voltage drive system, it controls EMI (electro magnetic interference) noise from the motor driver.

Features

- Single-chip servo system
- Large output current (3A)
- Digital servo system requires no adjustment.
- The voltage drive system (not supply voltage control) causes almost no spike voltage at commutation which causes EMI in conventional systems
- TTL-level START/STOP terminal
- Load-short brake at STOP mode
- Built-in current limiter depresses maximum current at starting.
- Frequency divide permits wide selection for quartz resonator.

Block Diagram

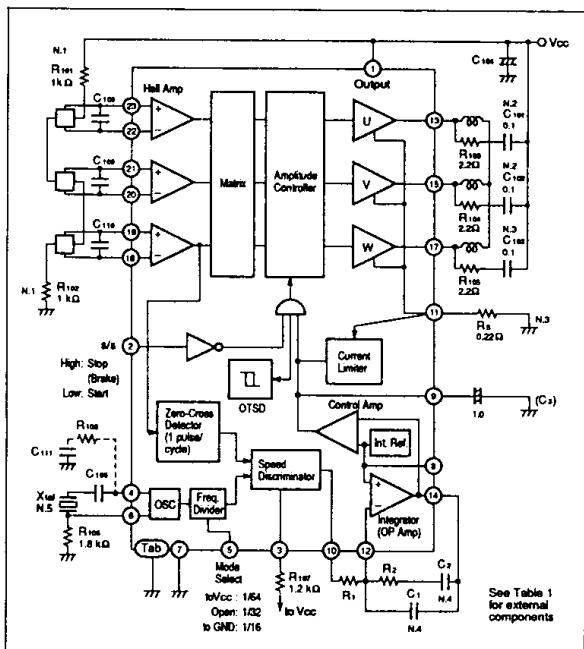


Table 1 External Components

| Part No. | Recommended Value | Function | Note |
|--|----------------------------|--------------------------|-------------|
| R ₁₀₁ , R ₁₀₂ | 1 kΩ | Hall effect element bias | 1 |
| R ₁₀₃ , R ₁₀₄ , R ₁₀₅ | 2.2 Ω (0.5 W) | Stability | |
| R ₁₀₆ | 1.8 kΩ | OSC bias | 6 |
| R ₁₀₇ | 1.2 kΩ | Speed descrim. bias | |
| R ₁₀₈ | 470 Ω | Stability | 6 |
| R _{1, R₂} | See functional description | Integration constant | |
| R _s | — | Current sense | 3 |
| C ₁₀₁ , C ₁₀₂ , C ₁₀₃ | 0.1 μF | Stability | 2 |
| C ₁₀₄ | ≥0.1 μF | Vcc bypassing | |
| C ₁₀₆ | 10 pF | AC coupling OSC | |
| C ₁₀₈ , C ₁₀₉ , C ₁₁₀ | ≥0.01 μF | Stability | |
| C ₁₁₁ | 4700 pF | Stability | 5 |
| C _{1, C₂} | See functional description | Integration constant | 4 |
| C ₃ | See functional description | Filter constant | |
| Xtal | See functional description | Resonator | |

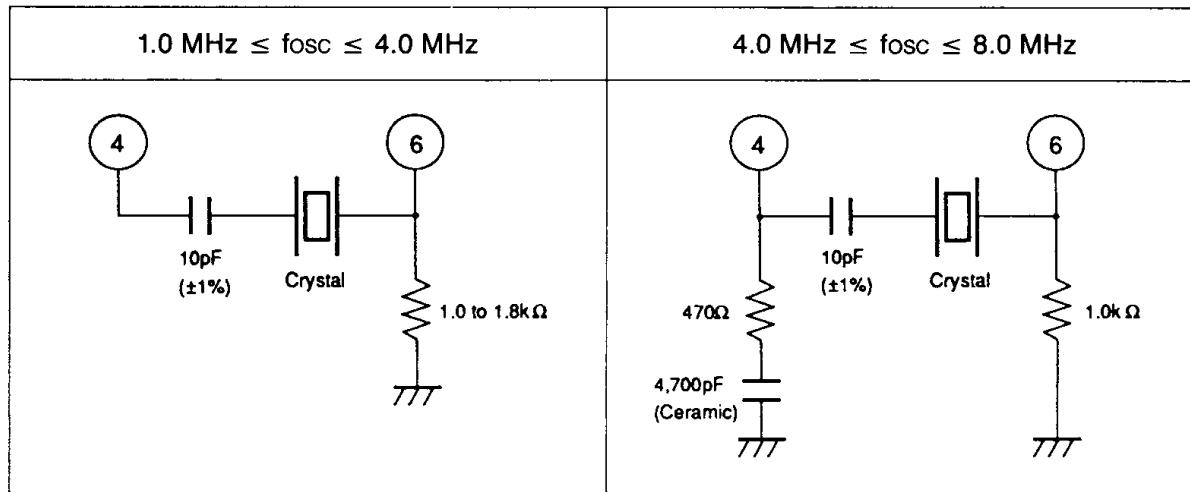
Notes: 1. Set R₁₀₁ and R₁₀₂ so that output voltage of more than 50 mVpp is applied to hall-effect elements.

2. Use capacitors for C₁₀₁ to C₁₀₃ which cause no 2nd resonance.
Connect the common points of C₁₀₁, C₁₀₂, and C₁₀₃ to the most stable of Vcc, GND, on the middle point of the coil (use non-polar capacitor when connecting them to the middle point of the coil).
3. Output current is limited as shown below by R_s value.

$$I_{limit} = \frac{0.56 V \pm 10 \%}{R_s(\Omega)}$$

For example, output current is limited to 2.55 A ± 10 % at R_s=0.22 Ω

4. C₁ and C₂ must be nonpolar.
5. Determine external components of Oscillator as shown below in accordance with the frequency range.



Functional Description

Resonator Selection

HA13426: The synchronous oscillating frequency, f_{osc} , and the motor rotation speed N have the relationship;

$$N = \frac{60}{512} \cdot \frac{m \cdot f_{osc}}{p} \text{ (rpm)} \quad (1)$$

where p is the number of motor poles and m is the dividing ratio of the divider. The mode select pin determines m (Table 2).

Table 2 Dividing Ratio

| Mode Select | m |
|-------------|------|
| GND | 1/16 |
| Open | 1/32 |
| Vcc | 1/64 |

Table 3 shows sample values of f_{osc} to rotate a 4-poles motor at 3600 rpm.

Table 3 fosc Examples

| Mode Select | fosc(MHz) |
|-------------|-----------|
| GND | 1.96608 |
| Open | 3.93216 |
| Vcc | 7.86432 |

HA13431/432/432MP: The synchronous oscillating frequency f_{osc} , and the FG frequency, f_{FG} , have the relationship;

$$f_{FG} = \frac{m \cdot f_{osc}}{1024} \quad (2)$$

where m is the dividing ratio of the divider, and determined by one of the mode select pin (Table 4).

Table 4 Dividing Ratio

| Mode Select | m |
|-------------|-----|
| GND | 1 |
| Open | 1/2 |
| Vcc | 1/4 |

Determining Integration Constants R₁, R₂, C₁, and C₂, and Filter Constant C₃

Figure 1 is the block diagram showing motor speed control by the HA13426/431/432/432MP. The part enclosed by dotted lines denotes the IC, and G₁ (S) and G₂ (S) indicate an integrator transfer function and the transfer function from control amp to output, respectively. Since these ICs are driven by voltage, the motor coil impedance and the kick-back voltage are contained in the loop.

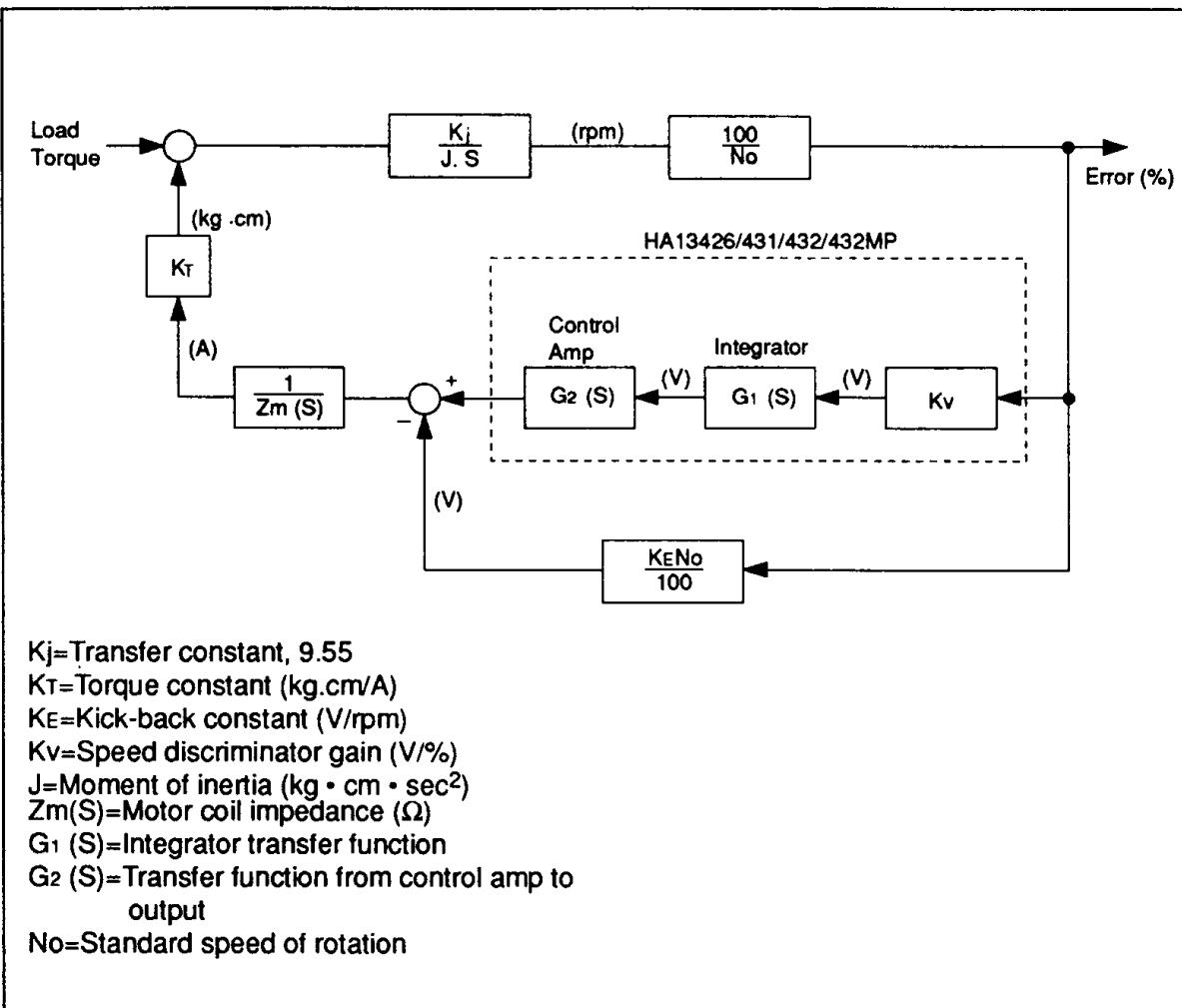


Figure 1 Block Diagram

In Figure 1, when

$$A(S) = \frac{K_j}{J \cdot S} \cdot \frac{100}{No} \quad \dots \dots \dots (3)$$

$$\beta(S) = \frac{K_t}{Z_m(S)} \left(K_v \cdot G_1(S) \cdot G_2(S) - \frac{K_E \cdot No}{100} \right) \dots \dots \dots (4)$$

Then Figure 1 can be shown in Figure 2.

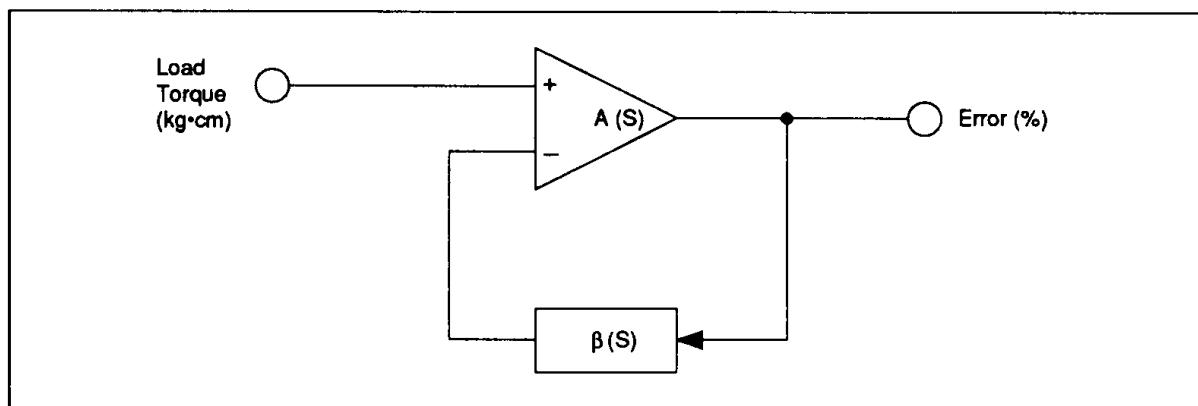


Figure 2 Simplified Block Diagram



HA13426

On the other hand, $Z_m(S)$, $G_1(S)$, and $G_2(S)$ are expressed as follows;

$$Z_m(S) = R_m(1+S/\omega_m) \dots (5)$$

$$G_1(S) = \frac{R_2}{R_1} \frac{1+\omega_2/S}{1+S/\omega_1} \dots (6)$$

$$G_2(S) = \frac{G_{CTL}}{1+S/\omega_3} \dots (7)$$

Then,

$$\omega_m = \frac{R_m}{L_m} \dots (8)$$

$$\omega_1 = \frac{1}{C_1 R_2} \dots (9)$$

$$\omega_2 = \frac{1}{C_2 R_2} \dots (10)$$

$$\omega_3 = \frac{1}{C_3 R_3} \dots (11)$$

G_{CTL} and R_3 are the internal constant of the IC. Substituting equations (5) to (11) into equation (4), $\beta(S)$, gives

$$\begin{aligned} \beta(S) &= \frac{K_T}{R_m(1+S/\omega_m)} \left(\frac{R_2 K_v G_{CTL}(1+\omega_2/S)}{R_1(1+S/\omega_1)(1+S/\omega_3)} \frac{K_e N_o}{100} \right) \\ &= \frac{R_2 K_T K_v G_{CTL}}{R_1 R_m} \frac{1+\omega_2/S}{(1+S/\omega_m)(1+S/\omega_1)(1+S/\omega_3)} \dots (12) \end{aligned}$$

assuming $\left(\frac{R_2 K_v G_{CTL}}{R_1} \gg \frac{K_e N_o}{100} \right)$

To control speed within a stable fashion, $A(S)$ and $\beta(S)$ must have the relationship shown in Figure 3. That is, the angular frequency of the crosspoint of $A(S)$ and $\beta(S)$, ω_0 , should be between the angular frequency of the integrator, ω_1 and ω_2 .

Determining ω_0 : ω_0 uses the value of 1/10 to 1/30 of the ω_m or the angular frequency of FG, ω_{FG} , whichever is lower. In the HA13426, the angular frequency of the Hall-effect signal is used for ω_{FG} , and the ω_0 has the value of 1/30 to 1/100 of ω_{FG} .

Calculating A_0 from equation(3):

$$A_0 = \frac{K_j}{J \cdot \omega_0} \frac{100}{N_o} \dots (13)$$

Designing R_1 and R_2

From Figure 3 and equation (12):

$$\frac{R_2}{R_1} = \frac{R_m}{K_T \cdot K_v \cdot G_{CTL} \cdot A_0} \dots (14)$$

Each IC is designed with K_v and G_{CTL} as shown in Table 5.

Table 5 Kv and GCTL

| Type | $K_v(V\%)$ | $G_{CTL}(V/V)$ |
|------------|------------|----------------|
| HA13426 | 0.03 | 16 typ |
| HA13431 | 0.023 | 16 typ |
| HA13432/MP | 0.023 | 8 typ |

Small R_1 increases C_1 and C_2 and large R_1 will cause speed error by the cutoff current of the speed discriminator and the input bias current of the integrator. Values of 10-56kΩ are recommended.

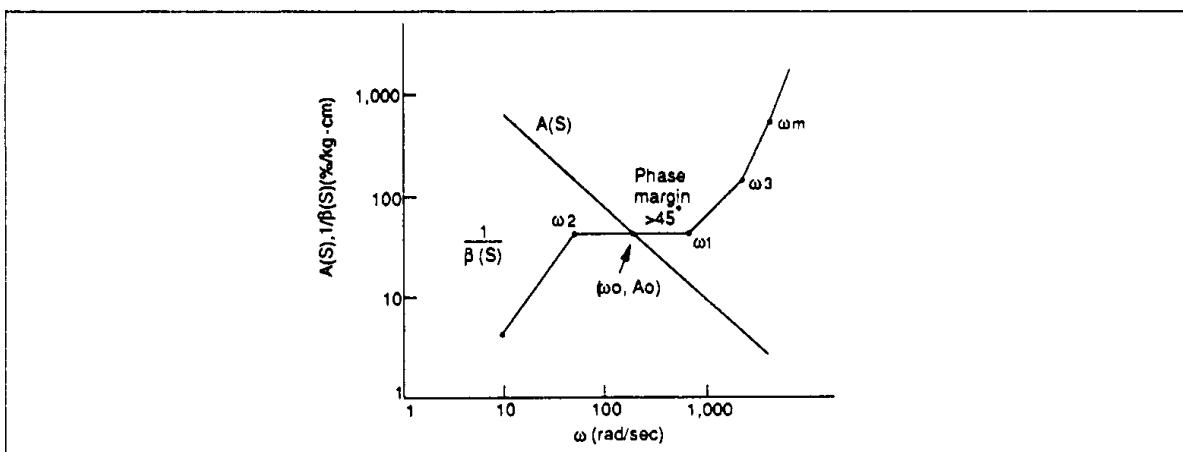


Figure 3 Stable Relationship of $A(S)$ and $\beta(S)$



Determining ω_1, ω_2 and ω_3 :

$$\omega_1 \geq 3\omega_0$$

$$\omega_2 \leq \omega_0/3$$

$$\omega_3 \geq 3\omega_0$$

Designing C_1, C_2, C_3 : from equations (9), (10), (11),

$$C_1 = 1/\omega_1 R_2$$

$$C_2 = 1/\omega_2 R_2$$

$$C_3 = 1/\omega_3 R_3$$

where the R_3 is $22\text{k}\Omega$.

Using an External Clock

As shown in Figure 4 an external clock can be provided at the OSC input pin. But applying too large an input causes mis-operation of the IC. Resistor R_s must be connected in series to control the current.

HA13426:

$$R_s \geq 2.5(V_{IH}-1.4)-1.5 \quad (\text{k}\Omega)$$

$$R_s \leq 7.5(1.4-V_{IL})-1.5 \quad (\text{k}\Omega)$$

A speed-up capacitor parallel to R_s should be considered.

HA13431/432/432MP:

$$R_s \geq 3.7(V_{IH}-1.7)-2 \quad (\text{k}\Omega)$$

$$R_s \leq 1.0(1.7-V_{IL})-2 \quad (\text{k}\Omega)$$

The input currents, I_{IH} and I_{IL} , are restricted as follows and the external clock must have a larger driving capacity:

$$I_{IH} = \frac{V_{IH}-1.4}{R_s+R_i} \quad (\text{mA})$$

$$I_{IL} = \frac{1.4-V_{IL}}{R_s+R_i} \quad (\text{mA})$$

where R_i , the input resistance of OSC, is $1.5\text{k}\Omega$ in HA13426 or $2\text{k}\Omega$ in the others.

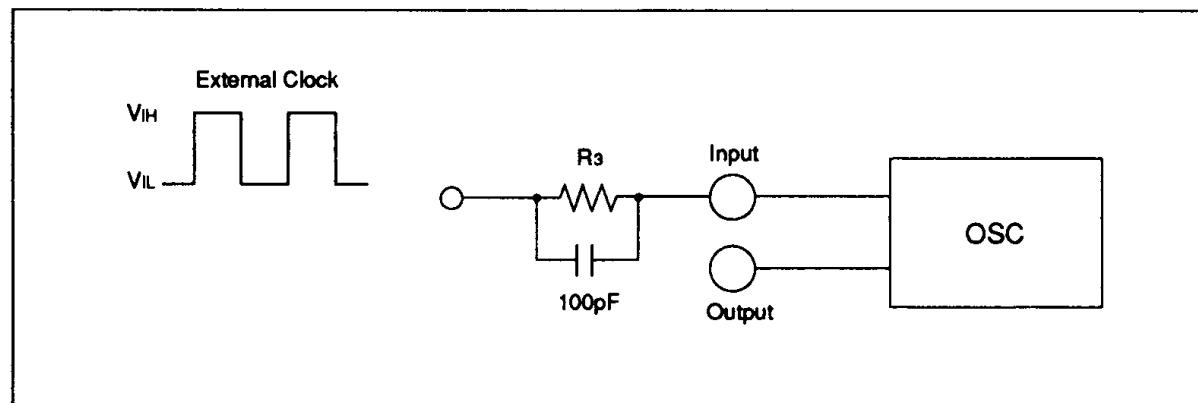


Figure 4 External Clock

Producing the Ready Signal

As shown in Figure 5, an external comparator can produce the ready signal. Since the DC gain is extremely high (70dB or more), the rotation error, ΔN , when the ready signal V_R becomes high is

determined by the accuracy of the speed discriminator without the influence of the comparator window.

Open collector output type comparators are recommended.

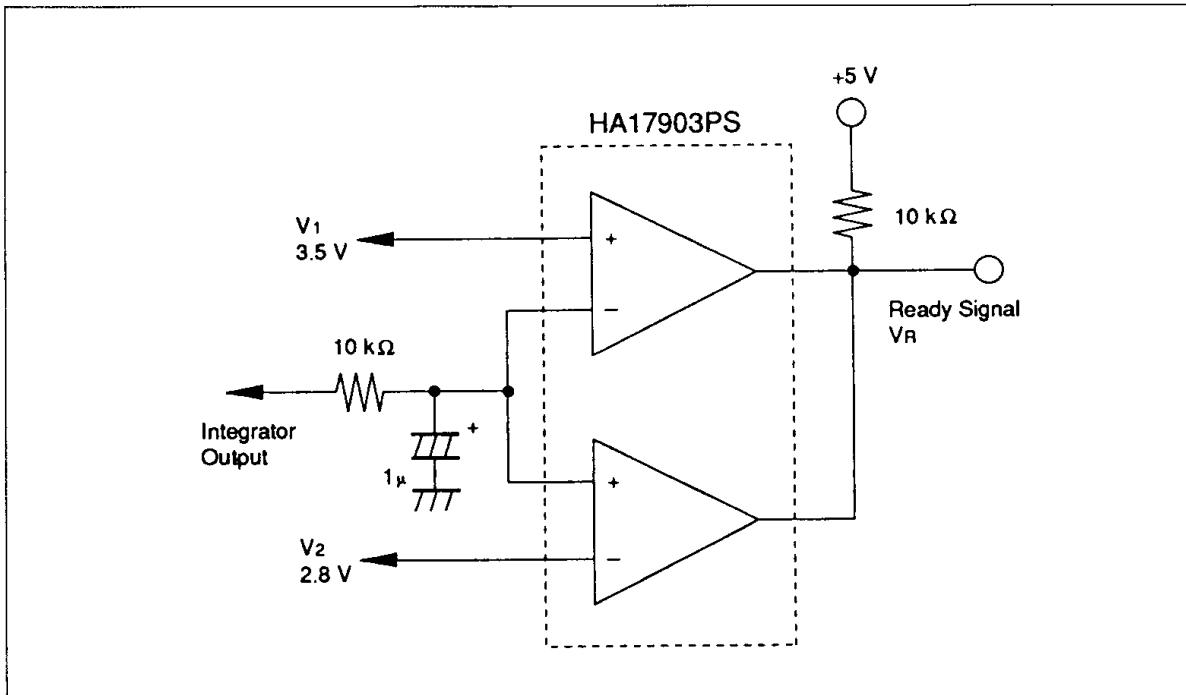


Figure 5 Ready Signal

Table 5 Absolute Maximum Ratings ($T_a = 25^\circ C$)

| Item | Symbol | Ratings | Unit | Note |
|--------------------------------------|------------------|----------------------|------|------|
| Supply voltage | V _{CC} | 15 | V | 1 |
| Input voltage | V _{IN} | 0 to V _{CC} | V | 2 |
| Output current | I _O | 3 | A | |
| Power dissipation | P _T | 25 | W | 3 |
| Junction temperature | T _J | 150 | °C | |
| Operating junction temperature range | T _{JOP} | -20 to +125 | °C | |
| Storage temperature range | T _{STG} | -55 to +125 | °C | |

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Notes: 1. Recommended operating voltage:

$V_{CC} = 12 V \pm 15\% (10.2 \text{ to } 13.8V)$

2. Applied to Hall-effect element amp, mode select input.

Maximum input voltage at start/stop is 6 V.

3. Thermal resistance:

$\theta_{J-R} \leq 3^\circ C/W$

$\theta_{J-A} \leq 40^\circ C/W$



Table 6 Electrical Characteristics (Ta=25°C, Vcc=12 V)

| Item | | Symbol | Min | Typ | Max | Unit | Test Condition |
|-------------------------|----------------------------------|-----------------------|-----|-------|------|------|------------------------------------|
| Total | Supply current | I _{so} | — | 50 | 70 | mA | S/S = 2.0 V |
| | | I _s | — | 55 | 75 | mA | S/S = 0.8 V, R _L = Open |
| | Over-temperature protection | T _{sd} | — | 150 | — | °C | Shutdown |
| | | Thys | — | 20 | — | °C | Hysteresis |
| Hall-effect element amp | Input bias current | I _{HB} | — | 2 | 10 | μA | V _H = 6.0 V |
| | Input common mode voltage range | V _H | 2.0 | — | 10 | V | |
| | Voltage gain | G _{VH} | — | 10 | — | dB | |
| Output stage | Quiescent output voltage | V _Q | 5.3 | 5.9 | 6.5 | V | |
| | Phase difference | △V _Q | — | — | ±0.3 | V | |
| | Saturation voltage (Note) | V _{CE(sat)1} | — | 2.4 | 3.2 | V | I _O = 2 A |
| | Output impedance | R _O | — | 0.2 | — | Ω | I _O = 0.4 A |
| Control amp | Internal ref. voltage | V _{ref1} | 3.0 | 3.2 | 3.4 | V | |
| | Voltage gain (CTL amp to output) | G _{CTL} | 21 | 24 | 27 | dB | |
| | Difference of gain | △G _{CTL} | — | — | ±2 | dB | |
| Integrator | Input bias current | I _B | — | — | ±0.1 | μA | |
| | Output voltage swing | A | — | 0.7 | — | V | I _O = 0.3 mA |
| | | A | — | 0.7 | — | V | I _O = -0.3 mA |
| Speed discriminator | Output voltage swing | V _{OH} | 5.8 | 6.1 | — | V | I _O = 0.3 mA |
| | | V _{OL} | — | — | 0.2 | V | I _O = -0.3 mA |
| | Cutoff current | I _{off} | — | — | ±0.1 | μA | Charge pump off |
| | Operating frequency | f _{CLK} | 60 | — | 250 | kHz | |
| Start/stop | Count number | N | — | 1024 | — | | |
| | Input high voltage | V _{IH} | 2.0 | — | — | V | Stop |
| | Input low voltage | V _{IL} | — | — | 0.8 | V | Start |
| | Input high current | I _{IH} | — | -0.15 | -0.5 | mA | V _H = 2.0 V |
| | Input low current | I _{IL} | — | -0.2 | -0.5 | mA | V _L = 0.8V |

HA13426

Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$) (cont)

| Item | | Symbol | Min | Typ | Max | Unit | Test Condition |
|-----------------|-----------------------------|------------|------|-------|------|------|------------------------|
| Current limiter | Reference voltage | | 0.52 | 0.56 | 0.60 | V | |
| Mode select | 1/16 division input voltage | $V_{1/16}$ | — | — | 0.8 | V | |
| | 1/32 division input voltage | $V_{1/32}$ | — | 6.3 | — | V | Open |
| | 1/64 division input voltage | $V_{1/64}$ | 11.2 | — | — | V | |
| | 1/16 division input current | $I_{1/16}$ | — | -0.63 | -1.3 | mA | $V_{IN} = 0\text{ V}$ |
| | 1/64 division input current | $I_{1/64}$ | — | 1.0 | 1.5 | mA | $V_{IN} = 12\text{ V}$ |
| Oscillator | Operating frequency | f_{osc} | — | — | 8.0 | MHz | |

Note: Sum of upper and lower transistor saturation voltages

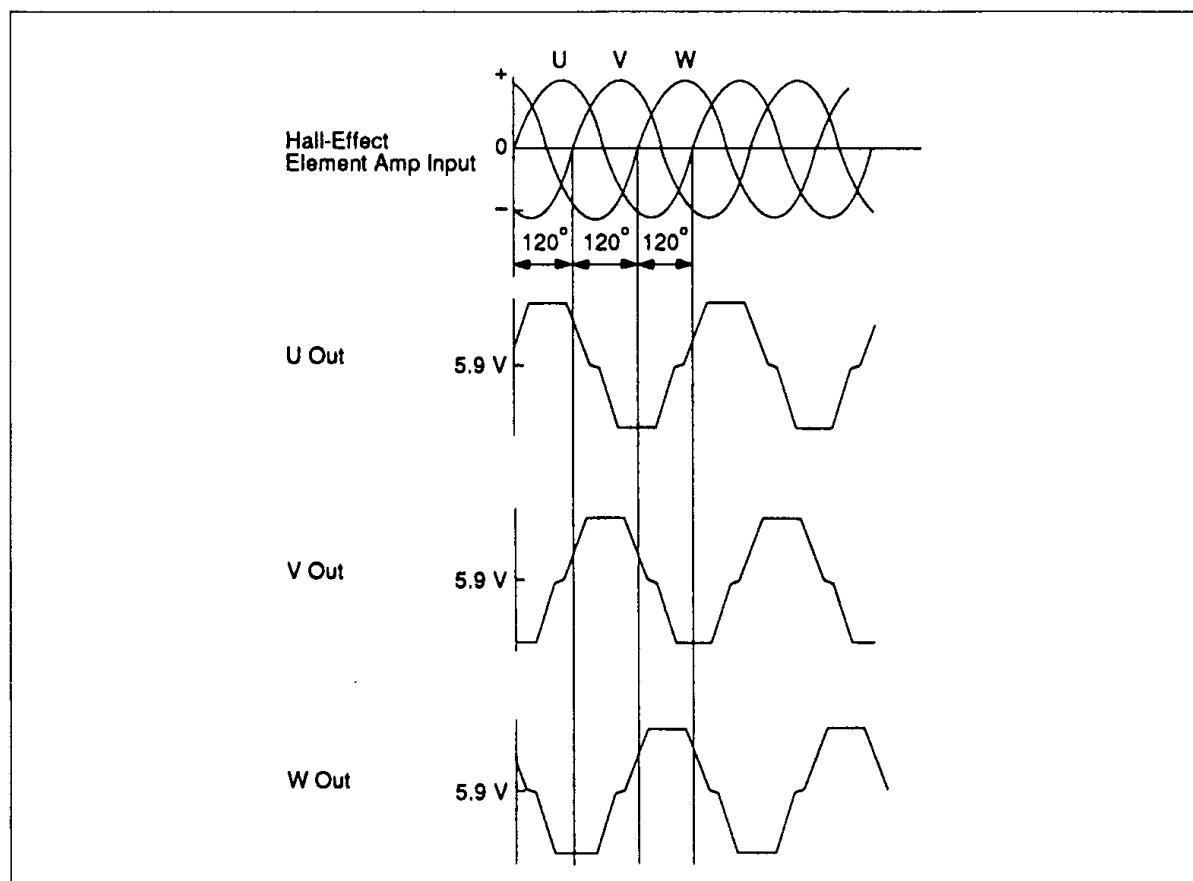


Figure 6 Timing Waveform

