

Phase Control Circuit - General Purpose Feedback

Description

The integrated circuit U211B2/ B3 is designed as a phase control circuit in bipolar technology with an internal frequency-voltage converter. Furthermore, it has an internal control amplifier which means it can be used for speed-regulated motor applications.

It has an integrated load limitation, tacho monitoring and soft-start functions, etc. to realize sophisticated motor control systems.

Features

- Internal frequency-to-voltage converter
- Externally-controlled integrated amplifier
- Overload limitation with a “fold back” characteristic
- Optimized soft-start function
- Tacho monitoring for shorted and open loop
- Automatic retriggering switchable

- Triggering pulse typ. 155 mA
- Voltage and current synchronization
- Internal supply-voltage monitoring
- Temperature reference source
- Current requirement ≤ 3 mA

Package: DIP18 - U211B2,
SO16 - U211B3

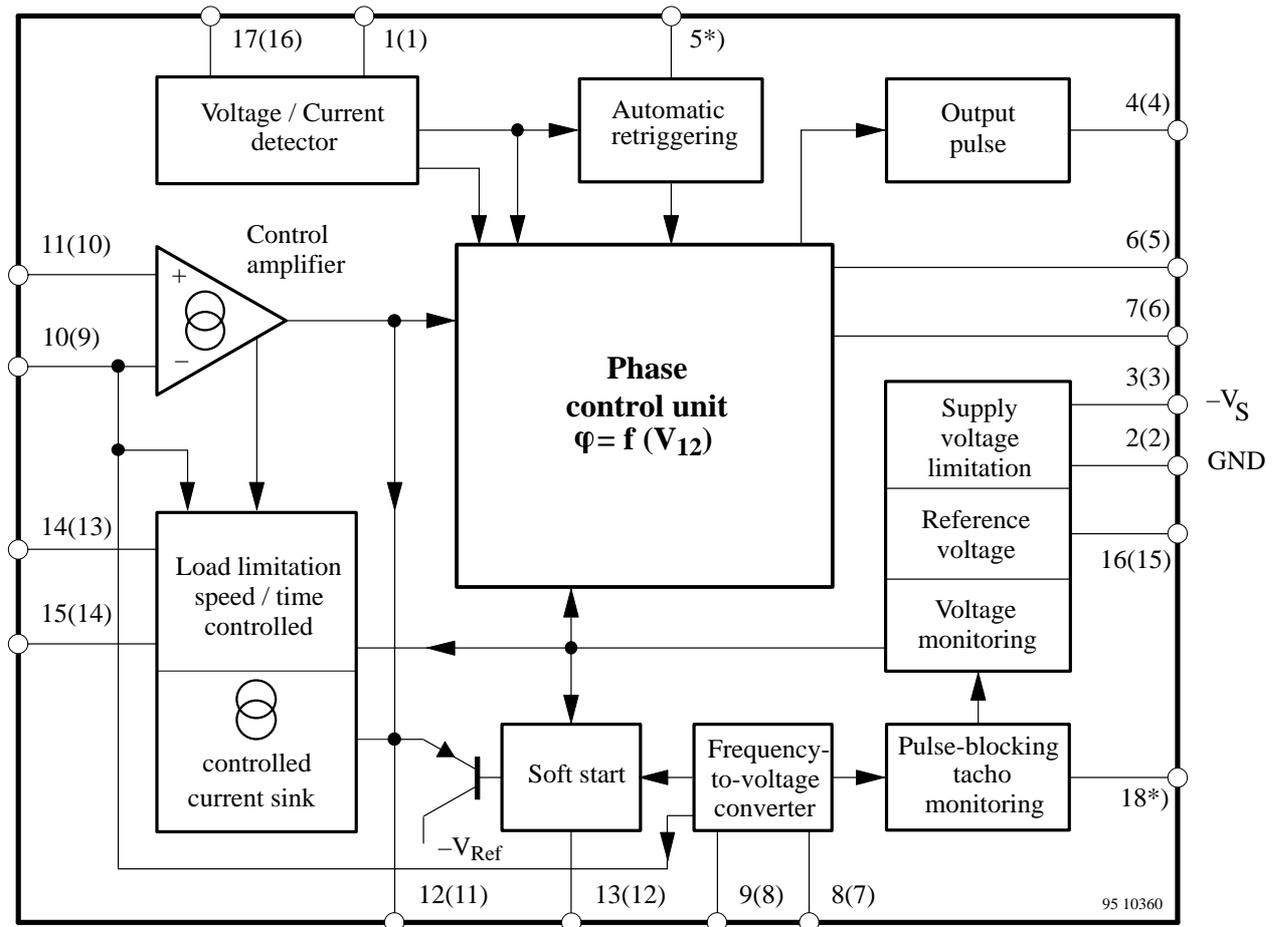


Figure 1. Block diagram (Pins in brackets refer to SO16)
*) Pins 5 and 18 connected internally

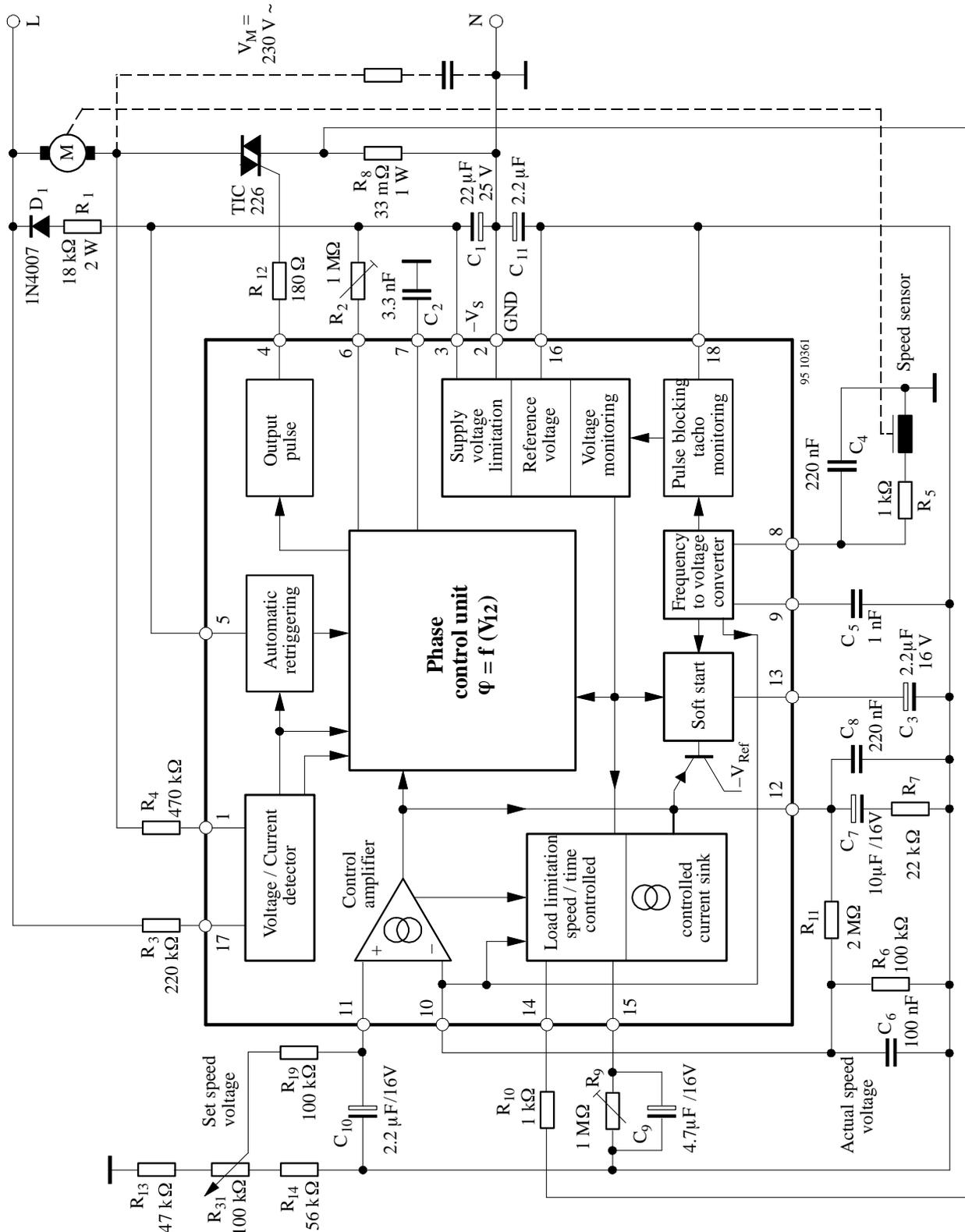


Figure 2. Speed control, automatic retriggering, load limiting, soft start

Description

Mains Supply

The U211B2 is fitted with voltage limiting and can therefore be supplied directly from the mains. The supply voltage between Pin 2 (+ pol/⊥) and Pin 3 builds up across D₁ and R₁ and is smoothed by C₁. The value of the series resistance can be approximated using (see figure 2):

$$R_1 = \frac{V_M - V_S}{2 I_S}$$

Further information regarding the design of the mains supply can be found in the data sheets in the appendix. The reference voltage source on Pin 16 of typ. -8.9 V is derived from the supply voltage and is used for regulation.

Operation using an externally stabilised DC voltage is not recommended.

If the supply cannot be taken directly from the mains because the power dissipation in R₁ would be too large, then the circuit shown in the following figure 3 should be used.

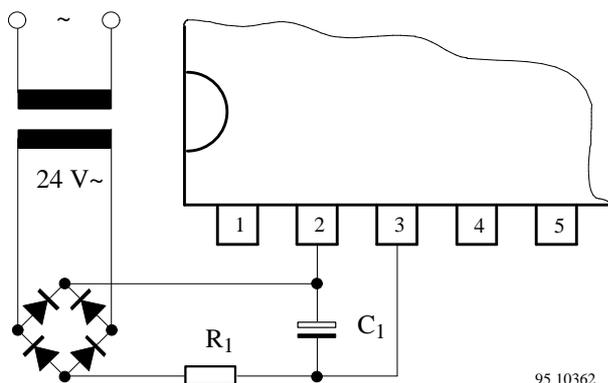


Figure 3. Supply voltage for high current requirements

Phase Control

There is a general explanation in the data sheet, TEA1007, on the common phase control function. The phase angle of the trigger pulse is derived by comparing the ramp voltage (which is mains synchronized by the voltage detector) with the set value on the control input Pin 12. The slope of the ramp is determined by C₂ and its charging current. The charging current can be varied using R₂ on Pin 6. The maximum phase angle α_{max} can also be adjusted using R₂.

When the potential on Pin 7 reaches the nominal value predetermined at Pin 12, then a trigger pulse is generated whose width t_p is determined by the value of C₂ (the value of C₂ and hence the pulse width can be evaluated by assuming 8 μs/nF). At the same time, a latch is set, so that as long as the automatic retriggering has not been activated, then no more pulses can be generated in that half cycle.

The current sensor on Pin 1 ensures that, for operations with inductive loads, no pulse will be generated in a new half-cycle as long as a current from the previous half cycle is still flowing in the opposite direction to the supply voltage at that instant. This makes sure that “gaps” in the load current are prevented.

The control signal on Pin 12 can be in the range 0 V to -7 V (reference point Pin 2).

If V₁₂ = -7 V then the phase angle is at maximum = α_{max} i.e., the current flow angle is a minimum. The phase angle α_{min} is minimum when V₁₂ = V₂.

Voltage Monitoring

As the voltage is built up, uncontrolled output pulses are avoided by internal voltage surveillance. At the same time, all of the latches in the circuit (phase control, load limit regulation, soft start) are reset and the soft-start capacitor is short circuited. Used with a switching hysteresis of 300 mV, this system guarantees defined start-up behavior each time the supply voltage is switched on or after short interruptions of the mains supply.

Soft-Start

As soon as the supply voltage builds up (t₁), the integrated soft-start is initiated. The figure below shows the behaviour of the voltage across the soft-start capacitor and is identical with the voltage on the phase control input on Pin 12. This behaviour guarantees a gentle start-up for the motor and automatically ensures the optimum run-up time.

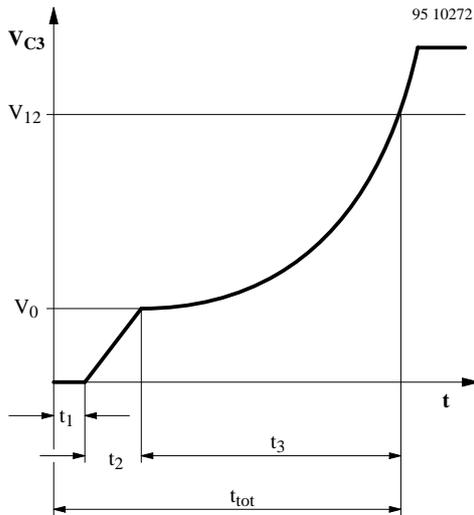


Figure 4. Soft-start

- t_1 = build-up of supply voltage
- t_2 = charging of C_3 to starting voltage
- $t_1 + t_2$ = dead time
- t_3 = run-up time
- t_{tot} = total start-up time to required speed

C_3 is first charged up to the starting voltage V_0 with typical $45 \mu\text{A}$ current (t_2). By then reducing the charging current to approx. $4 \mu\text{A}$, the slope of the charging function is substantially reduced so that the rotational speed of the motor only slowly increases. The charging current then increases as the voltage across C_3 increases giving a progressively rising charging function which accelerates the motor more and more strongly with increasing rotational speed. The charging function determines the acceleration up to the set-point. The charging current can have a maximum value of $55 \mu\text{A}$.

Frequency to Voltage Converter

The internal frequency to voltage converter (f/V-converter) generates a DC signal on Pin 10 which is proportional to the rotational speed using an AC signal from a tacho-generator or a light beam whose frequency is in turn dependent on the rotational speed. The high impedance input Pin 8, compares the tacho-voltage to a switch-on threshold of typ. -100 mV . The switch-off threshold is given with -50 mV . The hysteresis guarantees very reliable operation even when relatively simple tacho-generators are used. The tacho-frequency is given by:

$$f = \frac{n}{60} \times p \text{ (Hz)}$$

where: n = revolutions per minute
 p = number of pulses per revolution

The converter is based on the charge pumping principle. With each negative half wave of the input signal, a quantity of charge determined by C_5 is internally amplified and then integrated by C_6 at the converter output on Pin 10. The conversion constant is determined by C_5 , its charge transfer voltage of V_{ch} , R_6 (Pin 10) and the internally adjusted charge transfer gain.

$$G_i \left[\frac{I_{10}}{I_9} \right] = 8.3$$

$$k = G_i \times C_5 \times R_6 \times V_{ch}$$

The analog output voltage is given by

$$V_O = k \cdot f$$

The values of C_5 and C_6 must be such that for the highest possible input frequency, the maximum output voltage V_O does not exceed 6 V . While C_5 is charging up, the R_i on Pin 9 is approx. $6.7 \text{ k}\Omega$. To obtain good linearity of the f/V converter the time constant resulting from R_i and C_5 should be considerably less ($1/5$) than the time span of the negative half-cycle for the highest possible input frequency. The amount of remaining ripple on the output voltage on Pin 10 is dependent on C_5 , C_6 and the internal charge amplification.

$$\Delta V_O = \frac{G_i \times V_{ch} \times C_5}{C_6}$$

The ripple ΔV_O can be reduced by using larger values of C_6 . However, the increasing speed will then also be reduced.

The value of this capacitor should be chosen to fit the particular control loop where it is going to be used.

Pulse Blocking

The output of pulses can be blocked using Pin 18 (standby operation) and the system reset via the voltage monitor if $V_{18} \geq -1.25 \text{ V}$. After cycling through the switching point hysteresis, the output is released when $V_{18} \leq -1.5 \text{ V}$ followed by a soft-start such as that after turn on.

Monitoring of the rotation can be carried out by connecting an RC network to Pin 18. In the event of a short or open circuit, the triac triggering pulses are cut off by the time delay which is determined by R and C . The capacitor C is discharged via an internal resistance $R_i = 2 \text{ k}\Omega$ with each charge transfer process of the f/V converter. If there are no more charge transfer processes C is charged up via R until the switch-off threshold is exceeded and the triac triggering pulses are cut off. For operation without trigger pulse blocking or monitoring of the rotation, Pins 18 and 16 must be connected together.

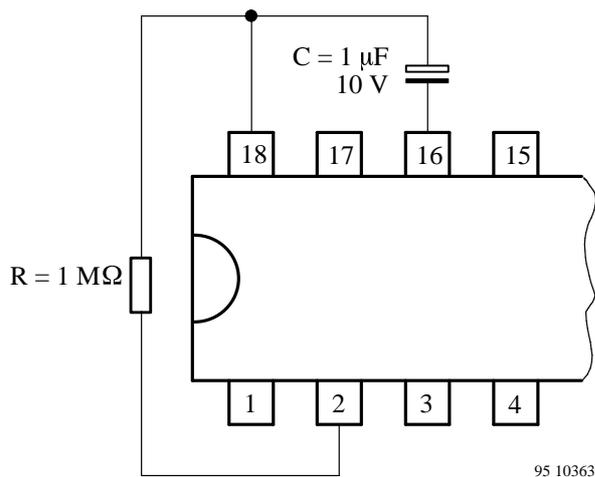


Figure 5. Operation delay

Control Amplifier (Figure 2)

The integrated control amplifier with differential input compares the set value (Pin 11) with the instantaneous value on Pin 10 and generates a regulating voltage on the output Pin 12 (together with the external circuitry on Pin 12) which always tries to hold the actual voltage at the value of the set voltages. The amplifier has a transmittance of typically $1000\text{ }\mu\text{A/V}$ and a bipolar current source output on Pin 12 which operates with typically $\pm 110\text{ }\mu\text{A}$. The amplification and frequency response are determined by R_7 , C_7 , C_8 and R_{11} (can be left out). For open loop operation, C_4 , C_5 , R_6 , R_7 , C_7 , C_8 and R_{11} can be omitted. Pin 10 should be connected with Pin 12 and Pin 8 with Pin 2. The phase angle of the triggering pulse can be adjusted using the voltage on Pin 11. An internal limitation circuit prevents the voltage on Pin 12 from becoming more negative than $V_{16} + 1\text{ V}$.

Load Limitation

The load limitation, with standard circuitry, provides absolute protection against overloading of the motor. The function of the load limiting takes account of the fact that motors operating at higher speeds can safely withstand large power dissipations than at lower speeds due to the increased action of the cooling fan. Similarly, considerations have been made for short term overloads for the motor which are, in practice, often required. These functions are not damaging and can be tolerated.

In each positive half-cycle, the circuit measures via R_{10} the load current on Pin 14 as a potential drop across R_8 and produces a current proportional to the voltage on Pin 14. This current is available on Pin 15 and is integrated by C_9 . If, following high current amplitudes or a large phase angle for current flow, the voltage on C_9 exceeds an internally set threshold of approx. 7.3 V

(reference voltage Pin 16) then a latch is set and the load limiting is turned on. A current source (sink) controlled by the control voltage on Pin 15 now draws current from Pin 12 and lowers the control voltage on Pin 12 so that the phase angle α is increased to α_{max} .

The simultaneous reduction of the phase angle during which current flows causes firstly: a reduction of the rotational speed of the motor which can even drop to zero if the angular momentum of the motor is excessively large, and secondly: a reduction of the potential on C_9 which in turn reduces the influence of the current sink on Pin 12. The control voltage can then increase again and bring down the phase angle. This cycle of action sets up a "balanced condition" between the "current integral" on Pin 15 and the control voltage on Pin 12.

Apart from the amplitude of the load current and the time during which current flows, the potential on Pin 12 and hence the rotational speed also affects the function of the load limiting. A current proportional to the potential on Pin 10 gives rise to a voltage drop across R_{10} , via Pin 14, so that the current measured on Pin 14 is smaller than the actual current through R_8 .

This means that higher rotational speeds and higher current amplitudes lead to the same current integral. Therefore, at higher speeds, the power dissipation must be greater than that at lower speeds before the internal threshold voltage on Pin 15 is exceeded. The effect of speed on the maximum power is determined by the resistor R_{10} and can therefore be adjusted to suit each individual application.

If, after the load limiting has been turned on, the momentum of the load sinks below the "o-momentum" set using R_{10} , then V_{15} will be reduced. V_{12} can then increase again so that the phase angle is reduced. A smaller phase angle corresponds to a larger momentum of the motor and hence the motor runs up - as long as this is allowed by the load momentum. For an already rotating machine, the effect of rotation on the measured "current integral" ensures that the power dissipation is able to increase with the rotational speed. The result is: a current controlled acceleration run-up., which ends in a small peak of acceleration when the set point is reached. The latch of the load limiting is simultaneously reset. The speed of the motor is then again under control and it is capable of carrying its full load. The above mentioned peak of acceleration depends upon the ripple of actual speed voltage. A large amount of ripple also leads to a large peak of acceleration.

The measuring resistor R_8 should have a value which ensures that the amplitude of the voltage across it does not exceed 600 mV .

Design Hints

Practical trials are normally needed for the exact determination of the values of the relevant components in the load limiting. To make this evaluation easier, the

following table shows the effect of the circuitry on the important parameters of the load limiting and summarises the general tendencies.

Parameters	Component affected		
	R ₁₀	R ₉	C ₉
P _{max}	increases	decreases	n.e.
P _{min}	increases	decreases	n.e.
P _{max} / min	increases	n.e.	n.e.
t _d	n.e.	decreases	increases
t _r	n.e.	increases	increases

P_{max} – maximum continuous power dissipation
 P_{min} – power dissipation with no rotation
 t_d – operation delay time
 t_r – recovery time
 n.e. – no effect

$P_1 = f_{(n)} n \neq 0$
 $P_1 = f_{(n)} n = 0$

Pulse Output Stage

The pulse output stage is short circuit protected and can typically deliver currents of 125 mA. For the design of smaller triggering currents, the function $I_{GT} = f(R_{GT})$ has been given in the data sheets in the appendix.

Automatic Retriggering

The variable automatic retriggering prevents half cycles without current flow, even if the triac is turned off earlier e.g. due to a collector which is not exactly centered (brush lifter) or in the event of unsuccessful triggering. If it is necessary, another triggering pulse is generated after a time lapse which is determined by the repetition rate set by resistance between Pin 5 and Pin 3 (R₅₋₃). With the maximum repetition rate (Pin 5 directly connected to Pin 3), the next attempt to trigger comes after a pause of 4.5 t_p and this is repeated until either the triac fires or the half-cycle finishes. If Pin 5 is connected, then only one trigger pulse per half-cycle is generated. Because the value of R₅₋₃ determines the charging current of C₂, any repetition rate set using R₅₋₃ is only valid for a fixed value of C₂.

General Hints and Explanation of Terms

To ensure safe and trouble-free operation, the following points should be taken into consideration when circuits are being constructed or in the design of printed circuit boards.

- The connecting lines from C₂ to Pin 7 and Pin 2 should be as short as possible: The connection to Pin 2 should not carry any additional high current such as the load current. When selecting C₂, a low temperature coefficient is desirable.
- The common (earth) connections of the set-point generator, the tachogenerator and the final interference suppression capacitor C₄ of the f/V converter should not carry load current.
- The tachogenerator should be mounted without influence by strong stray fields from the motor.
- The connections from R₁₀ and C₅ should be as short as possible.

To achieve a high noise immunity, a maximum ramp voltage of 6 V should be used.

The typical resistance R_φ can be calculated from I_φ as follows:

$$R_{\phi} \text{ (k}\Omega\text{)} = \frac{T(\text{ms}) \times 1.13(\text{V}) \times 10^3}{C/\text{nF} \times 6(\text{V})}$$

T = Period duration for mains frequency
(10 ms at 50 Hz)

C_φ = Ramp capacitor, max. ramp voltage 6 V
and constant voltage drop at R_φ = 1.13 V.

A 10% lower value of R_φ (under worst case conditions) is recommended.

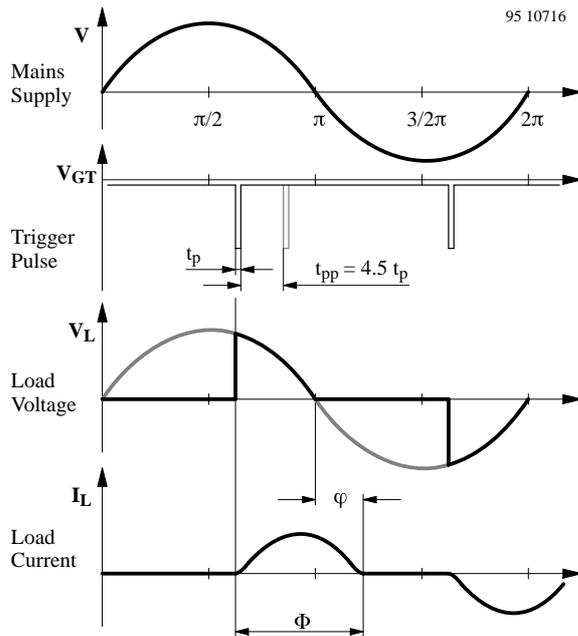


Figure 6. Explanation of terms in phase relationship

Design Calculations for Mains Supply

The following equations can be used for the evaluation of the series resistor R_1 for worst case conditions:

$$R_{1\max} = 0.85 \frac{V_{M\min} - V_{S\max}}{2 I_{\text{tot}}} \quad R_{1\min} = \frac{V_M - V_{S\min}}{2 I_{S\max}}$$

$$P_{(R1\max)} = \frac{(V_{M\max} - V_{S\min})^2}{2 R_1}$$

where:

V_M = Mains voltage

V_S = Supply voltage on Pin 3

I_{tot} = Total DC current requirement of the circuit
 $= I_S + I_p + I_x$

$I_{S\max}$ = Current requirement of the IC in mA

I_p = Average current requirement of the triggering pulse

I_x = Current requirement of other peripheral components

R_1 can be easily evaluated from the figures 20 to 22.

Absolute Maximum Ratings

Reference point Pin 2, unless otherwise specified

Parameters	Symbol	Value	Unit
Current requirement $t \leq 10 \mu\text{s}$	Pin 3 $-I_S$	30	mA
	$-i_s$	100	
Synchronization current $t < 10 \mu\text{s}$ $t < 10 \mu\text{s}$	Pin 1 I_{syncI}	5	mA
	Pin 17 I_{syncV}	5	
	Pin 1 $\pm i_I$	35	
	Pin 17 $\pm i_I$	35	
f/V converter Pin 8			
Input current $t < 10 \mu\text{s}$	I_I	3	mA
	$\pm i_I$	13	
Load limiting Pin 14			
Limiting current, neg. half wave $t < 10 \mu\text{s}$	I_I	5	mA
		35	
Input voltage	Pin 14 $\pm V_i$	1	V
	Pin 15 $-V_I$	$ V_{16} \text{ to } 0$	
Phase control			
Input voltage	Pin 12 $-V_I$	0 to 7	V
Input current	Pin 12 $\pm I_I$	500	μA
	Pin 6 $-I_I$	1	mA
Soft-start			
Input voltage	Pin 13 $-V_I$	$ V_{16} \text{ to } 0$	V
Pulse output			
Reverse voltage	Pin 4 V_R	$V_S \text{ to } 5$	V
Pulse blocking			
Input voltage	Pin 18 $-V_I$	$ V_{16} \text{ to } 0$	V
Amplifier			
Input voltage	Pin 11 V_I	0 to V_S	V
	Pin 9 open Pin 10 $-V_I$	$ V_{16} \text{ to } 0$	
Reference voltage source			
Output current	Pin 16 I_o	7.5	mA
Storage temperature range	T_{stg}	-40 to +125	$^{\circ}\text{C}$
Junction temperature	T_j	125	$^{\circ}\text{C}$
Ambient temperature range	T_{amb}	-10 to +100	$^{\circ}\text{C}$

Thermal Resistance

Parameters	Symbol	Maximum	Unit
Junction ambient DIP18 SO16 on p.c. SO16 on ceramic	R_{thJA}	120	K/W
		180	
		100	

Electrical Characteristics

$-V_S = 13.0 \text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, reference point Pin 2, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for mains operation	Pin 3	$-V_S$	13.0		V_{Limit}	V
Supply voltage limitation	$-I_S = 4 \text{ mA}$ $-I_S = 30 \text{ mA}$ Pin 3	$-V_S$ $-V_S$	14.6 14.7		16.6 16.8	V
DC current requirement	$-V_S = 13.0 \text{ V}$ Pin 3	I_S	1.2	2.5	3.0	mA
Reference voltage source	$-I_L = 10 \mu\text{A}$ $-I_L = 5 \text{ mA}$ Pin 16	$-V_{\text{Ref}}$	8.6 8.3	8.9	9.2 9.1	V
Temperature coefficient	Pin 16	$-TC_{V_{\text{Ref}}}$		0.5		mV/K
Voltage monitoring						
Turn-on threshold	Pin 3	$-V_{\text{SON}}$	11.2	13.0		V
Turn-off threshold	Pin 3	$-V_{\text{SOFF}}$	9.9	10.9		V
Phase control currents						
Synchronization current	Pin 1	$\pm I_{\text{syncI}}$	0.35		2.0	mA
	Pin 17	$\pm I_{\text{syncV}}$	0.35		2.0	
Voltage limitation	$\pm I_L = 5 \text{ mA}$ Pins 1 and 17	$\pm V_I$	1.4	1.6	1.8	V
Reference ramp, figure 7						
Charge current	$I_7 = f(R_6)$; $R_6 = 50 \text{ k to } 1 \text{ M}\Omega$ Pin 7	I_7	1	20		μA
R_φ -reference voltage	$\alpha \geq 180^\circ\text{C}$ Pins 6 and 3	$V_{\varphi\text{Ref}}$	1.06	1.13	1.18	V
Temperature coefficient	Pin 6	$TC_{V_{\varphi\text{Ref}}}$		0.5		mV/K
Pulse output, figure 18						
	Pin 4					
Output pulse current	$R_{\text{GT}} = 0$, $V_{\text{GT}} = 1.2 \text{ V}$	I_o	100	155	190	mA
Reverse current		I_{or}		0.01	3.0	μA
Output pulse width	$C_\varphi = 10 \text{ nF}$	t_p		80		μs
Amplifier						
Common mode signal range	Pins 10 and 11	$V_{10, 11}$	V_{16}		-1	V
Input bias current	Pin 11	I_{IO}		0.01	1	μA
Input offset voltage	Pins 10 and 11	V_{10}		10		mV
Output current	Pin 12	$-I_o$ $+I_o$	75 88	110 120	145 165	μA
Short circuit forward, transmittance	Figure 14 $I_{12} = f(V_{10-11})$ Pin 12	Y_f		1000		$\mu\text{A/V}$
Pulse blocking, tachometer monitoring						
	Pin 18					
Logic-on		$-V_{\text{TON}}$	3.7	1.5		V
Logic-off		$-V_{\text{TOFF}}$		1.25	1.0	
Input current	$V_{18} = V_{\text{TOFF}} = 1.25 \text{ V}$ $V_{18} = V_{16}$	I_i	14.5	0.3	1	μA
Output resistance		R_o	1.5	6	10	k Ω

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Frequency to voltage converter Pin 8						
Input bias current		I_{IB}		0.6	2	μA
Input voltage limitation	Figure 13 $I_I = -1 \text{ mA}$ $I_I = +1 \text{ mA}$	$-V_I$ $+V_I$	660 7.25		750 8.05	mV V
Turn-on threshold		$-V_{TON}$		100	150	mV
Turn-off threshold		$-V_{TOFF}$	20	50		mV
Charge amplifier						
Discharge current	Figure 2 $C_5 = 1 \text{ nF}$, Pin 9	I_{dis}		0.5		mA
Charge transfer voltage	Pins 9 to 16	V_{ch}	6.50	6.70	6.90	V
Charge transfer gain	I_{10}/I_9 Pins 9 and 10	G_i	7.5	8.3	9.0	
Conversion factor	Figure 2 $C_5 = 1 \text{ nF}$, $R_6 = 100 \text{ k}\Omega$	K		5.5		mV/Hz
Output operating range	Pins 10 to 16	V_O		0-6		V
Linearity				± 1		%
Soft-start , figures 8, 9, 10, 11, 12 f/v-converter non-active						
Starting current	$V_{13} = V_{16}$, $V_8 = V_2$ Pin 13	I_O	20	45	55	μA
Final current	$V_{13} = 0.5$ Pin 13		50	85	130	
f/v-converter active						
Starting current	$V_{13} = V_{16}$ Pin 13	I_O	2	4	7	μA
Final current	$V_{13} = 0.5$		30	55	80	μA
Discharge current	Restart pulse Pin 13	I_O	0.5	3	10	mA
Automatic retriggering , figure 19 Pin 5						
Repetition rate	$R_{5-3} = 0$	t_{pp}	3	4.5	6	t_p
	$R_{5-3} = 15 \text{ k}\Omega$			20		
Load limiting , figures 15, 16, 17 Pin 14						
Operating voltage range	Pin 14	V_I	-1.0		1.0	V
Offset current	$V_{10} = V_{16}$ Pin 14	I_O	5		12	μA
	$V_{14} = V_2$ via $1 \text{ k}\Omega$ Pin 15-16			0.1	1.0	
Input current	$V_{10} = 4.5 \text{ V}$ Pin 14	I_I	60	90	120	
Output current	$V_{14} = 300 \text{ mV}$ Pin 15-16	I_O	110		140	
Overload ON	Pin 15-16	V_{TON}	7.05	7.4	7.7	V

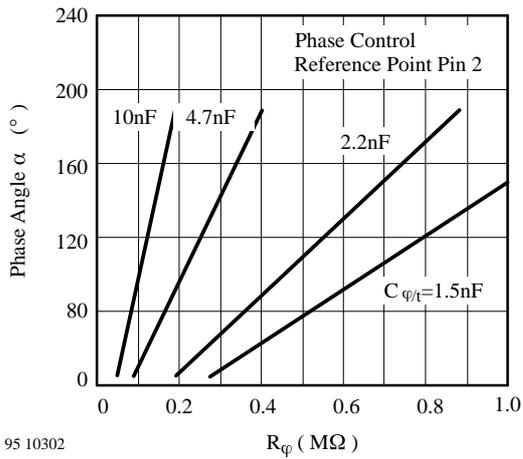


Figure 7.

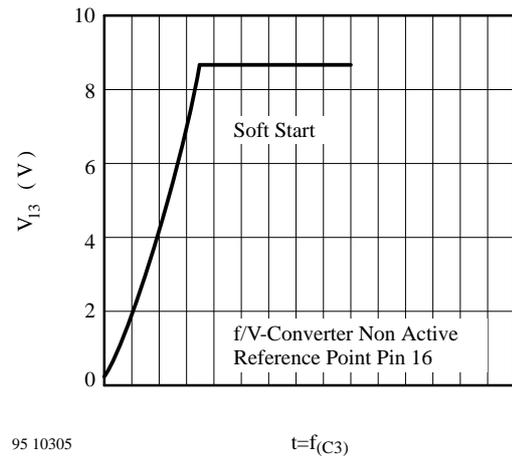


Figure 10.

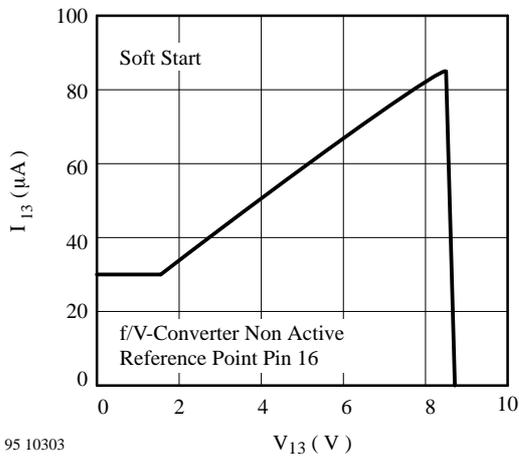


Figure 8.

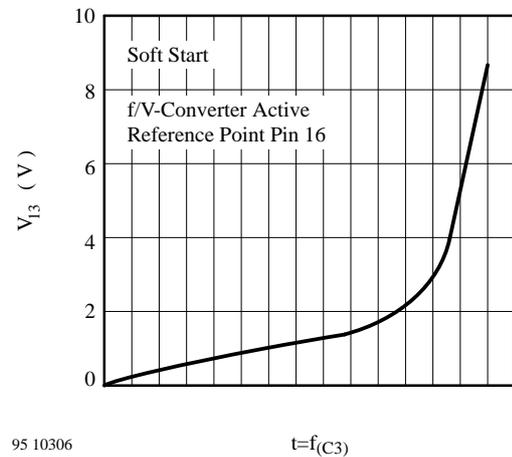


Figure 11.

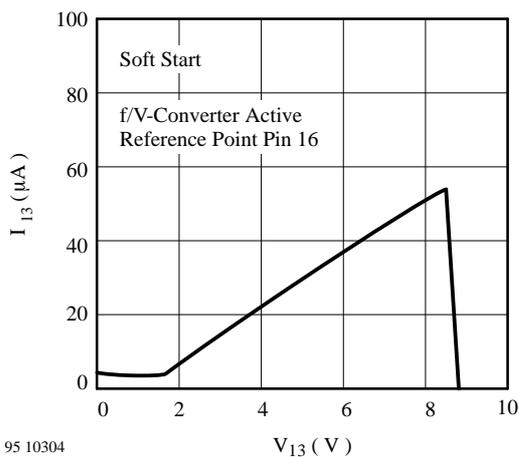


Figure 9.

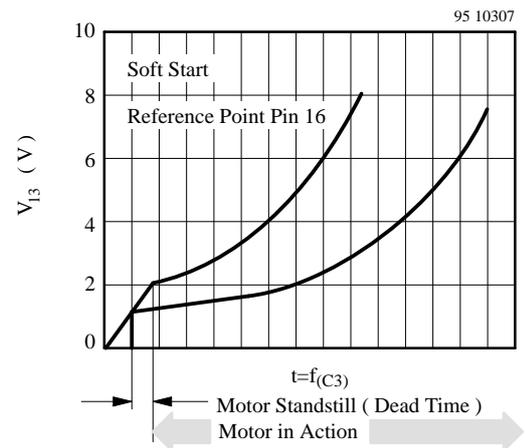


Figure 12.

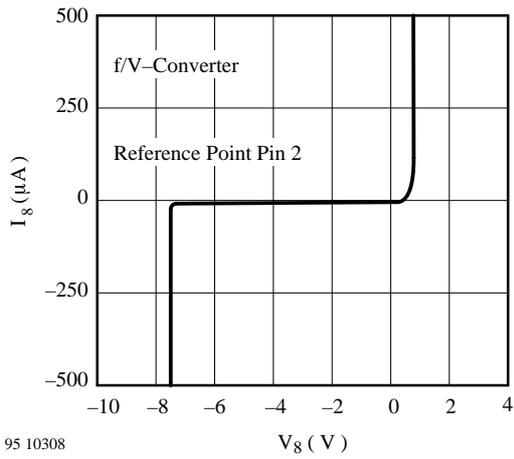


Figure 13.

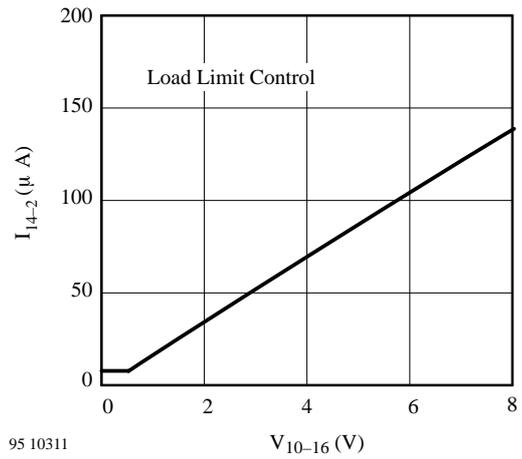


Figure 16.

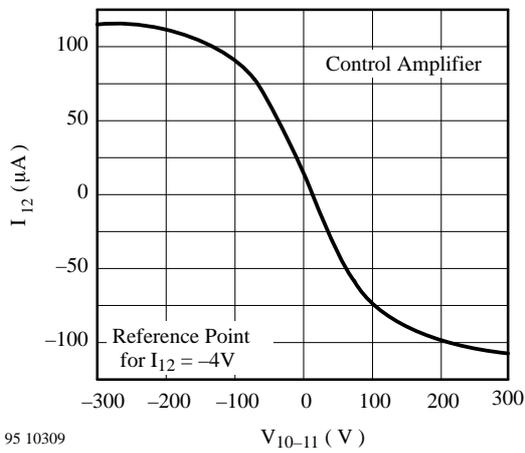


Figure 14.

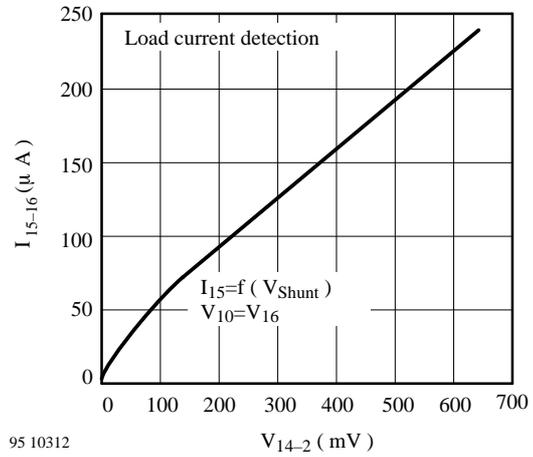


Figure 17.

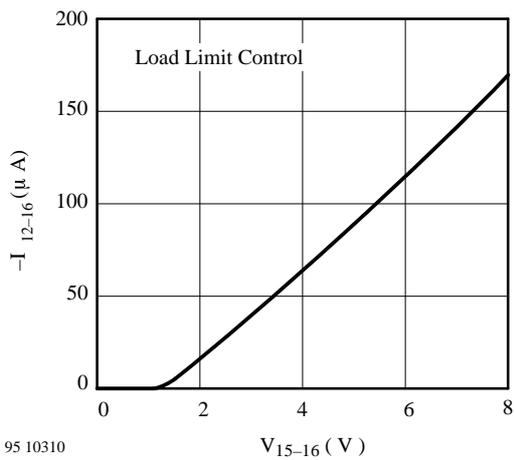


Figure 15.

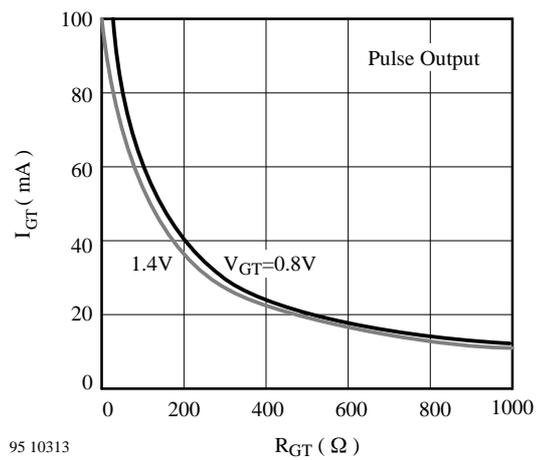


Figure 18.

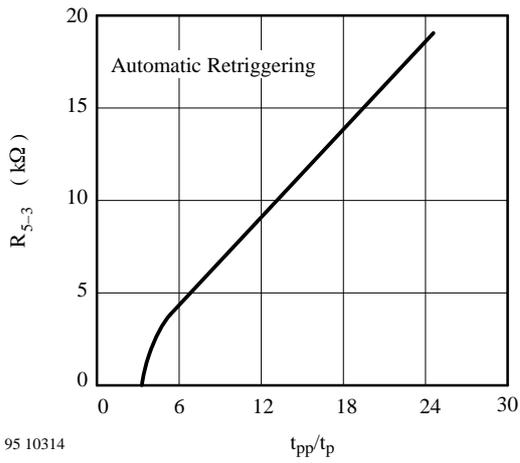


Figure 19.

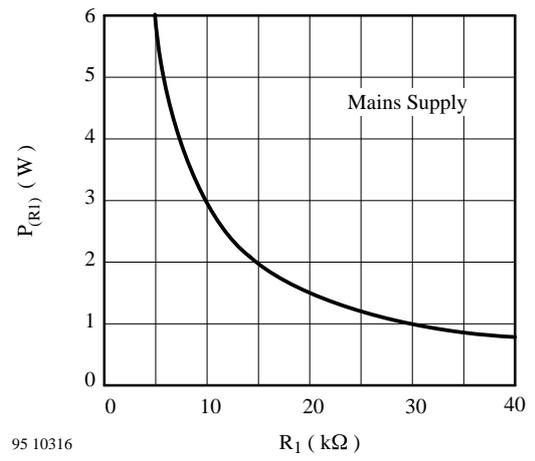


Figure 21.

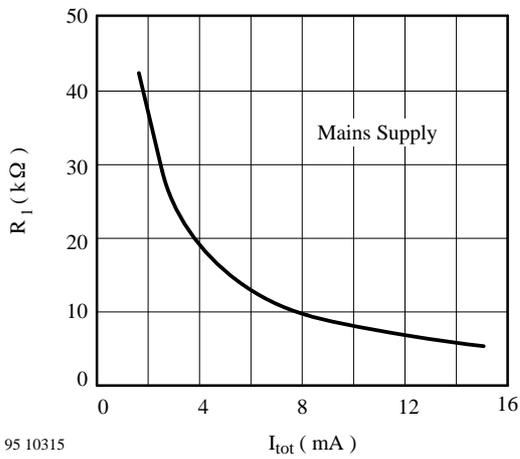


Figure 20.

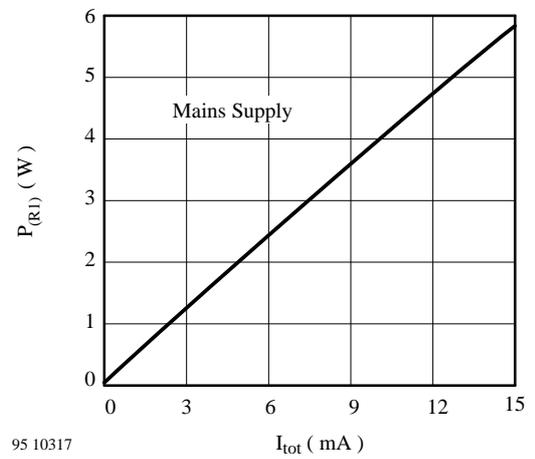


Figure 22.

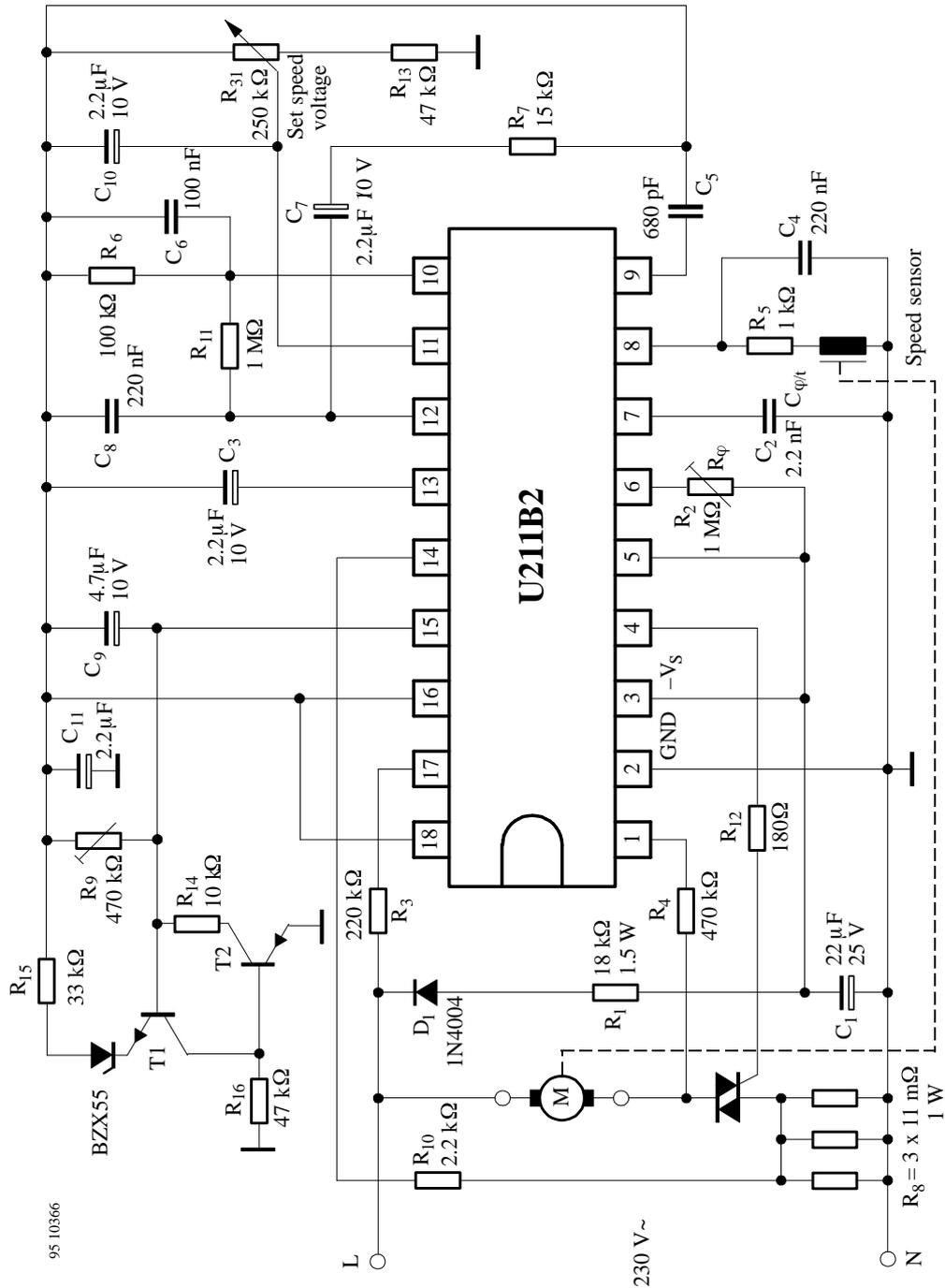


Figure 24. Speed control, automatic retriggering, load switch-off, soft-start

The maximum load regulation shows the principle in the same speed dependency as the original version (see figure 2). When reaching the maximum load, the control unit is turned to α_{max} , adjustable with R_2 . Then only I_O flows. This function is effected by the thyristor, formed by T_1 and T_2 which ignites as soon as the voltage at Pin 15 reaches ca. 6.8 V (Reference point Pin 16). The potential

at Pin 15 is lifted and kept by R_{14} over the internally operating threshold whereby the maximum load regulation starts and adjusts the control unit constantly to α_{max} (I_O), inspite of a reduced load current. The motor shows that the circuit is still in operation by a quiet buzzing noise.

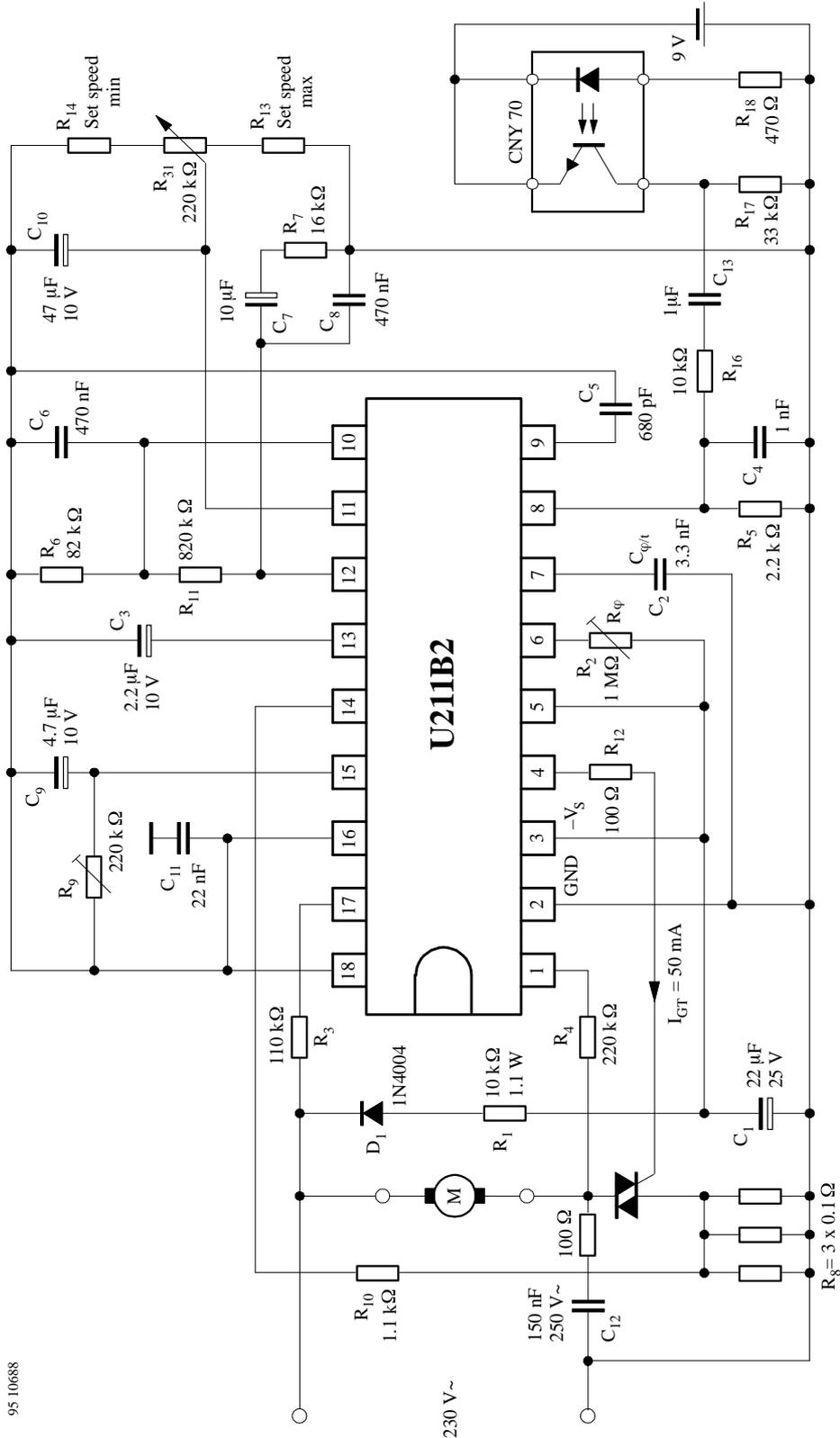


Figure 27. Speed control, max. load control with reflective opto coupler CNY70 as emitter

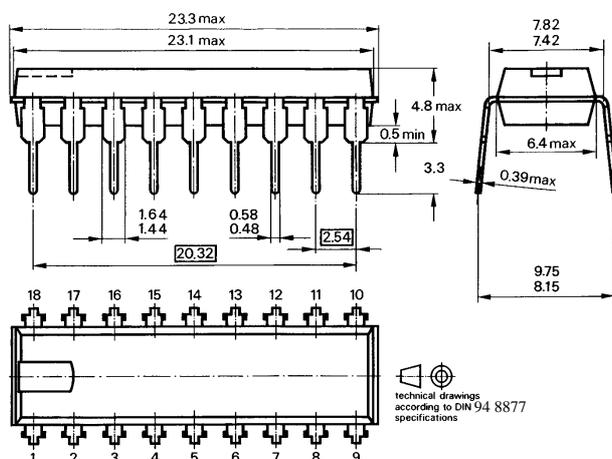
The circuit is designed as a speed control on the reflection-coupled principle with 4 periods per revolution and a max. speed of 30.000 rpm. The separation of the coupler from the rotating aperture should be 1 mm approximately. In this experimental circuit, the power supply for the coupler was provided externally because of the relatively high current consumption.

Instructions for adjusting:

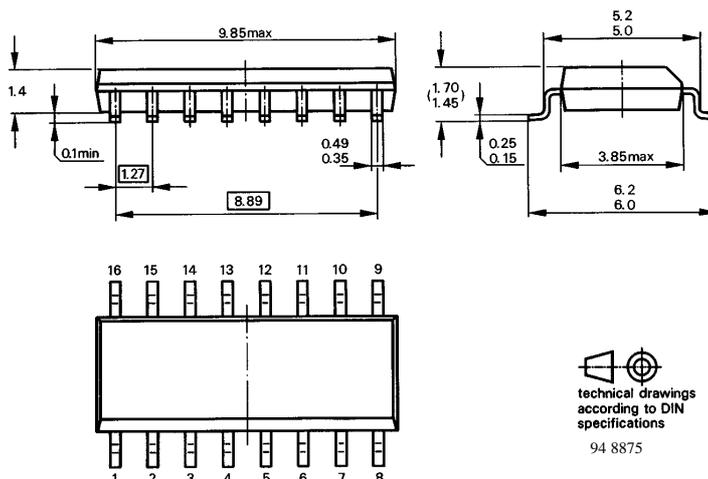
- In the initial adjustment of the phase-control circuit, R_2 should be adjusted so that when $R_{14} = 0$ and R_{31} are in min. position, the motor just turns.
- The speed can now be adjusted as desired by means of R_{31} between the limits determined by R_{13} and R_{14} .
- The switch-off power of the limit load control can be set by R_9 . The lower R_9 , the higher the switch-off power.

Dimensions in mm

Package: DIP18 – U211B2



Package: SO16 – U211B3



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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