

D/644A/6 June 2000

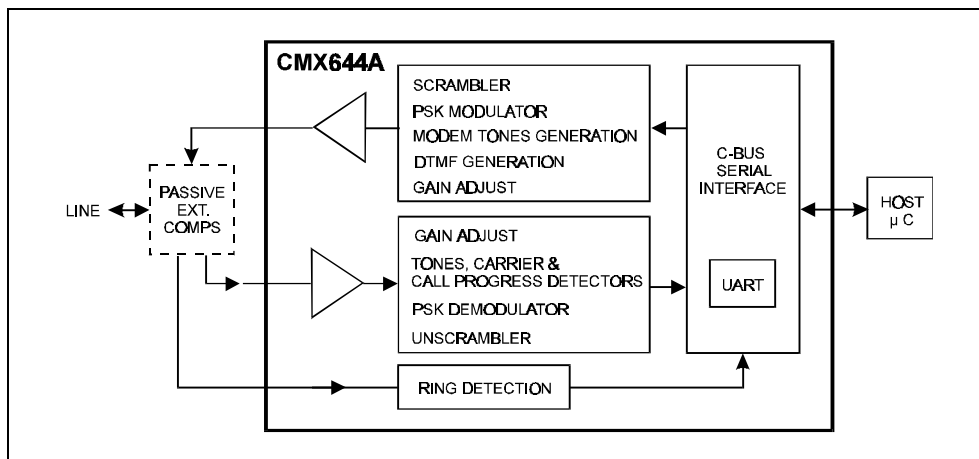
Provisional Issue

### Features

- V.22/Bell 212A Compatible Modem
- Integrated DTMF Encoder
- Call Progress/Accurate Answer Tone Detection
- Line Reversal and Ringing Detector
- Low Power Operation (2.7V)
- Fully Integrated UART Functions

### Applications

- Telephone Telemetry Systems
- Remote Utility Meter Reading
- Security Systems/Cash Terminals
- Industrial Control Systems
- Pay-Phones
- Cable TV Set-Top Boxes



### 1.1 Brief Description

The CMX644A V.22 modem is intended for use in any telephone based information and telemetry system with low power requirements. Using V.22 signalling, fast call set up times and robust error resistant transmission can be implemented by efficient low power circuits. The circuit can operate at 1200b/s full duplex over 2-or 4-wire circuits. Control of the device is via a simple high speed serial bus and data may be optionally formatted by the on-chip UART. This allows easy interfacing to a host  $\mu$ Controller. The data transmitted and received by the modem is also transferred over the same high speed serial bus. In addition to V.22, support is included to meet the Bell 212A standard. The integrated DTMF encoder can be used as part of the dial out function. All 16 DTMF combinations are available along with a single tone 'melody' mode.

The answer tone generator/detector and call progress tone detectors included on the CMX644A make the set-up of a telephone call a simple matter for the host  $\mu$ Controller.

In many data collection and telemetry systems low power consumption is important. The CMX644A features a 'Zero Power' standby mode. Whilst in standby, the device can still detect a ringing voltage or line voltage reversal. The CMX644A can operate on a supply voltage between 3.0V and 5.5V across the full temperature range of -40°C to +85°C. A low impedance pull down output is provided for a hook relay. The CMX644A is pin compatible with the CMX624 V23/Bell 202 modem also from CML.

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## 1.2 Block Diagram

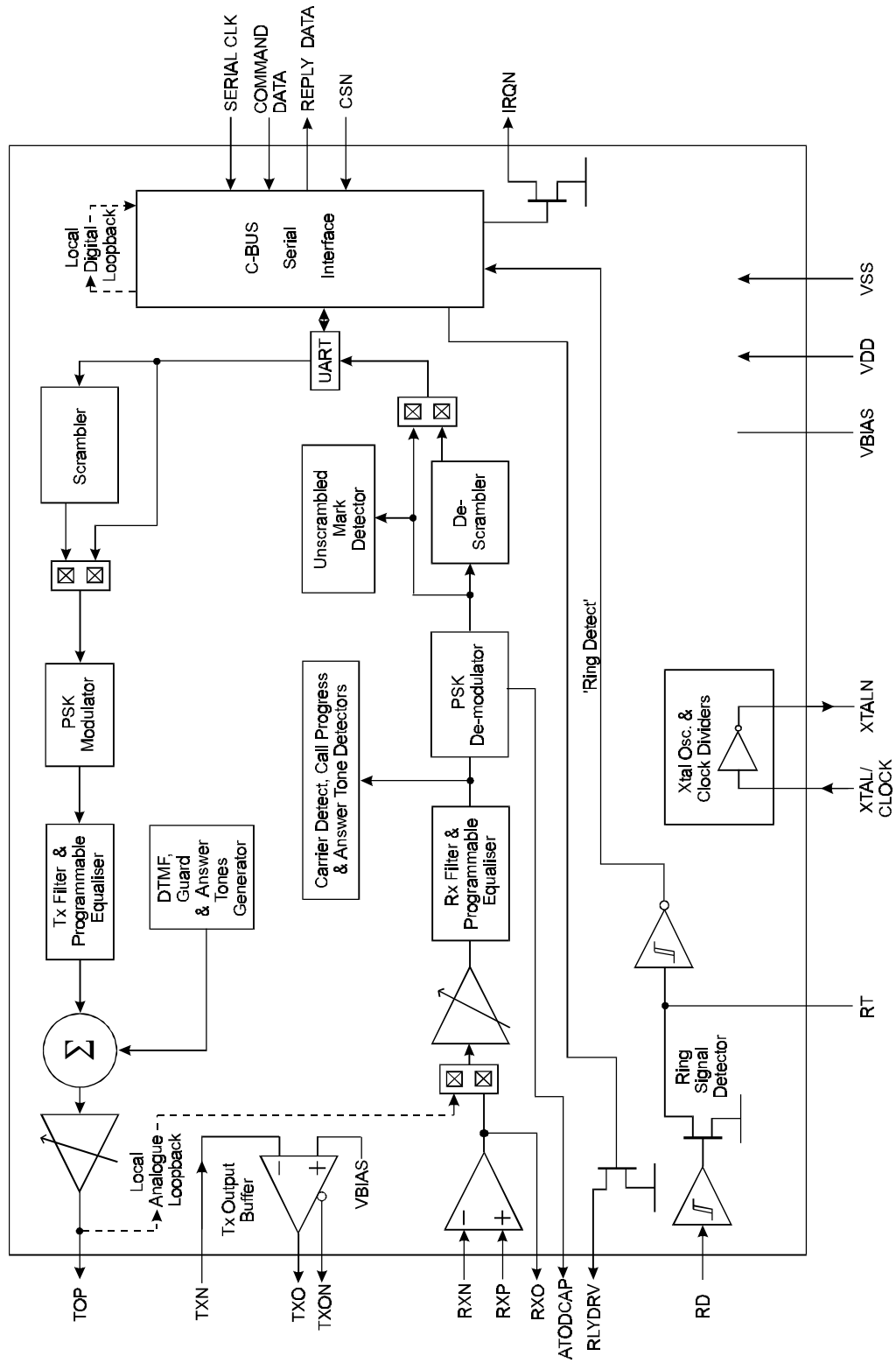


Figure 1 Block Diagram

### 1.3 Signal List

CMX644A D2/D5/P4	Signal		Description
Pin No.	Name	Type	
1	XTALN	O/P	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	I/P	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	I/P	The 'C-BUS' serial clock input. This clock, produced by the $\mu$ Controller, is used for the transfer timing of commands to and from the device.
4	COMMAND DATA	I/P	The 'C-BUS' serial data input from the $\mu$ Controller. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronised to the SERIAL CLOCK.
5	REPLY DATA	T/S	The 'C-BUS' serial data output to the $\mu$ Controller. The transmission of REPLY DATA bytes is synchronised to the SERIAL CLOCK under control of the CSN input. This 3-state output is held at high impedance when not sending data to the $\mu$ Controller.
6	CSN	I/P	The 'C-BUS' data loading control function: this input is provided by the $\mu$ Controller. Data transfer sequences are initiated, completed or aborted by the CSN signal.
7	IRQN	O/P	This output indicates an interrupt condition to the $\mu$ Controller by going to a logic '0'. This is a 'wire-ORable' output, enabling the connection of up to 8 peripherals to 1 interrupt port on the $\mu$ Controller. This pin has a low impedance pulldown to logic '0' when active and a high impedance when inactive. An external pull-up resistor is required.
8	TOP	O/P	The output of the transmit gain control.
9	TXO	O/P	The output of the line driver amplifier.
10	TXN	I/P	The inverting input to the line driver amplifier.
11	TXON	O/P	The inverted output of the line driving amplifier. Pins TXO and TXON provide symmetrical outputs for use with a balanced load to give sufficient Tx line signal levels even at low $V_{DD}$ .

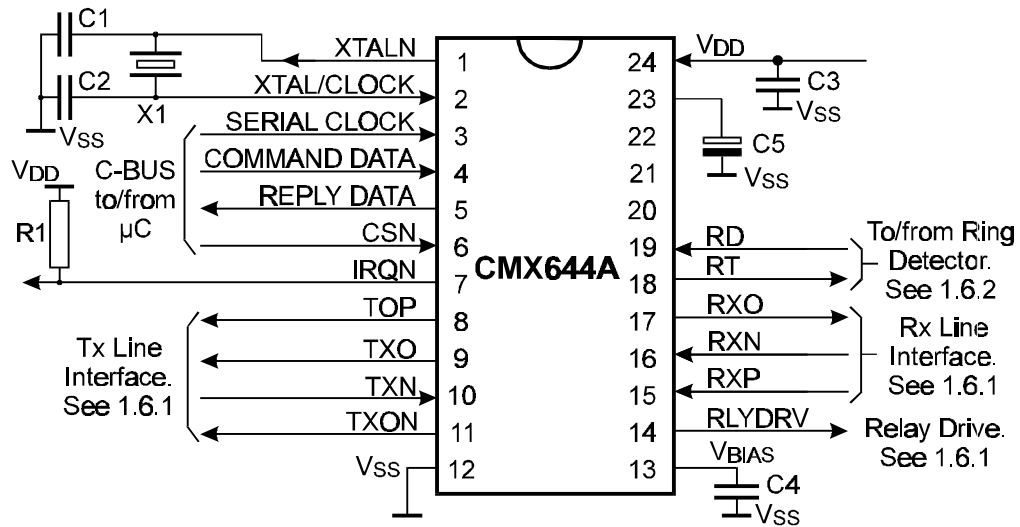
### 1.3 Signal List (Continued)

CMX644A D2/D5/P4	Signal		Description
Pin No.	Name	Type	
12	V <sub>SS</sub>	POWER	The negative supply rail (ground).
13	V <sub>BIAS</sub>	O/P	A bias line for the internally circuitry, held at ½ V <sub>DD</sub> . This pin must be decoupled by a capacitor mounted close to the device pins.
14	RLYDRV	O/P	An open-drain output for controlling a relay.
15	RXP	I/P	The non-inverting input of the receive op-amp.
16	RXN	I/P	The inverting input of the receive op-amp.
17	RXO	O/P	The output of the receive op-amp.
18	RT	BI	Open-drain output and Schmitt trigger input forming part of the Ring or Line Polarity Reversal detector. An external resistor to V <sub>DD</sub> and a capacitor to V <sub>SS</sub> should be connected to RT to filter and extend the RD input signal.
19	RD	I/P	Input to the Ring or Line Polarity Reversal Detector.
20, 21, 22	-	N/C	No connections should be made to these pins.
23	ATODCAP	O/P	The reference voltage for the internal A to D of the receiver. This pin must be decoupled by a capacitor mounted close to the device pins.
24	V <sub>DD</sub>	POWER	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be decoupled to V <sub>SS</sub> by a capacitor mounted close to the device pins.

**Notes:** I/P = Input  
 O/P = Output  
 N/C = No (external) Connections  
 B/I = Bidirectional  
 T/S = Tristate

This device is capable of detecting and decoding small amplitude signals. It is recommended that the printed circuit board is laid out with a ground plane in the CMX644A area to provide a low impedance connection between the V<sub>SS</sub> pin and the V<sub>DD</sub> and V<sub>BIAS</sub> decoupling capacitors. The receive path should be protected as much as possible from extraneous signals.

### 1.4 External Components



R1	100kΩ *	C1, C2	18pF
X1	3.6864MHz, 7.372800MHz or 11.0592MHz	C3, C4	0.1µF
		C5	1µF

Resistors ±1%, capacitors ±20% unless otherwise stated.

\* R1 should be selected so that the IRQN pin has returned to its normal (high) state before the CSN pin goes high.

**Figure 2 Recommended External Components for Typical Application**

#### Notes on Xtal Osc and Clock Dividers

Frequency and timing accuracy of the CMX644A is determined by the clock present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL/CLOCK input. If the clock is supplied from an external source, C1, C2 and X1 should not be fitted.

The on-chip oscillator is turned off in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a rise in the supply current drawn by CMX644A.

## 1.5 General Description

### 1.5.1 'C-BUS' Interface

This block provides for the transfer of data and control or status information between the CMX644A's internal registers and the  $\mu\text{C}$  over the 'C-BUS' serial bus. Each transaction, see Figure 3, consists of a single Register Address byte sent from the  $\mu\text{C}$  which may be followed by a single data byte sent from the  $\mu\text{C}$  to be written into one of the CMX644A's Write Only Registers, or a single byte of data read out from one of the CMX644A's Read Only Registers.

Data sent from the  $\mu\text{C}$  on the Command Data line is clocked into the CMX644A on the rising edge of the Serial Clock input. Reply Data sent from the CMX644A to the  $\mu\text{C}$  is valid when the Serial Clock is high. The interface is compatible with the most common  $\mu\text{C}$  serial interfaces such as SCI, SPI and Microwire, and may also be easily implemented with general purpose  $\mu\text{C}$  I/O pins controlled by a simple software routine. See section 1.7.1 and Figure 9 for detailed 'C-BUS' timing requirements.

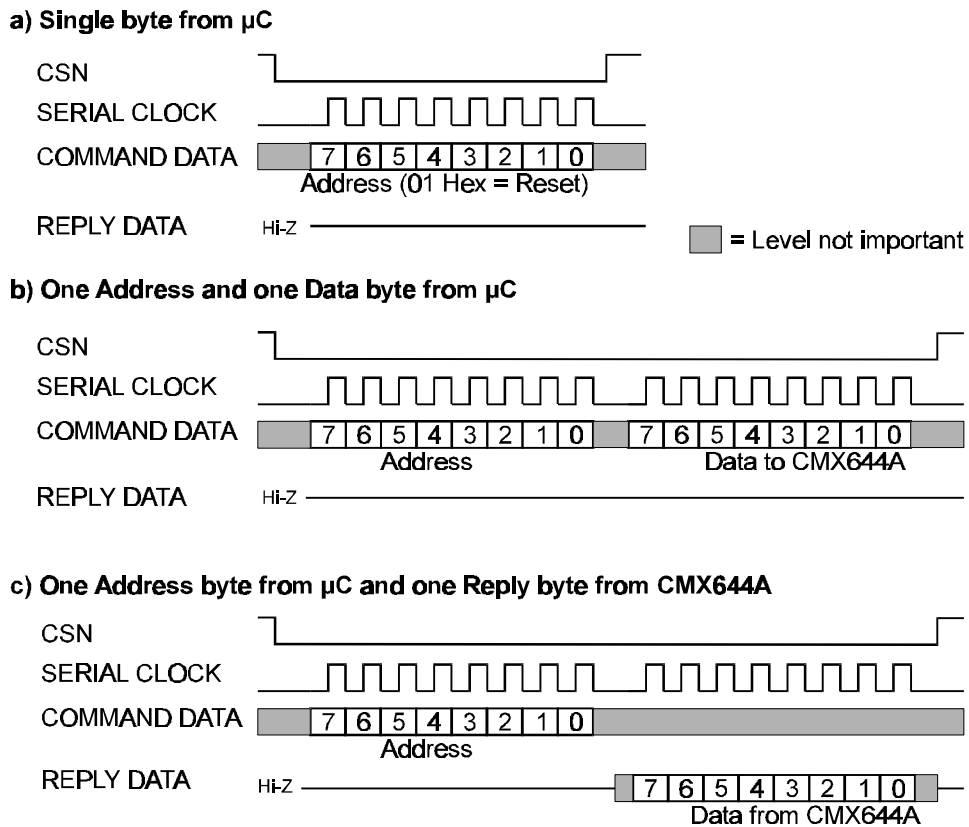


Figure 3 'C-BUS' Transactions

## 1.5.2 UART

This block connects the  $\mu\text{C}$ , via the 'C-BUS' interface, to the received data from the PSK Demodulator and to the transmit data input to the PSK Modulator.

As part of this function, the block can be programmed to convert data to be transmitted from 7 or 8-bit bytes to asynchronous data characters, adding Start and Stop bits and - optionally - a parity bit to the data before passing it to the PSK Modulator. Similarly, in the receive direction it can extract data bits from asynchronous characters coming from the PSK Demodulator, stripping off the Start and Stop bits and performing an optional Parity check on the received data before passing the result over the 'C-BUS' to the  $\mu\text{C}$ . Bits 0-5 of the UART MODE Register control the number of Stop and Data bits and the Parity options for both receive and transmit directions.

Data to be transmitted should be loaded by the  $\mu\text{C}$  into the TX DATA BYTE Register when the Tx Data Ready bit (bit 1) of the FLAGS Register goes high. It will then be treated by the Tx UART block in one of two ways, depending on the setting of bit 5 of the UART MODE Register:

If bit 5 of the UART MODE Register is '0' ('Sync' mode) then the 8 bits from the TX DATA BYTE Register will be transmitted sequentially LSB (D0) first.

If bit 5 of the UART MODE Register is '1' ('Async' mode) then the 7 or 8 bits will be transmitted as asynchronous data characters according to the following format:

One Start bit (Space).

7 or 8 Data bits from the TX DATA BYTE Register (D0-D6 or D0-D7) as determined by bit 0 of the UART MODE Register. LSB (D0) transmitted first.

Optional Parity bit (even or odd parity) as determined by bits 1 and 2 of the UART MODE Register.

Zero, One or Two Stop bits (Mark) as determined by bits 3 and 4 of the UART MODE Register.

In both cases data will only be transmitted if bit 6 of the TX PSK MODE Register is set to '1'.

Failure to load the TX DATA BYTE Register with a new value when required will result in bit 2 (TX DATA UNDERFLOW) of the FLAGS Register being set to '1' and a continuous Mark ('1') signal will then be transmitted until a new value is loaded into TX DATA BYTE Register.

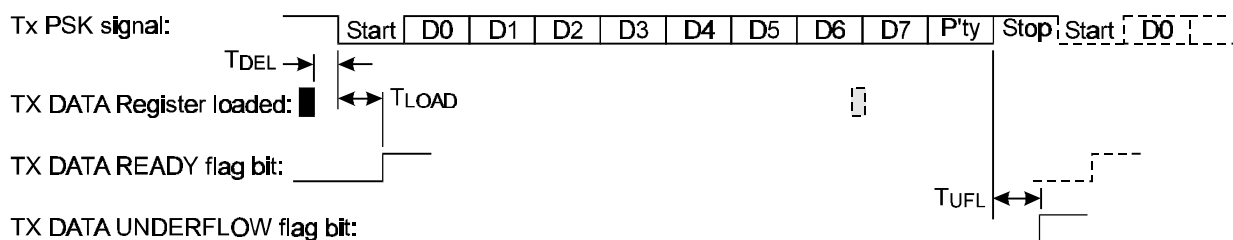


Figure 4a Transmit UART Function (Async)



Received data from the PSK Demodulator goes into the receive part of the UART block, where it is handled in one of two ways depending on the setting of bit 5 of the UART MODE Register:

If bit 5 of the UART MODE Register is '0' ('Sync' mode) then the receive part of the UART block will simply take 8 consecutive bits from the Demodulator and transfer them to the RX DATA BYTE Register (the first bit going into the D0 position).

If bit 5 of the UART MODE Register is '1' ('Async' mode) then the received data output of the PSK Demodulator is treated as asynchronous characters each comprising:

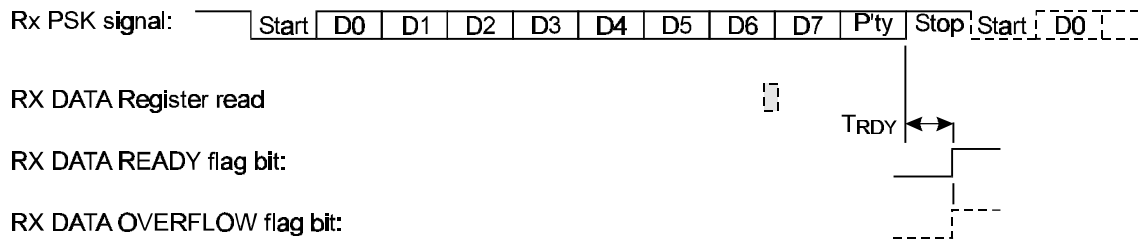
A Start bit (Space).

7 or 8 Data bits as determined by bit 0 of the UART MODE Register. These bits will be placed into the RX DATA BYTE Register with the first bit received going into the D0 position.

An optional Parity bit as determined by bits 1 and 2 of the UART MODE Register. If Parity is enabled (bit 2 of the UART MODE Register = '1') then bit 7 of the FLAGS Register will be set to '1' if the received parity is incorrect.

Any number of Stop bits (Mark).

Bit 3 (RX DATA READY) of the FLAGS Register will be set to '1' every time a new received value is loaded into the RX DATA BYTE Register. If the previous contents of the RX DATA BYTE Register had not been read out over the 'C-BUS' before the new value is loaded from the UART then bit 4 (RX DATA OVERFLOW) of the FLAGS Register will also be set to '1'.



**Figure 4b Receive UART Function (Async)**

The C-BUS serial clock should be fast enough to ensure that an RX DATA READY interrupt is serviced completely within a time which is less than 8 bit-times at 1200 baud, i.e. in less than 6.67ms.

### 1.5.3 Software Description

#### Write-only 'C-BUS' Registers

REGISTER NAME	HEX ADDRESS/COMMAND	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
GENERAL RESET	\$01	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
SET-UP	\$E0	0	RELAY DRIVE	DETECT DET1	DETECT DET0	LOOP-BACK: L1	LOOP-BACK: L0	XTAL FRQ: X1	XTAL FRQ: X0
TX TONES	\$E1	TONE SEL	TONE / NOTONE	DTMF / MODEM TONES	DTMF / SNGL	D3	D2	D1	D0
GAIN BLOCKS	\$E2	TXGAIN TG3	TXGAIN TG2	TXGAIN TG1	TXGAIN TG0	RXGAIN RG3	RXGAIN RG2	RXGAIN RG1	RXGAIN RG0
TX DATA BYTE	\$E3	D7	D6	D5	D4	D3	D2	D1	D0
UART MODE	\$E4	0	0	SYNC/ASYNC	STOP BITS B	STOP BITS A	PARITY ENABLE	PARITY ODD/EVEN	DATA BITS 8/7
TX PSK MODE	\$E7	0	TXON ENAB	SCRAMB UNLOCK	SCRAMB ENABLE	EQUAL ET1	EQUAL ET0	ENABLE	HI / LO BAND
RX PSK MODE	\$E8	0	CPBW SELECT	DE-SCRAMB UNLOCK	DE-SCRAMB ENABLE	EQUAL ER1	EQUAL ER0	ENABLE	HI / LO BAND
IRQ MASK BITS	\$EE	RX PARITY	RING DETECT	DETECT	RX DATA OVER-FLOW	RX DATA READY	TX DATA UNDER-FLOW	TX DATA READY	UN-SCRAMB MARK

#### Write-only Register Descriptions

##### GENERAL RESET (\$01)

The reset command has no data attached to it. Application of the GENERAL RESET sets all write-only register bits to '0'.

##### SET-UP Register (\$E0)

###### (Bit 7)

Reserved for future use. This bit should be set to '0'.

###### RELAY DRIVE

###### (Bit 6)

This bit controls a low impedance pull-down transistor connected to the RLYDRV pin to assist with the operation of an 'off-hook relay'. When set to '1' the transistor acts as a pull-down and will sink current. When set to '0' the pin is in a high impedance state.

##### DETECT DET1 and DET0

###### (Bits 5 and 4)

These 2 bits control the operation of the receiver filter in order to facilitate the detection of the following signals as shown in the table below:

DET1 Bit 5	DET0 Bit 4	Required Rx HI/LO Band Setting (Register \$E8, Bit 0)	Detection Mode
0	0	As required for Rx PSK	PSK Carrier
0	1	LO = '0'	Call Progress
1	0	HI = '1'	Answer Tone
1	1	As required for Rx PSK	Detectors OFF

Rx PSK MODE register ENABLE bit should be set to '1' for answer tone and call progress detection.

**LOOPBACK L1 and L0  
(Bits 3 and 2)**

These 2 bits control internal signal paths such that loopback tests can be performed. Function is according to the following table:

<b>L1 Bit 3</b>	<b>L0 Bit 2</b>	
0	0	<b>Normal Device Operation:</b> no loopback.
0	1	<b>Local Analogue Loopback:</b> the output of the Tx gain block is routed to the input of the receiver gain block. (The connection between the receiver op-amp and gain block is broken).
1	0	<b>Local Digital Loopback:</b> data is loaded into the TX DATA BYTE register in the usual way via the 'C-BUS' when indicated by the TX DATA READY flag. This digital data is internally retimed serially to the modem bit-rate and is then clocked into the receiver buffer. When the receiver buffer is full the RX DATA READY flag will be set and the data can then be read out of RX DATA BYTE register via the 'C-BUS'.
1	1	Reserved for future use.

**XTAL FRQ X1 and X0  
(Bits 1 and 0)**

These two bits control the internal primary clock dividers to allow for a choice of 3 crystal frequencies. They can also be set to put the device into 'Zero Power' mode: in this mode all functions are powersaved, except for the 'C-BUS' and the Ring Detector. In 'Zero Power' the crystal oscillator is disabled and the Bias resistor chain is disconnected from the supplies.

Note: When the device is brought out of 'Zero Power' mode, the software should allow at least 20ms for the crystal oscillator to re-start and for the Bias capacitor to re-charge, before proceeding with any further device functions. The function is given by the following table:

<b>X1 Bit 1</b>	<b>X0 Bit 0</b>	<b>Crystal / Mode</b>
0	0	'Zero Power'
0	1	3.6864MHz crystal
1	0	7.3728MHz crystal
1	1	11.0592MHz crystal

**TX TONES Register (\$E1)**

This register is used to transmit both DTMF and modem progress tones.

**TONESEL  
(Bit 7)**

This bit selects the "Answer Tone" frequency in the receive detector. A '0' selects 2225Hz and a '1' selects 2100Hz.

**TONE/NOTONE  
(Bit 6)**

This bit should be used to begin and end the transmission of tones once the required frequency has been programmed. When set to '1' the tone will be transmitted; when set to '0' a Notone (Bias Voltage) will be generated.

**DTMF/MODEM TONES  
(Bit 5)**

When this bit is set to '1' the device is configured for DTMF. When it is set to '0' the device is configured to transmit modem progress tones.

**DTMF/SNGL  
(Bit 4)**

For normal DTMF operation this bit should be set to '0'. For test purposes it can be set to '1' in order to select the tone frequencies individually.

The following table shows the settings required for transmitting DTMF (Bit 5 should be set to '1'. Bits 6 and 7 should be operated as described above).

D3	D2	D1	D0	Lower Freq. (Hz) (setting Bit 4 = 0)	Upper Freq. (Hz) (setting Bit 4 = 0)	Keypad symbol	Single Tone Freq. (Hz) (setting Bit 4 = 1)
0	0	0	0	941	1633	D	1633
0	0	0	1	697	1209	1	1209
0	0	1	0	697	1336	2	1336
0	0	1	1	697	1477	3	1477
0	1	0	0	770	1209	4	1209
0	1	0	1	770	1336	5	1336
0	1	1	0	770	1477	6	1477
0	1	1	1	852	1209	7	1209
1	0	0	0	852	1336	8	852
1	0	0	1	852	1477	9	852
1	0	1	0	941	1336	0	941
1	0	1	1	941	1209	*	941
1	1	0	0	941	1477	#	941
1	1	0	1	697	1633	A	697
1	1	1	0	770	1633	B	770
1	1	1	1	852	1633	C	852

The following table shows the settings required for transmitting modem progress tones. (Set Bit 4 to '0' and Bit 5 to '0'. Bits 6 and 7 should be operated as described earlier).

D3	D2	D1	D0	Frequency (Hz)	Tone Description
0	0	0	0	550	Guard
0	0	0	1	1300	Calling
0	0	1	0	1800	Guard
0	0	1	1	2100	Answer
0	1	0	0	2225	Answer

**GAIN BLOCKS Register (\$E2)**

Bits 0 to 3 (RG0 to RG3) control the levels of the receiver input gain block according to the following table:

<b>RG3 (Bit 3)</b>	<b>RG2 (Bit 2)</b>	<b>RG1 (Bit 1)</b>	<b>RG0 (Bit 0)</b>	<b>GAIN (dB)</b>
0	0	0	0	-4.70
0	0	0	1	-3.46
0	0	1	0	-2.12
0	0	1	1	-0.96
0	1	0	0	0.00
0	1	0	1	0.87
0	1	1	0	1.64
0	1	1	1	2.36
1	0	0	0	3.08
1	0	0	1	3.69
1	0	1	0	4.22
1	0	1	1	4.76
1	1	0	0	5.27
1	1	0	1	5.78
1	1	1	0	6.21
1	1	1	1	6.58

The gain should be set in a calibration procedure in order to trim out the effects of any component tolerances which may give rise to a variation in the Carrier Detect Threshold levels.

Bits 4 to 7 (TG0 to TG3) control the levels of the transmit path gain block according to the following table:

<b>TG3 (Bit 7)</b>	<b>TG2 (Bit 6)</b>	<b>TG1 (Bit 5)</b>	<b>TG0 (Bit 4)</b>	<b>GAIN (dB)</b>
0	0	0	0	OFF (o/p at Bias)
0	0	0	1	-5.6
0	0	1	0	-5.2
0	0	1	1	-4.8
0	1	0	0	-4.4
0	1	0	1	-4.0
0	1	1	0	-3.6
0	1	1	1	-3.2
1	0	0	0	-2.8
1	0	0	1	-2.4
1	0	1	0	-2.0
1	0	1	1	-1.6
1	1	0	0	-1.2
1	1	0	1	-0.8
1	1	1	0	-0.4
1	1	1	1	0.0

**TX DATA BYTE Register (\$E3)**

The bytes of data to be transmitted should be loaded into this register. It is double buffered, thus giving the user up to 8 bit periods to load in the next 8 bits. Each byte represents 4 lots of 2 consecutive bits (dibits) with the most significant dibit being loaded first (taking Bit 7 of this register as being the most significant). The data is reversed so that it is transmitted least significant dibit first. These dibits represent a transmitted phase change according to the following table:

Dibit values	Phase change
00	+ 90°
01	0°
11	+ 270°
10	+ 180°

Note that the left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

**UART MODE Register (\$E4)****(Bit 7 and Bit 6)**

Reserved for future use. These bits should be set to '0'.

**SYNC/ASYNC  
(Bit 5)**

When this bit is '0', data will be transmitted and received in normal 8 bit mode without modification.

When this bit is '1', data will be transmitted and received with one start bit ('0') and 7/8 bits, odd/even parity, 0 or 1 or 2 stop bits according to the remainder of the bits in this register.

Prior to handshaking the UART Mode register needs Bit 5 cleared for synchronous operation. After the handshaking procedure has completed Bit 5 the UART Mode register should be set for asynchronous data transfer. The remaining bits of this register should be configured to be compatible with the modem you are talking to. The minimum number of stop bits only applies to the transmitter, the receiver does not require any defined number of stop bits.

**STOP BITS A and B  
(Bits 4 and 3)**

The minimum number of stop bits transmitted after each data byte plus parity is defined by the table below.

Stop Bits A	Stop Bits B	Number of Stop Bits
0	0	0
0	1	1
1	0	1
1	1	2

The receiver does not require any defined number of stop bits.

**PARITY ENABLE  
(Bit 2)**

When this bit is '1' an extra bit is added after the data to indicate the parity of that data.

When set to '0', parity is disabled. This bit affects both transmitter and receiver.

**PARITY ODD/EVEN  
(Bit 1)**

When this bit is '1' the parity is set odd, and when this bit is '0' the parity is set even.

This bit affects both transmitter and receiver.

**DATA BITS 8/7  
(Bit 0)**

When this bit is '1' the data is set to transmit and receive 7 bits i.e. bits 0 - 6.

When this bit is '0' the normal 8 bits of data is programmed. This bit affects both transmitter and receiver.

**TX PSK MODE Register (\$E7)****(Bit 7)**

Reserved for future use. This bit should be set to '0'.

**TXON ENAB****(Bit 6)**

This bit enables or powersaves the inverted output of the line driving amplifier (TXON). When set to '1' TXON is enabled; together with TXO these outputs provide sufficient complementary output to drive a line even at low VDD. When set to '0' the TXON output is powersaved, reducing the total supply current for applications in which a single-ended output is sufficient.

**SCRAMB UNLOCK****(Bit 5)**

When this bit is set to '1' the scrambler will check for sequences of 64 consecutive ones at its output (caused by scrambler lockup) and once detected it will invert the next input to the scrambler. When this bit is set to '0' the lock-up prevention is disabled.

**SCRAMB ENABLE****(Bit 4)**

When this bit is set to '1' the Tx data is passed through the scrambler. When it is set to '0' the scrambler is bypassed.

**EQUAL ET1 and ET0****(Bits 3 and 2)**

These 2 bits control the level of equalisation applied to the transmitted signal according to the following table:

<b>ET1 (Bit 3)</b>	<b>ET0 (Bit 2)</b>	<b>Transmitter Equalisation</b>
0	0	no equalisation
0	1	Low
1	0	Medium
1	1	High

See Figures 5a and 5b for the typical equaliser responses. The equaliser is automatically powersaved when both ET1 and ET0 are set to '0'.

**ENABLE****(Bit 1)**

When this bit is set to '1' the internal output of the PSK modulator is enabled. When it is set to '0' the internal output of the PSK modulator is set to  $V_{BIAS}$ . Associated flags are only set when this bit is '1'.

**HI/LO BAND****(Bit 0)**

This bit determines whether the transmitted PSK signal should occupy the low channel (900Hz - 1500Hz) or the high channel (2100Hz - 2700Hz). When the bit is set to '0' the low channel is selected. When it is set to '1' the high channel is selected.

**RX PSK MODE Register (\$E8)****(Bit 7)**

Reserved for future use. This bit should be set to '0'.

**CPBW SELECT****(Bit 6)**

When this bit is set to '1' the Call Progress Detector bandwidth is approximately 300Hz - 620Hz.

When this bit is set to '0' the Call Progress Detector bandwidth is approximately 400Hz - 620Hz.

**DE-SCRAMB UNLOCK****(Bit 5)**

When this bit is set to '1' the de-scrambler will check for sequences of 64 consecutive ones at its input and once detected it will invert the next output from the de-scrambler. When this bit is set to '0' the all ones detection is disabled - it should be set as such until the handshaking sequence is complete.

**DE-SCRAMB ENABLE****(Bit 4)**

When this bit is set to '1' the Rx data is passed through the de-scrambler. When it is set to '0' the de-scrambler is bypassed.

**EQUAL ER1 and ER0****(Bits 3 and 2)**

These 2 bits control the level of equalisation applied to the received signal according to the following table:

<b>ER1 (Bit 3)</b>	<b>ER0 (Bit 2)</b>	<b>Receiver Equalisation</b>
0	0	no equalisation
0	1	Low
1	0	Medium
1	1	High

See Figures 5a and 5b for the typical equaliser responses. The equaliser is automatically powersaved when ET1 and ET0 are set to "no equalisation" ('0', '0').

**ENABLE****(Bit 1)**

When this bit is set to '1' the PSK receiver is enabled. When it is set to '0' the receiver is disabled. Associated flags are only set when this bit is '1'.

**HI/LO BAND****(Bit 0)**

This bit determines whether the received PSK signal should be filtered and derived from the low channel (900Hz - 1500Hz) or the high channel (2100Hz - 2700Hz). When this bit is set to '0' the low channel is selected. When it is set to '1' the high channel is selected.



**IRQ MASK BITS (\$EE)**

This register is used to control the interrupts (IRQs) as described below:

<b>RX PARITY mask (Bit 7)</b>	When this bit is set to '1' it enables an interrupt that occurs when the RX PARITY flag (Bit 7, FLAGS Register, \$EF) changes from '0' to '1' i.e. there is an RX PARITY error. When this bit is '0' the interrupt is masked.
<b>RING DETECT mask (Bit 6)</b>	When this bit is set to '1' it enables an interrupt that occurs when RING DETECT CHANGE flag (Bit 6, FLAGS Register, \$EF) changes from '0' to '1'. When this bit is '0' the interrupt is masked.
<b>DETECT mask (Bit 5)</b>	When this bit is set to '1' it enables an interrupt that occurs when DETECT flag (Bit 5, FLAGS Register, \$EF) changes from '0' to '1'. When this bit is '0' the interrupt is masked.
<b>RX DATA OVERFLOW mask (Bit 4)</b>	When this bit is set to '1' it enables an interrupt that occurs when RX DATA OVERFLOW flag (Bit 4, FLAGS Register, \$EF) changes from '0' to '1'. When this bit is '0' the interrupt is masked.
<b>RX DATA READY mask (Bit 3)</b>	When this bit is set to '1' it enables an interrupt that occurs when RX DATA READY flag (Bit 3, FLAGS Register, \$EF) changes from '0' to '1'. When this bit is '0' the interrupt is masked.
<b>TX DATA UNDERFLOW mask (Bit 2)</b>	When this bit is set to '1' it enables an interrupt that occurs when TX DATA UNDERFLOW flag (Bit 2, FLAGS Register, \$EF) changes from '0' to '1'. When this bit is '0' the interrupt is masked.
<b>TX DATA READY mask (Bit 1)</b>	When this bit is set to '1' it enables an interrupt that occurs when TX DATA READY flag (Bit 1, FLAGS Register, \$EF) changes from '0' to '1'. When this bit is '0' the interrupt is masked.
<b>UNSCRAM MARK mask (Bit 0)</b>	When this bit is set to '1' it enables an interrupt that occurs when UNSCRAM MARK flag (Bit 0, FLAGS Register, \$EF) changes from '0' to '1'. When this bit is '0' the interrupt is masked.

### Read Only 'C-BUS' Registers

REGISTER NAME	HEX ADDRESS/COMMAND	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
RX DATA BYTE	\$EA	D7	D6	D5	D4	D3	D2	D1	D0
TONES DETECT	\$EC	1	RING DETECT	CALL PRGRSS DETECT	CARRIER DETECT	ANSWER DETECT	0	0	UN-SCRAM MARK DETECT
FLAGS	\$EF	RX PARITY	RING DETECT CHANGE	DETECT	RX DATA OVER-FLOW	RX DATA READY	TX DATA UNDER-FLOW	TX DATA READY	UN-SCRAM MARK

#### RX DATA BYTE Register (\$EA)

This register contains the last byte of data received. It is updated every 8 bits at the same time as the RX DATA READY flag is set. The RX DATA BYTE register is double buffered, thus giving the user up to 8 bit periods to read the data before it is overwritten by the next byte. Each received phase change is decoded into 2 bits (a dibit). The incoming dibits fill this register starting at the most significant end (Bits 7 and 6).

Phase change	Dibit values
+ 90°	00
0°	01
+ 270°	11
+ 180°	10

Note that the left-hand digit of the dibit will be the more significant of the 2 bits when located in this register.

#### TONES DETECT Register (\$EC)

This register provides information as to the presence or absence of various signalling conditions detected by the receiver. A logic '1' indicates that the signalling condition is present; a logic '0' indicates that it is absent.

<b>(Bit 7)</b>	This bit will be set to '1'.
<b>RING DETECT (Bit 6)</b>	Indicates the status of the Ring/Line Polarity Reversal Detector circuit. The logic level of this bit represents the level of the internal 'RING DETECT' node (see Figure 1 Block Diagram).
<b>CALL PRGRSS DETECT (Bit 5)</b>	Indicates the detection of call progress tones in the selected band. (300Hz to 620Hz or 400Hz to 620Hz).
<b>CARRIER DETECT (Bit 4)</b>	Indicates the detection of a carrier in the received channel.
<b>ANSWER DETECT (Bit 3)</b>	Indicates the detection of an Answer Tone of 2100Hz or 2225Hz.
<b>(Bits 2 and 1)</b>	These bits will be set to '0'.
<b>UNSCRAM MARK DETECT (Bit 0)</b>	Indicates the detection of unscrambled binary one in the received data for a period of time of 160ms.

Note that DETECT bits 5, 4 and 3 are mutually exclusive and are enabled by the setting of the DETECT DET1 and DET0 bits (SET-UP Registers Bits 5 and 4). All of the DETECT bits in the TONES DETECT register - except for RING DETECT (Bit 6) - require the RX PSK MODE register ENABLE bit to be set to '1'.

#### FLAGS Register (\$EF)

The flags register is used to indicate when the device requires attention. When a flag becomes set to '1' and its corresponding mask bit is '1' then an interrupt (IRQN) will be generated. Immediately after the flags register has been read, all the bits will be reset to '0' and consequently any interrupt will be cleared.

<b>RX PARITY flag (Bit 7)</b>	When this bit is '1' the received parity is in error. When this bit is '0' the received parity is correct.
<b>RING DETECT CHANGE flag (Bit 6)</b>	When RING DETECT (TONES DETECT Register, Bit 6) changes state, this bit will be set to '1'.
<b>DETECT flag (Bit 5)</b>	When any of the following bits - CALL PRGRSS DETECT, CARRIER DETECT or ANSWER DETECT (TONES DETECT Register Bits 5, 4, 3) - change state, this bit will be set to '1'.
<b>RX DATA OVERFLOW flag (Bit 4)</b>	If received data is not read out of the device within the 8-bit window of RX DATA READY going high, then this bit will be set to '1' to indicate an error condition.
<b>RX DATA READY flag (Bit 3)</b>	When a full byte of data is received and is available in the RX DATA BYTE register, this bit will be set to '1'. There is then an 8-bit window during which the RX DATA BYTE register must be read.
<b>TX DATA UNDERFLOW flag (Bit 2)</b>	If data is not loaded into the TX DATA BYTE register within the 8-bit window of TX DATA READY going high, then this bit will be set to '1' to indicate an error condition.
<b>TX DATA READY flag (Bit 1)</b>	When the Tx data buffer is ready to receive a new byte of data, this bit will be set to '1'. There is then an 8-bit window for the loading of the TX DATA BYTE register.
<b>UNSCRAM MARK flag (Bit 0)</b>	When the UNSCRAM MARK DETECT bit (TONES DETECT Register Bit 0) changes state, this bit will be set to '1'.

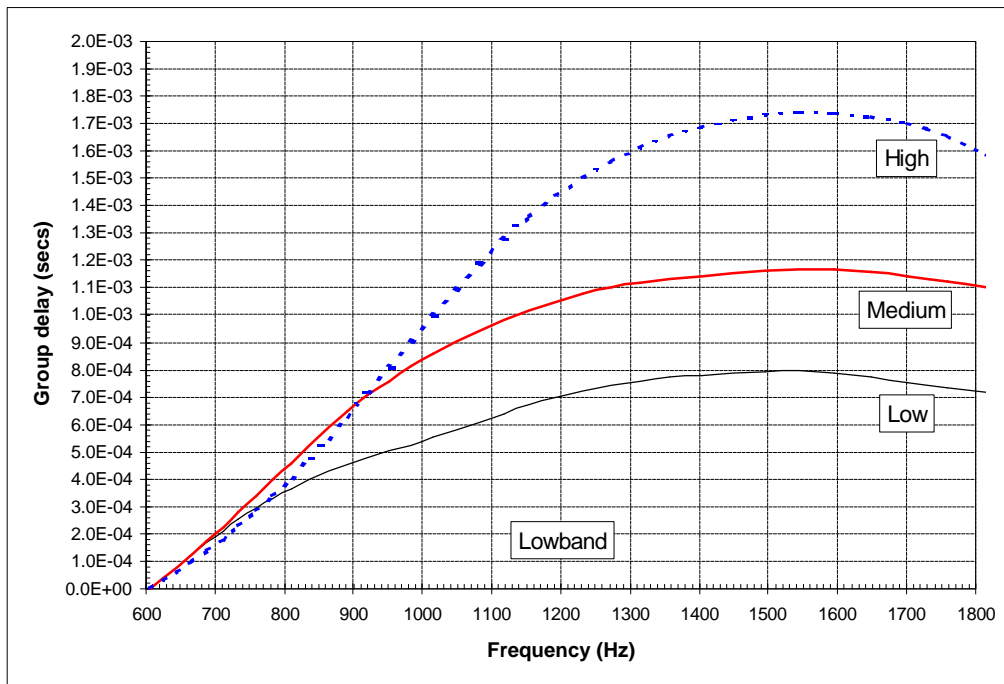


Figure 5a Transmit/Receive Equaliser Responses: Lowband

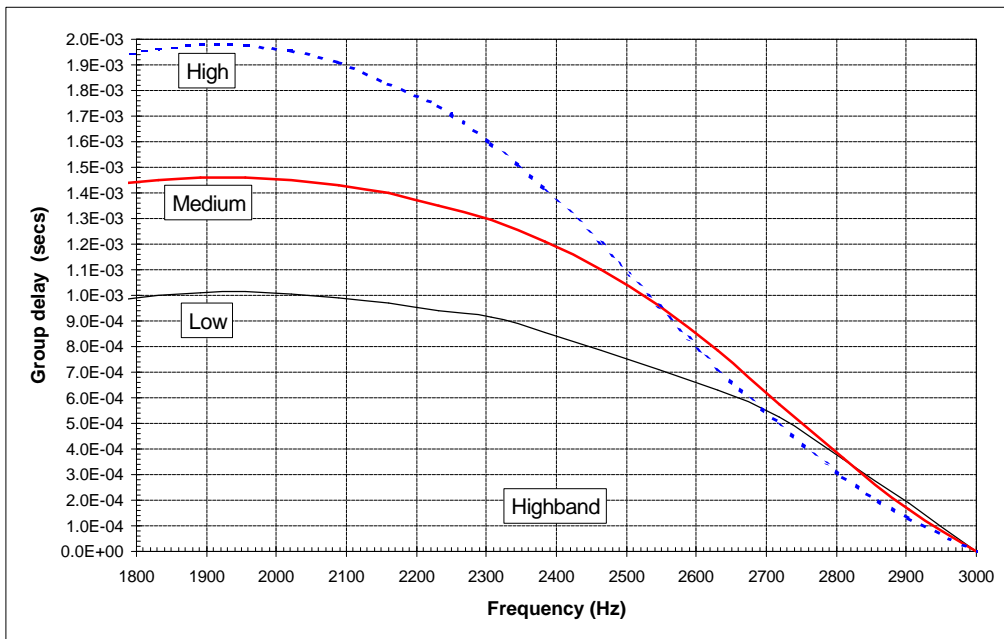


Figure 5b Transmit/Receive Equaliser Responses: Highband

The CMX644A utilises two internal equalisers - one is configured for the High Band, the other for the Low Band. The Transmit and Receive paths will be internally switched through the equaliser appropriate to their HI/LO BAND settings. In the event of both Transmit and Receive paths being set to the same band, both equalisers will be bypassed.

## 1.6 Application Notes

### 1.6.1 Line Interface

A line interface circuit is needed to provide dc isolation between the modem and the line, to perform line impedance termination, and to set the correct transmit and receive signal levels.

#### 4-Wire Line Interface

Figure 6a shows an interface circuit for use with a 600Ω 4-wire line. The line terminations are provided by R10 and R15, while R11 and R13 should be selected to give the desired transmit and receive levels.

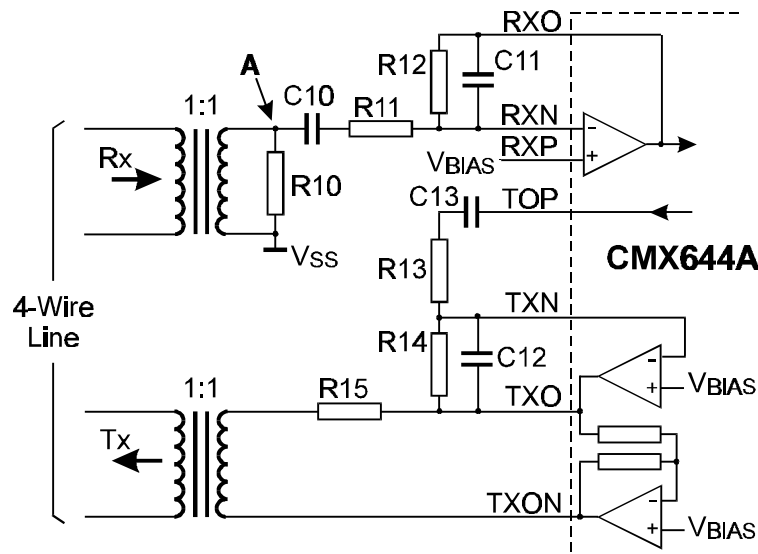
When  $V_{DD} = 5.0V$ , the gain of the receive input amplifier ( $R12/R11$ ) should be 6dB (times 2.0) plus whatever additional gain is required to compensate for the loss of the input transformer. At other values of  $V_{DD}$  the amplifier gain should be multiplied by the ratio  $V_{DD}/5.0$ .

Thus for  $R12 = 100k\Omega$ :

$$R11 = 100k\Omega * (5.0/V_{DD}) / (\text{Input transformer loss} * 2.0)$$

where the 'Input transformer loss' = (Rx level on 4-wire line) / (level at point A of Figure 6a).

Assuming a transformer loss of about 1dB, R11 should be 47kΩ at  $V_{DD} = 5.0V$ , and 68kΩ at 3.3V. The value of the resistor R11 is optimised for the carrier detect level. Increasing the input gain (by reducing the value of R11) will improve modem sensitivity.



Note Relay circuit, ac and dc loads and line protection are not shown for clarity.

R10	600Ω	R14	100kΩ	C10	100nF
R11	See text	R15	600Ω	C11	330pF
R12	100kΩ			C12	330pF
R13	See text			C13	100nF

Resistors  $\pm 1\%$ , capacitors  $\pm 20\%$ .

**Figure 6a 4-Wire Line Interface Circuit**

In the transmit direction, the level on the 4-wire line is determined by the level at the TOP pin, the gain of the Output Buffer Amplifier, a loss of nominally 6dB due to the line termination resistor R15, and the loss in the transformer.

The TOP pin signal level is proportional to  $V_{DD}$  and is also affected by the setting of the transmitter programmable gain block.

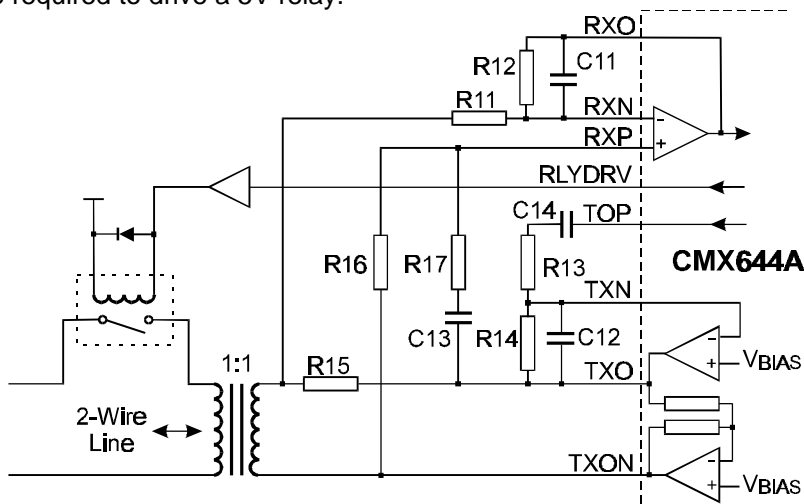
Assuming that the Tx programmable gain block is set to -2dB (giving a PSK signal level of -4dB wrt 775mVrms at the TOP pin when  $V_{DD} = 5.0V$ ) and that there is 1dB loss in the transformer, then:

$$\text{Tx PSK 4-wire line level} = -(4 + 6 + 1) + 20 * \text{LOG}_{10}(2 * R_{14}/R_{13}) + 20 * \text{LOG}_{10}(V_{DD} / 5.0) \text{ dBm}$$

For example, to generate a nominal Tx FSK line level of -10dBm, R13 should be 180kΩ when  $V_{DD} = 5.0V$ , falling to 120kΩ at 3.3V.

**2-Wire Line Interface**

Figure 6b shows an interface circuit suitable for connection to a 600Ω 2-wire line. The circuit also shows how a relay may be driven from the RLYDRV pin. Note that when the CMX644A is powered from less than 5.0V, buffer circuitry will be required to drive a 5V relay.



Note: ac and dc loads and line protection are not shown for clarity

R11	See text	R15	600Ω	C11	330pF
R12	100kΩ	R16	120kΩ	C12	330pF
R13	See text	R17	100kΩ	C13	10nF
R14	100kΩ			C14	100nF

Resistors ±1%, capacitors ±20%

**Figure 6b 2-Wire Line Interface Circuit**

This circuit includes a 2-wire to 4-wire hybrid circuit, formed by R11, R15, R16, R17, C13 and the impedance of the line itself, which ensures that the modem receive input and transmit output paths are both coupled efficiently to the line, while minimising coupling from the modem's transmit signal into the receive input. The values of R11 and R13 should be calculated in the same way as for the 4-wire interface circuit of Figure 6a. Note that the component values R17 and C13 depend on the transformer characteristics and should be adjusted to achieve a flat frequency response measured at the RXO pin.

### 1.6.2 Ring Detector Interface

Figure 7 shows how the CMX644A may be used to detect the large amplitude Ringing signal received at the start of an incoming telephone call.

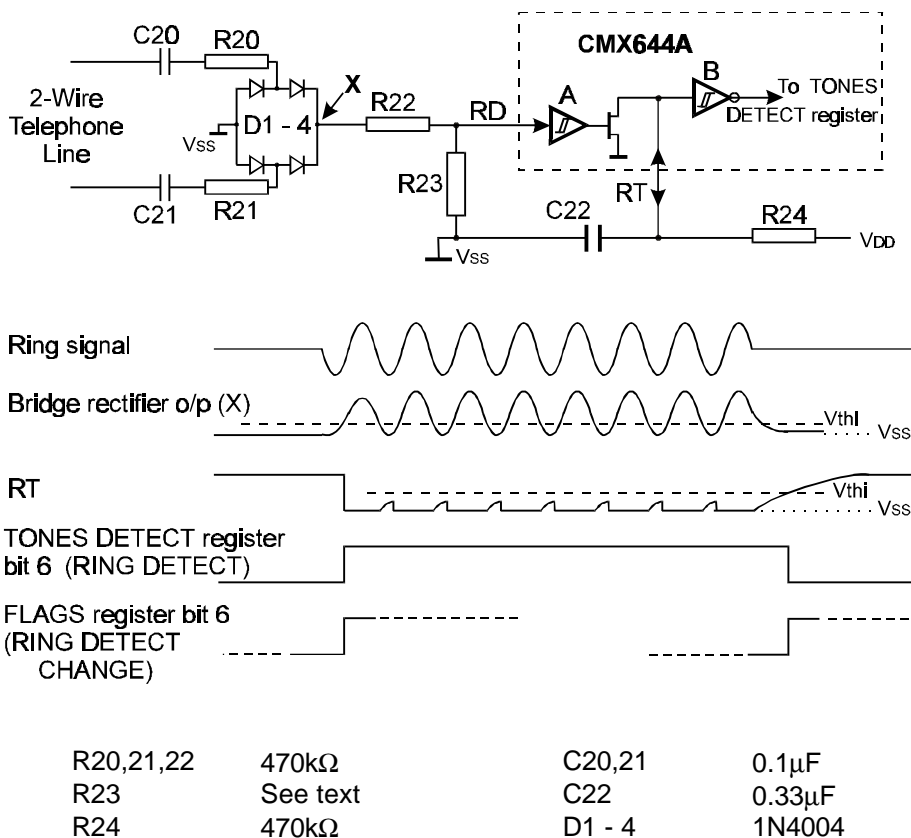
The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through either C20 and R20 or C21 and R21 to appear at the top end of R22 (point X in Figure 7) in a rectified and attenuated form.

The signal at point X is further attenuated by the potential divider formed by R22 and R23 before being applied to the CMX644A RD input. If the amplitude of the signal appearing at RD is greater than the input threshold (Vthi) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to VSS by discharging the external capacitor C22. The output of the Schmitt trigger 'B' will then go high, setting bit 6 (RING DETECT) of the TONES DETECT register.

The minimum amplitude ringing signal that is certain to be detected is  

$$(0.7 + V_{thi} * [R20 + R22 + R23] / R23) * 0.707 \text{ Vrms}$$
 where Vthi is the high-going threshold voltage of the Schmitt trigger A

With R20 - 22 all 470kΩ as Figure 7, then setting R23 to 68kΩ will guarantee detection of ringing signals of 40Vrms and above for VDD over the range 3.0 to 5.5V.



Resistors ±1%, capacitors ±20%

Figure 7 Ring Signal Detector Interface Circuit

If the time constant of R24 and C22 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger for the duration of a ring cycle.

The time for the voltage on RT to charge from  $V_{SS}$  towards  $V_{DD}$  can be derived from the formula

$$V_{RT} = V_{DD} * [1 - \exp(-t/(R24 \times C22)) ]$$

As the Schmitt trigger high-going input threshold voltage ( $V_{thi}$ ) has a minimum value of  $0.56 \times V_{DD}$ , then the Schmitt trigger B output will remain high for a time of at least  $0.821 \times R24 \times C22$  following a pulse at RD.

The values of R24 and C22 given in Figure 7 ( $470k\Omega$  and  $0.33\mu F$ ) give a minimum RT charge time of 100 msec, which is adequate for ring frequencies of 10Hz or above.

Note that the circuit will also respond to a telephone line voltage reversal. If necessary the  $\mu C$  can distinguish between a Ring signal and a line voltage reversal by measuring the time that bit 6 of the TONES DETECT register (RING DETECT) is high.

### 1.6.3 Software Protocol for Transmitting PSK Data Bytes

In order to transmit PSK data, the following steps should be followed. For clarity, not all bit settings are described here (but HI/LO Band, Equalisation, Guard Tones, Number of Stop Bits etc. should be set as appropriate).

1. Program SETUP register for correct crystal frequency. Wait at least 20ms if device was previously in 'Zero Power' mode before proceeding.
2. Set Tx Gain Block (GAIN BLOCKS Register \$E2) to required gain. Set UART mode.
3. Load first data byte into TX DATA BYTE Register (\$E3).
4. Read FLAGS Register (\$EF) in order to clear it.
5. Set IRQ MASK BITS Register (\$EE Bits 2 and 1) to allow appropriate interrupts (TX DATA UNDERFLOW and TX DATA READY). Note: If an underflow occurs, continuous mark ('1') will be transmitted.
6. Set ENABLE bit (TX PSK MODE Register \$E7) to '1'. The first byte of data will now be transmitted by the device.
7. Wait for a TX DATA READY generated interrupt (read FLAGS to check and clear the IRQ).
8. Load next TX DATA BYTE.
9. Go to 7.

Note that the transmission should be terminated by setting the ENABLE bit (TX PSK MODE Register) to '0'.



#### 1.6.4 Software Protocol for Receiving PSK Data Bytes

1. With the device out of 'Zero Power' mode, set up all receiver-related functions: Gain, HI/LO Band, Equalisation, UART mode, etc.
2. Perform a dummy read of the Rx DATA BYTE Register (\$EA) and discard the result.
3. Read FLAGS Register (\$EF) in order to clear it.
4. Set IRQ MASK BITS Register (\$EE Bits 7, 4 and 3) to allow appropriate interrupts (RX PARITY, RX DATA OVERFLOW and RX DATA READY).
5. Set ENABLE bit (RX PSK MODE Register \$E8) to '1'.
6. Wait for an RX DATA READY generated interrupt (read FLAGS to check and clear the IRQ).
7. Read RX DATA BYTE (\$EA).
8. Go to 5.

#### 1.6.5 Handling Underflow and Overflow Conditions

If the RX DATA BYTE Register has not been read before the next byte of Rx data is received, then the RX DATA OVERFLOW flag will be set and the RX DATA BYTE Register will hold the most recent byte of received data. The RX DATA READY flag will remain set if the FLAGS Register is not read before the overflow condition occurs. Both RX DATA READY and RX DATA OVERFLOW flags are reset upon reading the FLAGS Register, and are not set again until after the RX DATA BYTE Register has been read (ie the overflow condition has been cleared).

If the TX DATA BYTE Register is not written to before the last byte of Tx data is sent, then the TX DATA UNDERFLOW flag will be set and the Tx data will then consist of continuous mark ("1"), which will normally be scrambled, until new data is loaded into the TX DATA BYTE Register. The TX DATA READY flag will remain set if the FLAGS Register is not read before the underflow condition occurs. Both TX DATA READY and TX DATA UNDERFLOW flags are reset upon reading the FLAGS Register, and are not set again until after the TX DATA BYTE Register has been loaded with new data (ie the underflow condition has been cleared).

C-BUS transactions to handle underflow and overflow conditions are shown in the timing diagram of Figure 8. Note that allowance should be made for C-BUS latency ( $T_{DEL}$  and  $T_{LOAD}$ ) when changing register settings. eg To change the number of Tx stop bits transmitted with all subsequent data (STOP BITS A and B), first wait until the TX DATA READY flag is set. If this check is not made, then the number of stop bits in the Tx data byte which is currently being sent will be changed.

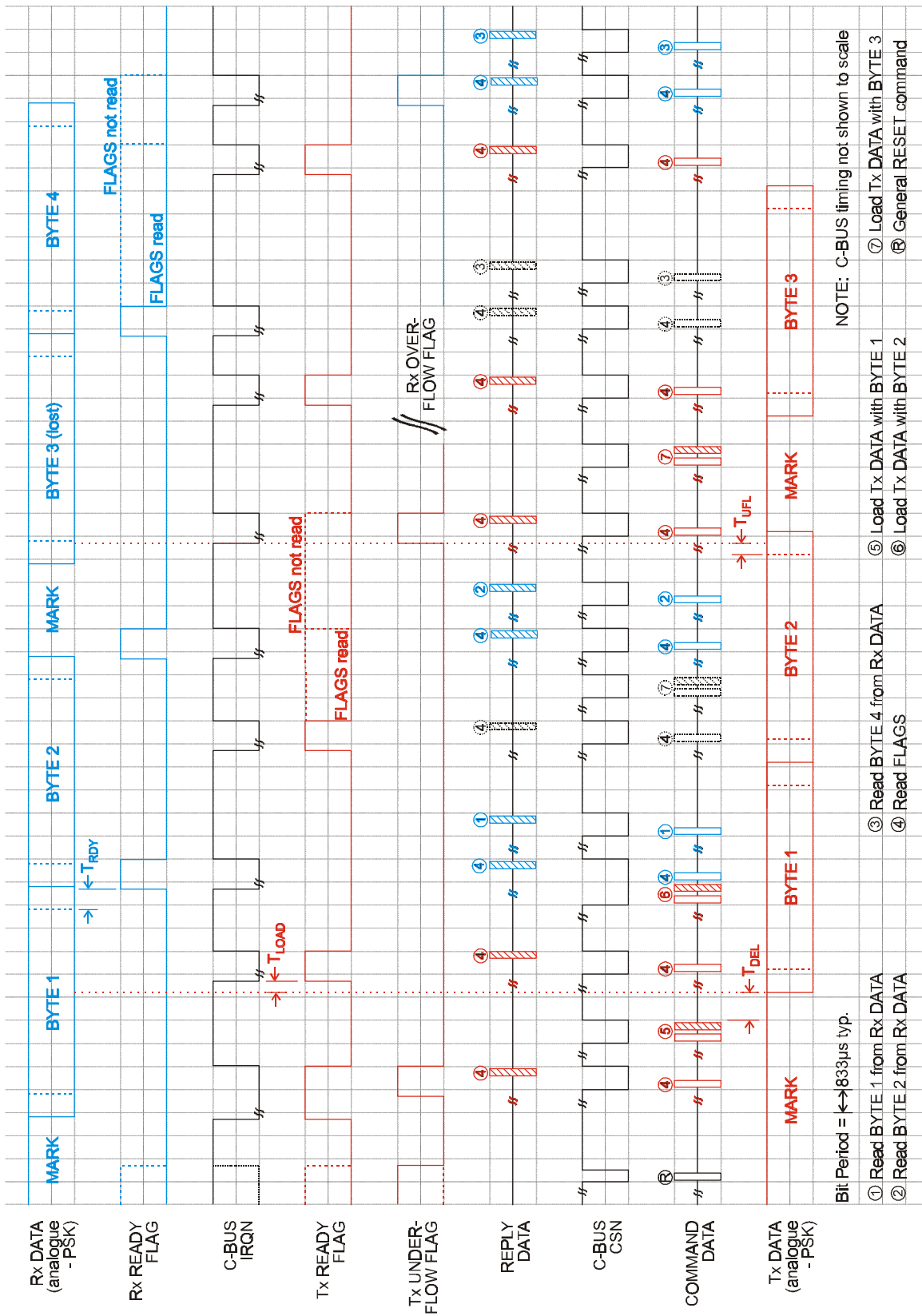


Figure 8 ASYNC MODE (Rx and Tx)

## 1.7 Performance Specification

### 1.7.1 Electrical Performance

#### 1.7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (VDD - VSS)	-0.3	7.0	V
Voltage on any pin to VSS	-0.3	V <sub>DD</sub> + 0.3	V
Current into or out of VDD and VSS pins	-50	+50	mA
Current sink into RLYDRV pin	0	+50	mA
Current into or out of any other pin	-20	+20	mA

<b>D2 Package</b>	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C	-	800	mW
... Derating	-	13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

<b>D5 Package</b>	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C	-	550	mW
... Derating	-	9	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

<b>P4 Package</b>	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C	-	800	mW
... Derating	-	13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

#### 1.7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

Nominal Xtal frequencies are 3.6864MHz, 7.372800MHz, 11.0592MHz.

	Min	Max.	Units
Supply (VDD - VSS)	2.7	5.5	V
Operating Temperature	-40	+85	°C
Xtal Frequency	-100	+100	ppm

### 1.7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD} = 2.7V$  at  $T_{amb} = 25^{\circ}C$  and  $V_{DD} = 3.0V$  to  $5.5V$  at  $T_{amb} = -40$  to  $+85^{\circ}C$ .  
0dBm corresponds to 775mVrms.

	Notes	Min.	Typ.	Max.	Units
<b>DC Parameters</b>					
$I_{DD}$ ('Zero Power')	2	-	1	-	$\mu A$
$I_{DD}$ (Operating at $V_{DD} = 3.0V$ and $T_{amb} = 25^{\circ}C$ )	2	-	3.2	4.0	mA
$I_{DD}$ (as above, but with equalisation enabled)	2	-	-	4.6	mA
Logic '1' Input Level	5	70%	-	-	$V_{DD}$
Logic '0' Input Level	5	-	-	30%	$V_{DD}$
Logic Input Leakage Current ( $V_{in} = 0$ to $V_{DD}$ ), (excluding XTAL/CLOCK input)		-1.0	-	+1.0	$\mu A$
Output Logic '1' Level ( $I_{OH} = 360\mu A$ )		$V_{DD} - 0.4$	-	-	V
Output Logic '0' Level ( $I_{OL} = 360\mu A$ )		-	-	0.4	V
IRQN O/P 'Off' State Current ( $V_{out} = V_{DD}$ )		-	-	1.0	$\mu A$
Schmitt trigger input high-going threshold ( $V_{thi}$ ) (see Figure 8)		$0.56V_{DD}$	-	$0.56V_{DD} + 0.6V$	V
Schmitt trigger input low-going threshold ( $V_{tlo}$ ) (See Figure 8)		$0.44V_{DD} - 0.6V$	-	$0.44V_{DD}$	V
Relay Driver pull-down on resistance ( $V_{DD} = 5.0V$ , 50mA maximum load current)		-	37.0	-	$\Omega$
<b>Xtal/Clock Input</b>					
Pulse Width ('High' or 'Low')	3	40	-	-	ns
Input impedance (at 100Hz)		10	-	-	M $\Omega$
Gain ( $I/P = 1mV$ rms at 1kHz)		20	-	-	dB
<b>AC Parameters</b>					
<b>Transmitter (at TOP pin)</b>					
<b>Guard Tones</b>					
Level (below PSK) of 550Hz		-	-3.0	-	dB
Level (below PSK) of 1800Hz		-	-6.0	-	dB
Frequency Accuracy		-0.25	-	+0.25	%
<b>PSK Output</b>					
Transmitted level	1, 4, 8	-3.0	-2.0	-1.0	dBm
Distortion		-	2.0	5.0	%
<b>DTMF Output</b>					
Transmitted level: high group	1, 4	-2.0	-1.0	0	dBm
Twist (high group - low group levels)	4	-	2.0	-	dB
Distortion		-	2.0	5	%
Frequency Accuracy		-0.25	-	+0.25	%

	Notes	Min.	Typ.	Max.	Units
<b>Receiver</b>					
Dynamic Range ( $V_{DD} = 5.0V$ )		-	45	-	dB
<b>Carrier Detect</b>					
Threshold: Will Decode	1, 6	-	-	-43	dBm
Threshold: Will Not Decode	1, 6	-48	-	-	dBm
Hysteresis	7	-	2.0	-	dB
Response Time (Delay)		-	20	50	ms
De-Response Time (Hold)		-	20	50	ms
<b>Answer Tone Detector</b>					
Threshold: Will Decode	1, 6	-	-	-43	dBm
Threshold: Will Not Decode	1, 6	-48	-	-	dBm
Response Time (Delay)		-	20	50	ms
De-Response Time (Hold)		-	20	50	ms
Decode Bandwidth (must decode)		2.0	-	-	%
Decode Bandwidth (must not decode)		-	-	6.0	%
<b>Call Progress Detector</b>					
Effective Bandwidth	9	300/400	-	620	Hz
Threshold: Will Decode	1, 6	-	-	-43	dBm
Threshold: Will Not Decode	1, 6	-48	-	-	dBm
Response Time (Delay)		-	20	50	ms
De-Response Time (Hold)		-	20	50	ms
<b>Programmable Gain Blocks</b>					
<b>Rx Gain Block</b>					
Nominal Range (Step Size: see Register Description)		-4.70	-	+6.58	dB
Step Accuracy		-0.5	-	+0.5	dB
<b>Tx Gain Block</b>					
Nominal Range		-5.6	-	0.0	dB
Step Size		-	0.4	-	dB
Step Accuracy		-0.2	-	+0.2	dB

- Notes:**
1. At  $V_{DD} = 5.0V$  only. Signal levels or currents are proportional to  $V_{DD}$ .
  2. Not including any current drawn from the modem pins by external circuitry.
  3. Timing for an external input to the CLOCK/XTAL pin.
  4. Tx Gain Block set to 0dB and measured with a pure tone or DTMF tone pair, without equalisation.
  5. Excluding RD, RT and XTAL/CLOCK pins.
  6. Rx Gain Block nominally set to 0dB but adjusted if necessary for component tolerances. Measurement point for threshold levels is prior to receive input amplifier circuit (point A on Figure 6a), with external components setting gain to 9dB. Detector levels measured with a pure tone.
  7. Hysteresis may be increased, if required, by adding one step (increasing the gain of) to the Rx Gain Block when a signal is detected and by removing this step when the signal is no longer detected.
  8. Measured with a 511-bit pseudorandom sequence.
  9. Depending on the setting of the CPBW SELECT bit in the RX PSK MODE Register.
  10. Measured without equalisation.

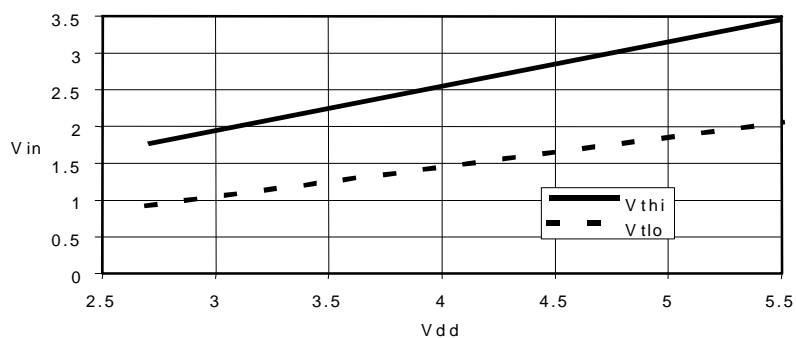


Figure 9 Typical Schmitt Trigger Input Voltage vs. V<sub>DD</sub>

<b>Tx Timings (See Figure 4a)</b>	<b>Notes</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Units</b>
Tx Delay from Tx data loaded (TDEL)	10	0	-	0.833	ms
Tx Output to Tx reload signal (TLOAD)	10	0	-	8.33	ms
Tx Parity to Tx Underflow flag set (TUFL)	10	0	-	1.667	ms
<b>Rx Timings (See Figure 4b)</b>	<b>Notes</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Units</b>
Parity to Rx Data Ready flag set (TRDY)	10	-	1.667	-	ms

1.7.1.3 Operating Characteristics (continued)

'C-BUS' Timings (See Figure 10)		Notes	Min.	Typ.	Max.	Units
tCSE	CSN-Enable to Clock-High time		100		-	ns
tCSH	Last Clock-High to CSN-High time		100		-	ns
tLOZ	Clock-Low to Reply Output enable time		0		-	ns
tHIZ	CSN-High to Reply Output 3-state time		-		1.0	µs
tCSOFF	CSN-High Time between transactions		1.0		-	µs
tNXT	Inter-Byte time		200		-	ns
tCK	Clock-Cycle time		200		-	ns
tCH	Serial Clock-High time		100		-	ns
tCL	Serial Clock-Low time		100		-	ns
tCDS	Command Data Set-Up time		75		-	ns
tCDH	Command Data Hold time		25		-	ns
tRDS	Reply Data Set-Up time		75		-	ns
tRDH	Reply Data Hold time		0		-	ns

Note: These timings are for the latest version of the 'C-BUS' as embodied in the CMX644A, and allow faster transfers than the original 'C-BUS' timings given in CML Publication D/800/Sys/3 July 1994.

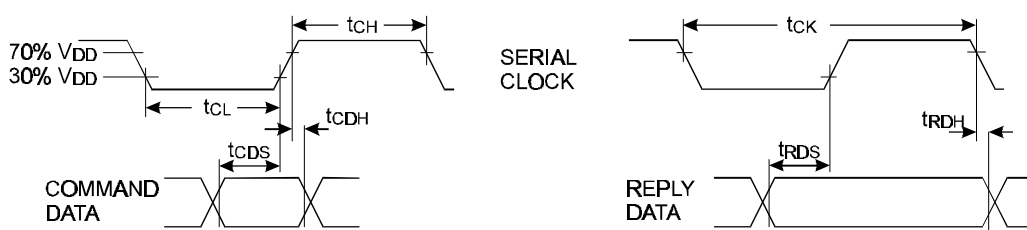
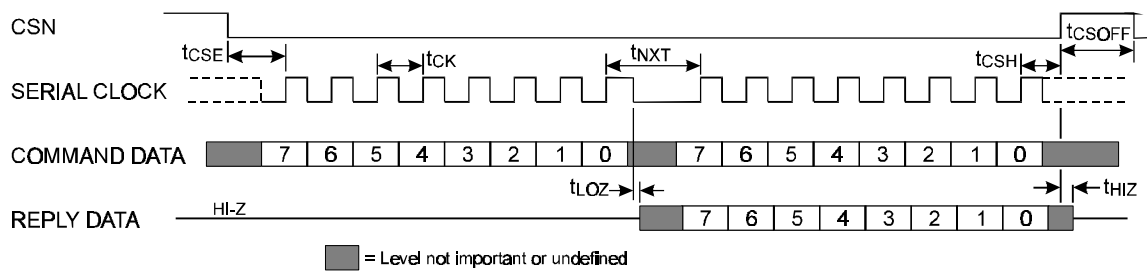
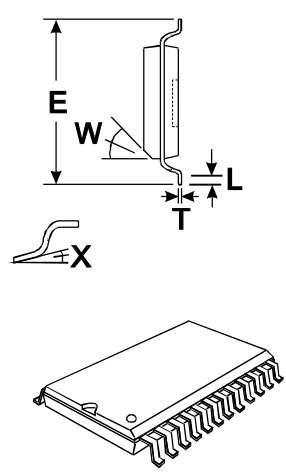
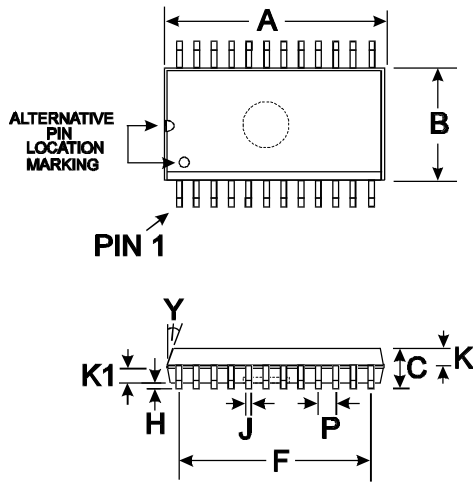


Figure 10 'C-BUS' Timing

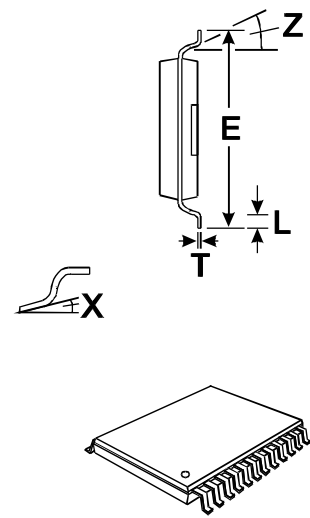
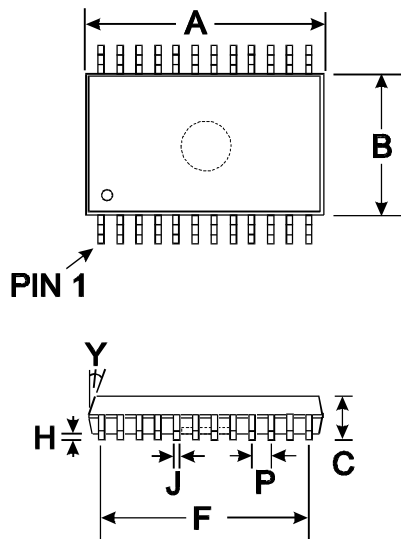
1.7.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A	0.597 (15.16)		0.613 (15.57)
* B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
F		0.550 (14.1)	
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X		0°	10°
Y		7°	

NOTE :  
 \* A & B are reference datum's and do not include mold deflash or protrusions.  
 All dimensions in inches (mm.)  
 Angles are in degrees

Figure 11a 24-pin SOIC (D2) Mechanical Outline: Order as part no. CMX644AD2

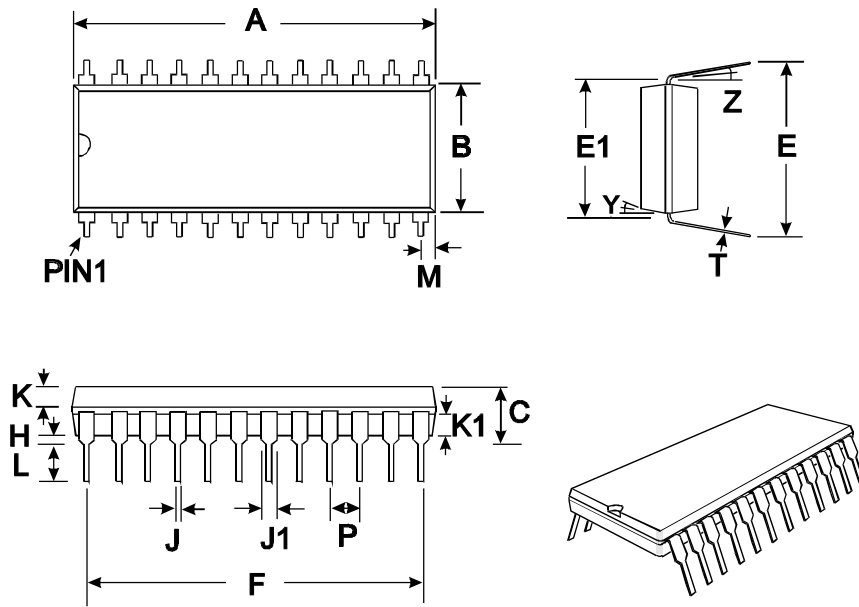


DIM.	MIN.	TYP.	MAX.
* A	0.318 (8.08)		0.328 (8.33)
* B	0.205 (5.21)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
F		0.281 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.56)		0.037 (0.94)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.23)
X		0°	8°
Y		7°	9°
Z		4°	10°

NOTE :  
 \* A & B are reference datum's and do not include mold deflash or protrusions.  
 All dimensions in inches (mm.)  
 Angles are in degrees

Figure 11b 24-pin SSOP (D5) Mechanical Outline: Order as part no. CMX644AD5





DIM.	MIN.	TYP.	MAX.
* A	1.200 (30.48)		1.270 (32.26)
* B	0.500 (12.70)		0.555 (14.10)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.06)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE :

\* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)  
Angles are in degrees

Figure 11c 24-pin DIL (P4) Mechanical Outline: Order as part no. CMX644AP4

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.



**CML Microcircuits**

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These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

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This notification is relevant product information to which it is attached.

Company contact information is as below:



**CML Microcircuits  
(UK) Ltd**

COMMUNICATION SEMICONDUCTORS

Oval Park, Langford, Maldon,  
Essex, CM9 6WG, England  
Tel: +44 (0)1621 875500  
Fax: +44 (0)1621 875600  
uk.sales@cmlmicro.com  
www.cmlmicro.com



**CML Microcircuits  
(USA) Inc.**

COMMUNICATION SEMICONDUCTORS

4800 Bethania Station Road,  
Winston-Salem, NC 27105, USA  
Tel: +1 336 744 5050,  
0800 638 5577  
Fax: +1 336 744 5054  
us.sales@cmlmicro.com  
www.cmlmicro.com



**CML Microcircuits  
(Singapore) Pte Ltd**

COMMUNICATION SEMICONDUCTORS

No 2 Kallang Pudding Road, 09-05/  
06 Mactech Industrial Building,  
Singapore 349307  
Tel: +65 7450426  
Fax: +65 7452917  
sg.sales@cmlmicro.com  
www.cmlmicro.com