T-51-19

HARRIS

CA555, CA555C, LM555C*

Timers For Timing Delays & Oscillator Applications in Commercial, Industrial & Military Equipment

August 1991

Features

- Accurate Timing from Microseconds Through Hours
- Astable and Monostable Operation
- Adjustable Duty Cycle
- Output Capable of Sourcing or Sinking up to 200mA
- Output Capable of Driving TTL Devices
- Normally ON and OFF Outputs
- High-Temperature Stability .... 0.005%/°C
- Directly Interchangeable with SE555, NE555, MC1555, and MC1455

Applications

- Precision Timing
- Sequential Timing
- Time-Delay Generation
- Pulse Generation
- Pulse-Width and Position Modulation
- Pulse Detector

Description

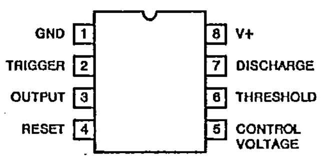
The CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the wave-form signal, and the output of these circuits can source or sink up to a 200-milliampere current or drive TTL circuits.

The CA555 and CA555C are supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead TO-5 style packages with dual-in-line formed leads (DIL-CAN, S suffix), 8-lead Small Outline package (M suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), and in chip form (H suffix). These types are direct replacement for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

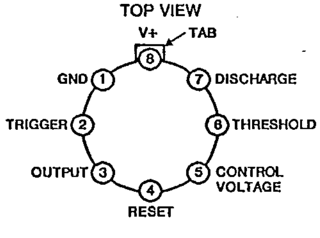
Pinouts

CA555, CA555C, LM555C
8 PIN MINI-DIP
TOP VIEW



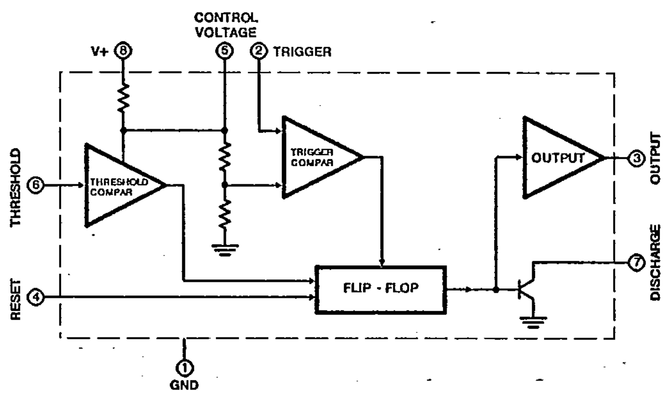
TO-5 Style Package with Formed Leads

CA555, CA555C, LM555C
8 LEAD METAL CAN
TOP VIEW



TO-5 Style Package

Functional Diagram



8 SPECIAL ANALOG CIRCUITS

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.
CAUTION: These devices are sensitive to electrostatic discharghe. Proper I.C. handling procedures should be followed.

File Number 834.1

Specifications CA555, CA555C, LM555C

Absolute Maximum Ratings Absolute-Maximum Values

DC Supply Voltage 18V
Device Dissipation:
Up to T_A = +55°C 600mW
Above T_A = +55°C .... Derate Linearly 5mW/°C

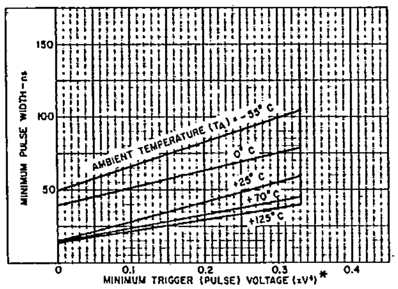
Ambient Temperature Range:
Operating CA555 .... -55°C to +125°C
CA555C .... 0°C to +70°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (During Soldering): At distance 1/16 ± 1/32in. (1.59 ± 0.79mm) from case for 10s max .... +265°C

Electrical Characteristics T_A = +25°C, V+ = 5V to 15V Unless Otherwise Specified

CHARACTERISTICS	TEST CONDITIONS	LIMITS						UNITS
		CA555			CA555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
DC Supply Voltage, V+		4.5	-	18	4.5	-	16	V
DC Supply Current (Low State), Note 1, I+	V+ = 5V, $R_L = \infty$	-	3	5	-	3	6	mA
	V+ = 15V, $R_L = \infty$	-	10	12	-	10	15	mA
Threshold Voltage, V_{TH}		-	(2/3)V+	-	-	(2/3)V+	-	V
Trigger Voltage	V+ = 5V	1.45	1.67	1.9	-	1.67	-	V
	V+ = 15V	4.8	5	5.2	-	5	-	V
Trigger Current		-	0.5	-	-	0.5	-	μA
Threshold Current, Note 2, I_{TH}		-	0.1	0.25	-	0.1	0.25	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		-	0.1	-	-	0.1	-	mA
Control Voltage Level	V+ - 5V	2.9	3.33	3.8	2.6	3.33	4	V
	V+ = 15V	9.6	10	10.4	9	10	11	V
Output Voltage Drop: Low State, V_{OL}	V+ = 5V, I_{SINK} = 5mA	-	-	-	-	0.25	0.35	V
	I_{SINK} = 8mA	-	0.1	0.25	-	-	-	V
	V+ = 15V, I_{SINK} = 10mA	-	0.1	0.15	-	0.1	0.25	V
	I_{SINK} = 50mA	-	0.4	0.5	-	0.4	0.75	V
	I_{SINK} = 100mA	-	2.0	2.2	-	2.0	0.5	V
	I_{SINK} = 200mA	-	2.5	-	-	2.5	-	V
Output Voltage Droop: High State, V_{OH}	V+ = 5V, I_{SOURCE} =100mA	3.0	3.3	-	2.75	3.3	-	V
	V+ = 15V, I_{SOURCE} =100mA	13.0	13.3	-	12.75	13.3	-	V
	I_{SOURCE} = 200mA	-	12.5	-	-	12.5	-	V
Timing Error (Monostable):	R_1, R_2 = 1kΩ to 100kΩ, C = 0.1μF Tested at V+ = 5V, V+ = 15V	-	0.5	2	-	1	-	%
Frequency Drift with Temperature		-	30	100	-	50	-	p/m/°C
Drift with Supply Voltage		-	0.05	0.2	-	0.1	-	%/V
Ouput Rise Time, t_r		-	100	-	-	100	-	ns
Ouput Fall Time, t_f		-	100	-	-	100	-	ns

NOTES:

1. When the output is in a high state, the DC supply current is typically 1mA less than the low-state value.
2. The threshold current will determine the sum of the values of R_1 and R_2 to be used in Figure 15 (astable operation); the maximum total $R_1 + R_2$ = 20MΩ.



*WHERE x IS THE DECIMAL MULTIPLIER OF THE SUPPLY VOLTAGE

FIGURE 1. MINIMUM PULSE WIDTH vs MINIMUM TRIGGER VOLTAGE

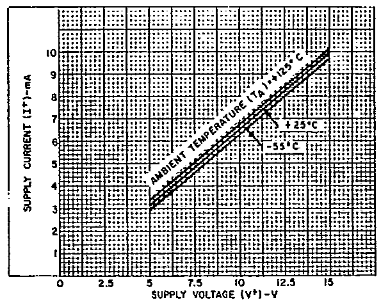


FIGURE 2. SUPPLY CURRENT vs SUPPLY VOLTAGE

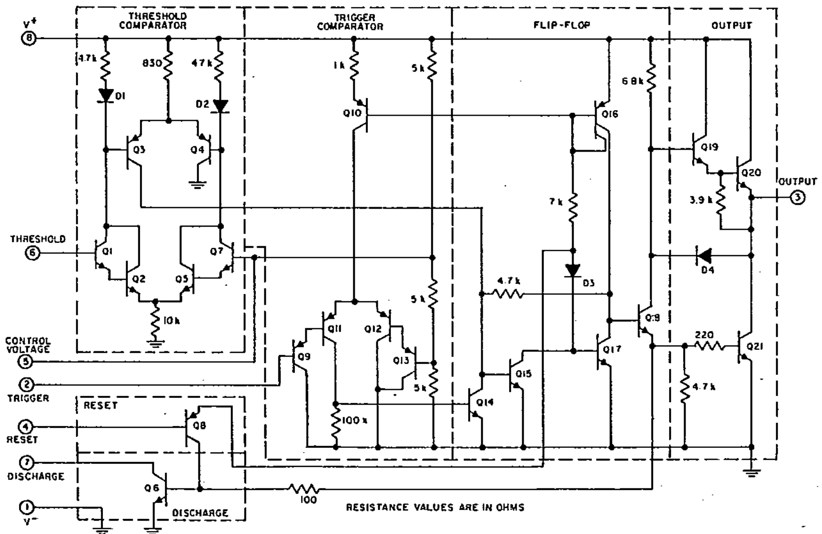


FIGURE 3. SCHEMATIC DIAGRAM OF THE CA555 AND CA555C

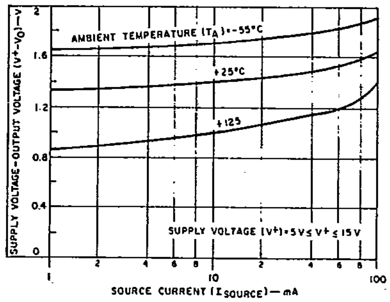


FIGURE 4. OUTPUT VOLTAGE DROP (HIGH STATE) vs SOURCE CURRENT

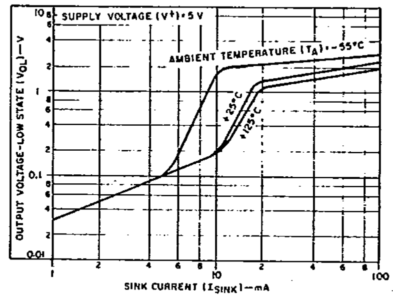


FIGURE 5. OUTPUT VOLTAGE-LOW STATE vs SINK CURRENT AT V+ = 5V

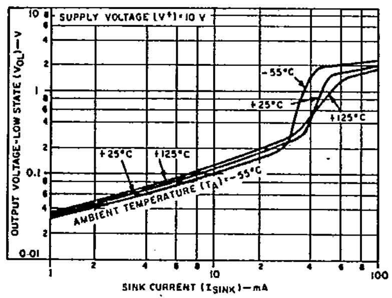


FIGURE 6. OUTPUT VOLTAGE-LOW STATE vs SINK CURRENT AT V+ = 10V

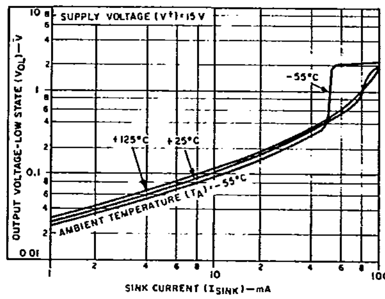


FIGURE 7. OUTPUT VOLTAGE-LOW STATE vs SINK CURRENT AT V+ = 15V

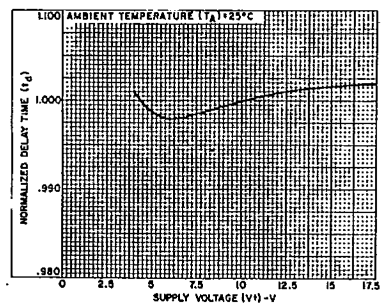


FIGURE 8. DELAY TIME vs SUPPLY VOLTAGE

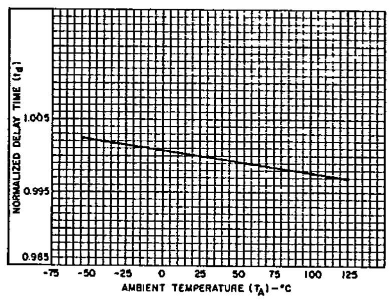
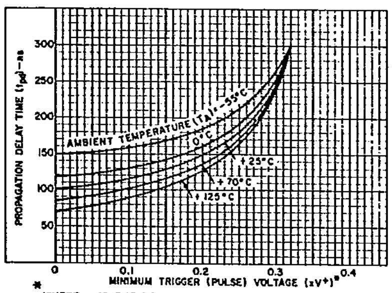


FIGURE 9. DELAY TIME vs TEMPERATURE



* WHERE x IS THE DECIMAL MULTIPLIER OF THE SUPPLY VOLTAGE

FIGURE 10. PROPAGATION DELAY TIME vs TRIGGER VOLTAGE

Typical Applications

Reset Timer (Monostable Operation)

Figure 11 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.

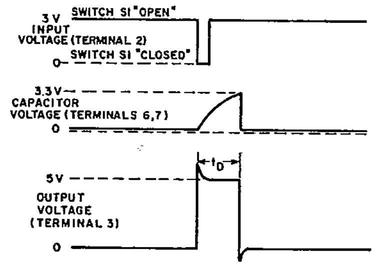
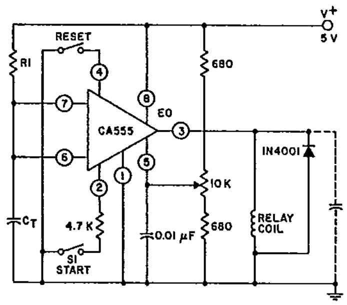


FIGURE 12. TYPICAL WAVEFORMS FOR RESET TIMER



ALL RESISTANCE VALUES ARE IN OHMS

FIGURE 11. RESET TIMER (MONOSTABLE OPERATION)

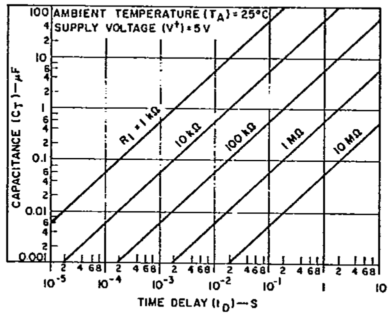


FIGURE 13. TIME DELAY vs RESISTANCE AND CAPACITANCE

Since the charge rate and threshold level of the are both directly proportional to V+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1V change in V+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Figure 12 shows the typical waveforms generated during this mode of operation, and Figure 13 gives the family of time delay curves with variations in R_1 and C_T.

Repeat Cycle Timer (Astable Operation)

Figure 14 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R1 and R2.

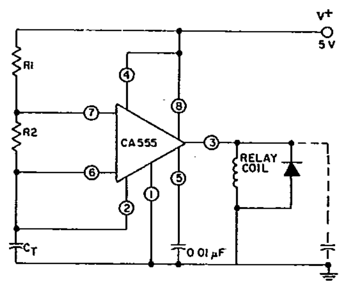


FIGURE 14. REPEAT CYCLE TIMER (ASTABLE OPERATIONAL)

$$T = 0.693\,(R_1 + 2R_2)\,C_T = t_1 + t_2$$

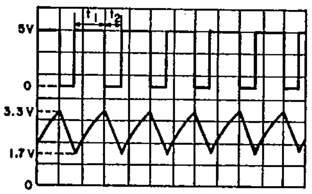
where $t_1 = 0.693\,(R_1 = R_2)\,C_T$

and $t2 = 0.693\,(R2)\,CT$

the duty cycle is:

$$\frac{t_2}{t_1 + t_2} = \frac{R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Figure 15. Figure 16 give the family of curves of free running frequency with variations in the value of $(R_1 + 2R_2)$ and C_T.



Top Trace: Output voltage (2V/div. and 0.5 ms/div.)
Bottom Trace: Capacitor voltage (1 V/div. and 0.5 ms/div.)

FIGURE 15. TYPICAL WAVEFORMS FOR REPEAT CYCLE TIMER

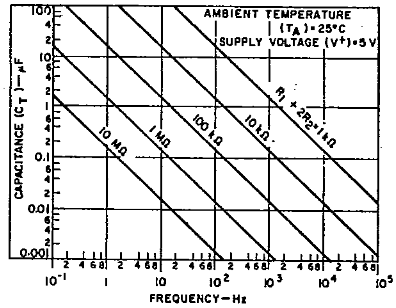


FIGURE 16. FREE RUNNING FREQUENCY OF REPEAT CYCLE TIMER WITH VARIATION IN CAPACITANCE AND RESISTANCE