National Semiconductor

March 1988

MM54C906/MM74C906
Hex Open Drain N-Channel Buffers
MM54C907/MM74C907
Hex Open Drain P-Channel Buffers

General Description

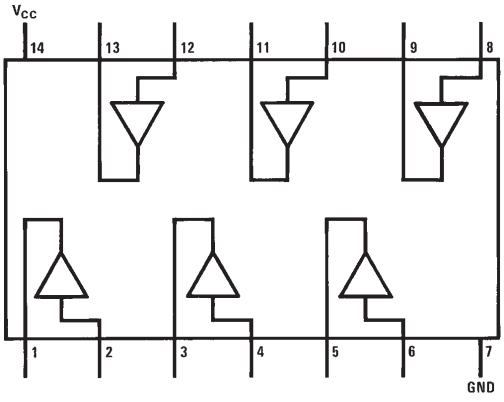
These buffers employ monolithic CMOS technology in achieving open drain outputs. The MM54C906/MM74C906 consists of six inverters driving six N-channel devices; and the MM54C907/MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

Features

- Wide supply voltage range — 3V to 15V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} (typ.)
- High current sourcing and sinking open drain outputs

Connection and Logic Diagrams

Dual-In-Line Package



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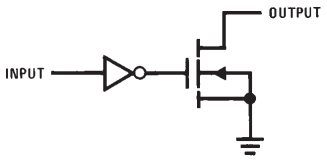
Top View

Order Number MM54C906, MM54C907, MM74C906 or MM74C907

MM54C906/MM74C906



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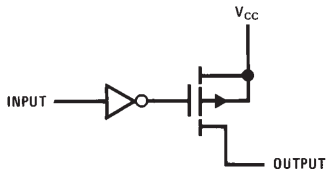
MM54C907/MM74C907



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  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$-0.3V$ to $V_{CC} + 0.3V$
Voltage at Any Output Pin	
MM54C906/MM74C906	$-0.3V$ to $+18V$
MM54C907/MM74C907	$V_{CC} - 18$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C906/MM54C907	$-55°C$ to $+125°C$
MM74C906/MM74C907	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$, Output Open		0.05	15	μA
	Output Leakage MM54C906	$V_{CC} = 4.5V$, $V_{IN} = V_{CC} - 1.5V$ $V_{CC} = 4.5V$, $V_{OUT} = 18V$		0.005	5	μA
	MM74C906	$V_{CC} = 4.75V$, $V_{IN} = V_{CC} - 1.5V$ $V_{CC} = 4.75V$, $V_{OUT} = 18V$		0.005	5	μA
	MM54C907	$V_{CC} = 4.5V$, $V_{IN} = 1V + 0.1\ V_{CC}$ $V_{CC} = 4.5V$, $V_{OUT} = V_{CC} - 18V$		0.005	5	μA
	MM74C907	$V_{CC} = 4.75V$, $V_{IN} = 1V + 0.1\ V_{CC}$ $V_{CC} = 4.75V$, $V_{OUT} = V_{CC} - 18V$		0.005	5	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5V$ $V_{CC} - 1.5V$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
OUTPUT DRIVE CURRENT						
	MM54C906	$V_{CC} = 4.5V$, $V_{IN} = 1V + 0.1\ V_{CC}$ $V_{CC} = 4.5V$, $V_{OUT} = 0.5V$ $V_{CC} = 4.5V$, $V_{OUT} = 1.0V$	 2.1 4.2	 8.0 12.0		 mA mA
	MM74C906	$V_{CC} = 4.75V$, $V_{IN} = 1V + 0.1\ V_{CC}$ $V_{CC} = 4.75V$, $V_{OUT} = 0.5V$ $V_{CC} = 4.75V$, $V_{OUT} = 1.0V$	 2.1 4.2	 8.0 12.0		 mA mA
	MM54C907	$V_{CC} = 4.5V$, $V_{IN} = V_{CC} - 1.5V$ $V_{CC} = 4.5V$, $V_{OUT} = V_{CC} - 0.5V$ $V_{CC} = 4.5V$, $V_{OUT} = V_{CC} - 1V$	 -1.05 -2.1	 -1.5 -3.0		 mA mA
	MM74C907	$V_{CC} = 4.75V$, $V_{IN} = V_{CC} - 1.5V$ $V_{CC} = 4.75V$, $V_{OUT} = V_{CC} - 0.5V$ $V_{CC} = 4.75V$, $V_{OUT} = V_{CC} - 1V$	 -1.05 -2.1	 -1.5 -3.0		 mA mA
	MM54C906/MM74C906	$V_{CC} = 10V$, $V_{IN} = 2V$ $V_{CC} = 10V$, $V_{OUT} = 0.5V$ $V_{CC} = 10V$, $V_{OUT} = 1V$	 4.2 8.4	 -20 -30		 mA mA
	MM54C907/MM74C907	$V_{CC} = 10V$, $V_{IN} = 8V$ $V_{CC} = 10V$, $V_{OUT} = 9.5V$ $V_{CC} = 10V$, $V_{OUT} = 9V$	 -2.1 -4.2	 -4.0 -8.0		 mA mA

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$, R = 10k			150	ns
		$V_{CC} = 10V$, R = 10k			75	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$ (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$ (Note 4)			75 + 0.7 RC	ns
t_{pd}	Propagation Delay Time to a Logical "1"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$ (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$ (Note 4)			75 + 0.7 RC	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$, R = 10k			150	ns
		$V_{CC} = 10V$, R = 10k			75	ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{OUT}	Output Capacity	(Note 2)		20		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		30		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

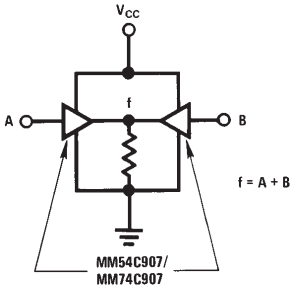
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90. (Assumes outputs are open).

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capacity (C_{OUT}).

Typical Applications

Wire OR Gate



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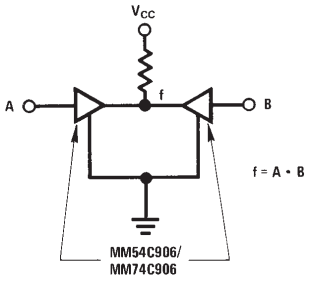
Note: Can be extended to more than 2 inputs.

Wire AND Gate



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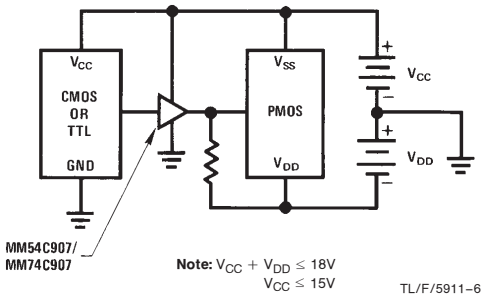
Note: Can be extended to more than 2 inputs.

CMOS or TTL to PMOS Interface



Note: $V_{CC} + V_{DD} \leq 18V$
$V_{CC} \leq 15V$

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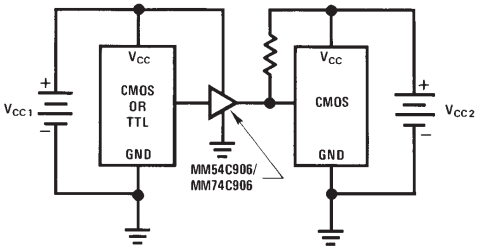
CMOS or TTL to CMOS at a Higher V_{CC}



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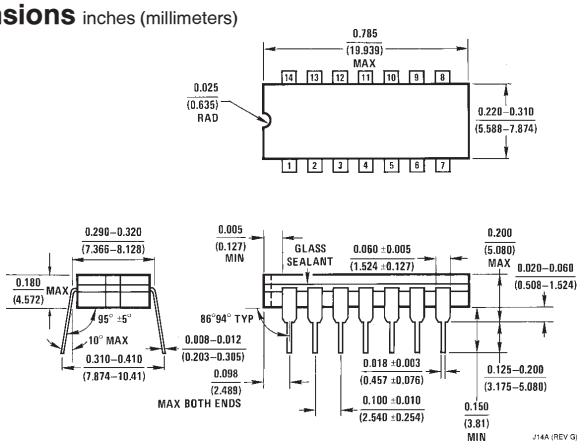
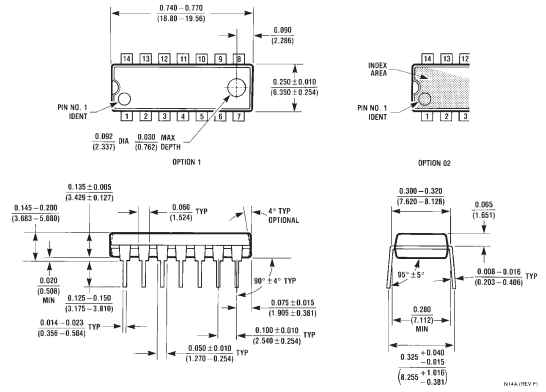
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C906J, MM54C907J, MM74C906J, MM74C907J
NS Package Number J14A



Molded Dual-In-Line Package (N)
Order Number MM54C906N, MM54C907N, MM74C906N or MM74C907N
NS Package Number N14A

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408