

# COS/MOS INTEGRATED CIRCUITS (continued)

## HBC/HBF 4000A series (continued)

TYPE	DESCRIPTION	• PROPAG. DELAY TIME $t_{PHL}/t_{PLH}$ (ns)	• OUT. DRIVE CURRENT N-CHANNEL SINK $I_{DN}$ (mA)	• OUT. DRIVE CURRENT P-CHANNEL SOURCE $I_{DP}$ (mA)	• CLOCK FREQUENCY $f_{max}$ (MHz)	PACKAGE
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### Shift registers

#### Static

4006A	18-stage static shift register	125	0.5	-0.3	5	DIP H, L, P, V,
4014A	8-stage static shift register	100	0.5	-0.44	5	DIP K, M, Q, W
4015A	Dual 4-stage static shift register	100	0.5	-0.44	5	DIP K, M, Q, W
4021A	8-stage static shift register	100	0.5	-0.44	5	DIP K, M, Q, W
4031A	64-stage static shift register	200	10	-1.5	4	DIP K, M, Q, W

#### Dynamic

4062A*	200-stage dynamic shift register	—	—	—	—	DIP K, W
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#### Parallel-In/Parallel-Out

4034A	MSI 8-stage static shift register	240	0.5	-0.25	5	DIP U, X
4035A	4-stage parallel in/out shift register	100	2.5	-1.3	5	DIP K, M, Q, W

### Counters

#### Binary/Ripple

4020A	14-stage binary/ripple counter	150	0.6	-0.5	7	DIP K, M, Q, W
4024A	7-stage binary counter	125	1	-0.7	7	DIP H, L, P, V
4040A	12-stage binary/ripple counter	125	1	-1	10	DIP K, M, Q, W
4045A	21-stage counter	—	6	-6	10	DIP K, M, Q, W
4060A	14-stage ripple-carry binary counter/ divider and oscillator	—	0.75	-0.5	4	DIP K, M, Q, W

#### Synchronous

4017A	Decade counter/divider	125	1	-1	5	DIP K, M, Q, W
4018A	Presetable divide-by "N" counter	125	1	-1	5	DIP K, M, Q, W
4022A	Divide-by-8-counter/divider	125	1	-0.8	5	DIP K, M, Q, W
4059A*	Programmable divide-by-"N" counter	140	12	-1.5	5	DIP U, X

\* Coming soon •  $V_{DD} = 10$  V