December 2009

AR8236 Six-Port Fast Ethernet Switch

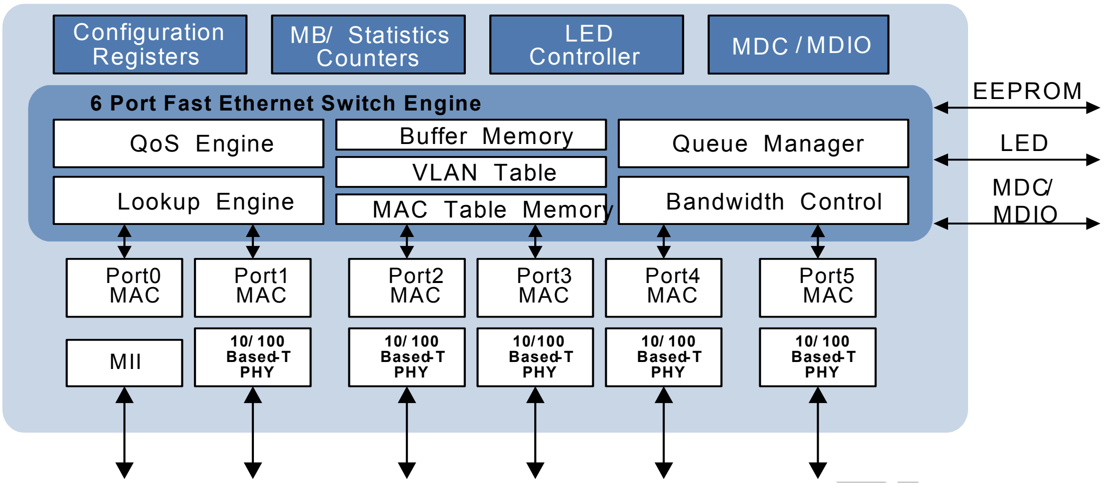
General Description

The AR8236 is a highly integrated Six-port Fast Ethernet switch with non-blocking switch fabric, a high-performance lookup unit with 1024 MAC address, 16 VLAN table, and a four-traffic class Quality of Service (QoS) engine. The AR8236 has the flexibility to support various networking applications. The AR8236 support many offload functions to increase the system performance. The AR8236 is designed for cost sensitive switch applications in wireless AP router, home gateway, and xDSL/PON/cable modem platform. The Fast Ethernet in the AR8236 complies fully with IEEE 802.3 standards. The AR8236 implements power saving techniques to facilitate low power consumption. The AR8236 is designed to work in all environments. True Plug-n-Play is supported with Auto-Crossover, Auto Polarity, and Auto-Negotiation in PHYs.

AR8236 Features

- Single-chip six-port Fast Ethernet QoS switch
- Single-chip six-port Fast Ethernet QoS switch controller with:
  - 5 port 10/100 UTP + 1 port MII MAC
  - 4 port 10/100 UTP + 2 port RMII MAC
  - 4 port 10/100 UTP + 1 port RMII MAC + 1 RMII PHY
- QoS support with four traffic classes based on arrival port, IEEE802.1p, IPv4 TOS, IPv6 TC and Destination MAC Address
- Supports strict priority, WRR, and mix mode (1 SP + 3 WRR or 2 SP + 2 WRR)
- Full IEEE 802.1Q VLAN ID processing per port and VLAN tagging for 16 VLAN IDs; and port based VLANs supported
- Support VLAN tag insert or remove function on per-port basis
- Support QinQ double tag
- IGMPv1/v2/v3 and MLDv1/v2 Snooping with hardware join and fast leave function
- Port states & BPDU handling support IEEE802.1D Spanning Tree Protocol
- High performance lookup engine with 1024 MAC Address with automatic learning and aging and support for static addresses
- Support 40 MIB counters per port
- Autocast MIB counters to cpu port
- Support ingress & egress rate limit
- Broadcast storm Suppression
- Supports port mirror
- Support MAC and PHY loopback function for diagnosis
- Fully compliant with IEEE 802.3/802.3u auto-negotiation function
- Flow control fully supported IEEE 802.3x flow control for full duplex and back pressure for half duplex
- Supports port lock function
- Supports hardware looping detection
- Power saving on no link and low traffic rate for 10Base-T
- Supports Jumbo Frames

AR8236 System Block Diagram



1. Pin Descriptions

This section contains a listing of the pin descriptions (see Table 1-1 on page 7 and Figure 1-1 on page 6).

The following nomenclature is used for signal names:

_L	At the end of the signal name, indicates active low signals
N_ n_	Near the end of the signal name, indicates active low signals
N	At the end of the signal name indicates the negative side of a differential signal
NC	No connection is made from this pin to the internal die
P	At the end of the signal name, indicates the positive side of a differential signal

The following nomenclature is used for signal types described in Table 1-1 on page 7:

D	Open drain for digital pads
I	Digital input signal
I/O	Digital bidirectional signal
IA	Analog input signal
IH	Digital input with hysteresis
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
O	Digital output signal
OA	Analog output signal
P	A power or ground signal
PD	Internal pull-down for digital input
PU	Internal pull-up for digital input

Figure 1-1shows the package pinout.

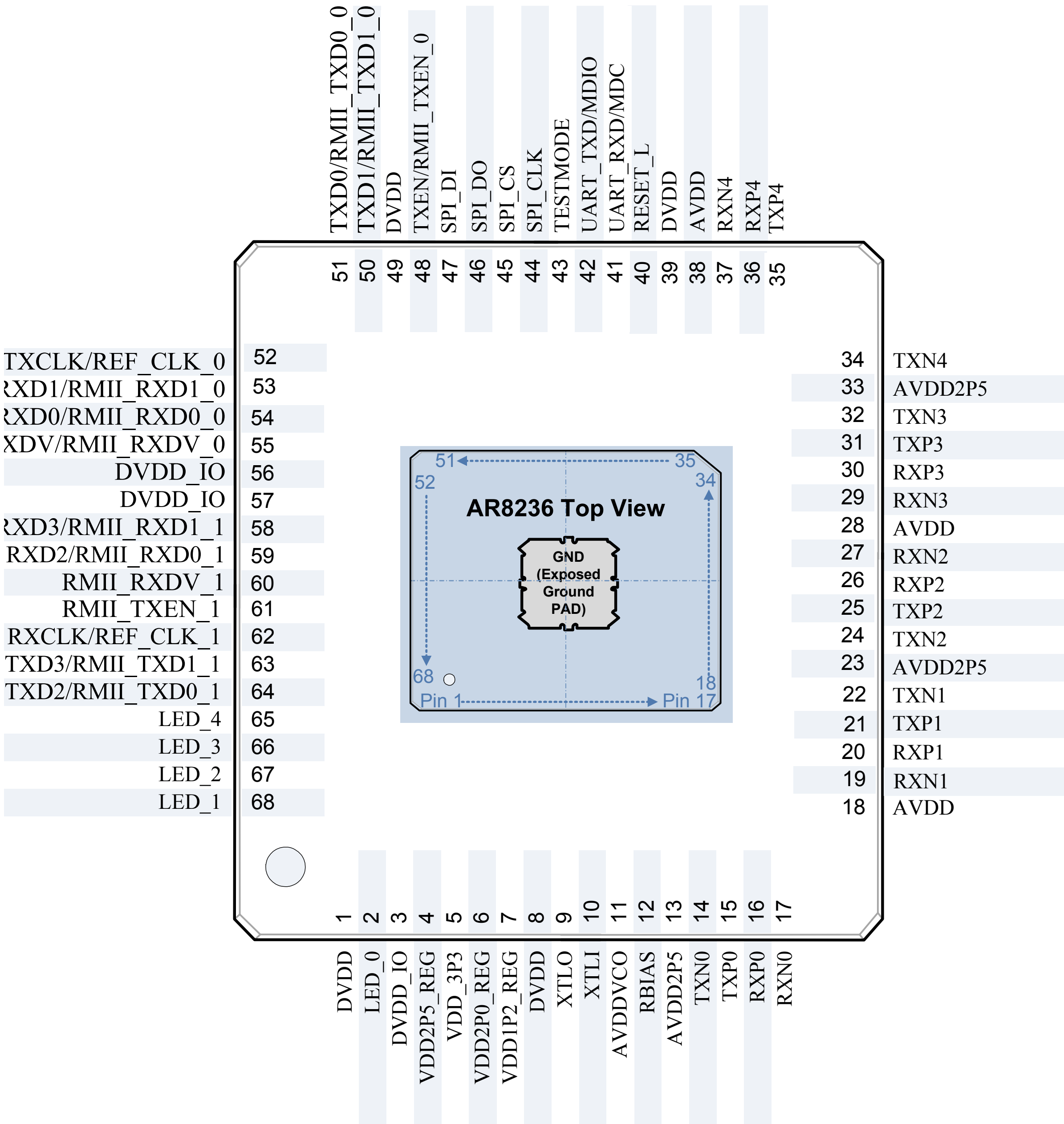


Figure 1-1. **68 pin QFN Package Pinout**

Table 1-1. **Signal to Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
Media Connection			
TXP0	15	IA, OA	Media-dependent interface, MDI[4:0]: Transmitter output positive/negative.
TXN0	14		
TXP1	21	IA, OA	
TXN1	22		
TXP2	25	IA, OA	
TXN2	24		
TXP3	31	IA, OA	
TXN3	32		
TXP4	35	IA, OA	
TXN4	34		
RXP0	16	IA, OA	Media-dependent interface, MDI[4:0]: Receive input positive/negative.
RXN0	17		
RXP1	20	IA, OA	
RXN1	19		
RXP2	26	IA, OA	
RXN2	27		
RXP3	30	IA, OA	
RXN3	29		
RXP4	36	IA, OA	
RXN4	37		
MAC 0/CPU port MII/RMII interface			
RXCLK	62	I/O, PD	MII receive clock. This is output clock from MAC0 when AR8236 operates at PHY type interface. It can be 25MHz/2.5MHz depending on the operating speed.
RXD0	54	I/O, PD	MII receive data or configuration; recommend adding a 22 Ohm damping resistor. these are output signals from MAC 0. The RXD[3:0]_0 are used as data input when operating in MII mode. The reference clock for these output signals will be as follows: 1. RXCLK_0 (pin 57):MII PHY type interface and MII MAC type interface.
RXD1	53	I/O, PD	
RXD2	59	I/O, PD	
RXD3	58	I/O, PU	
RXDV	55	I/O, PD	MII receive data valid. This is output signal for MAC0.
TXCLK	52	I/O, PD	This pin is the reference clock for TXD[3:0]_0 when operating in an MII interface. The clock will be output signal at PHY type interface and will be input signal at MAC type interface.. It also supports 50MHz clock input(Turbo-MII) when operating in MII mode MAC type interface.

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
TXEN	48	I, PD	MII transmit enable, this is input signal for the MAC0.
TXD0	51	I, PD	MII transmit data, these are input signals for MAC0. The TXD[3:0]_0 are used as data input when operating in an MII mode. The reference clock for these input signals will be: 1. TXCLK (pin 52): MII MAC type and PHY type interface
TXD1	50	I, PD	
TXD2	64	I, PD	
TXD3	63	I, PD	
RMII_RXDV_1	60	I/O	RMII receive data valid. This is the output signal for PHY4
RMII_TXEN_1	61	I,PD	RMII transmit enable. This is the input signal for PHY4
LED			
LED_0	2	O, D	PHY0 LED output. LED behavior can be configurable, see the LED Control Registers 0x00B0 ~ 0x00BC.
LED_1	68	O, D	PHY1 LED output. LED behavior can be configurable, see the LED Control Registers 0x00B0 ~ 0x00BC.
LED_2	67	O, D	PHY2 LED output. LED behavior can be configurable, see the LED Control Registers 0x00B0 ~ 0x00BC.
LED_3	66	O, D	PHY3 LED output. LED behavior can be configurable, see the LED Control Registers 0x00B0 ~ 0x00BC.
LED_4	65	O, D	WAN port LED output. The LED behavior can be configurable, see the LED Control Registers 0x00B0 ~ 0x00BC
UART/MDIO and SPI EEPROM			
SPI_CLK	44	I/O, PD	SPI Clock or configuration
SPI_CS	45	I/O, PD	SPI Chip select configuration
SPI_DI	47	I, PD	SPI Data input
SPI_DO	46	I/O, PU	SPI Data out or configuration
UART_RXD/MDC	41	I, PU	Management data clock reference
UART_TXD/MDIO	42	I/O	Management data
Miscellaneous			
RBIAS	12	OA	Connect 2.4 K Ω resistor to GND. The resistor value is adjustable depending on the PCB.
RESET_L	40	IH	Chip reset, active low. The active low duration must be greater than 10ms.
TESTMODE	43	I	Test Mode
XTLI	10	IA	Crystal oscillator input, connect a 27 pF capacitor to GND. An external 25 MHz clock with swing from 0–1 V can be injected to this pin. When external clock source is used, the 27 pF capacitor should be removed from this pin and the 27 pF capacitor at XTLO should be maintained.
XTLO	9	OA	Crystal oscillator output, connect a 27 pF capacitor to GND

Symbol	Pin	Type	Description
Power			
AVDD	18, 28, 38	P	Analog 1.2 V
AVDD2P5	13, 23, 33	P	Analog 2.5 V
DVDD	1, 8, 39, 49	P	Digital 1.2 V
DVDD_IO	3, 56, 57	P	Digital I/O V
VDD3P3	5	P	3.3 V power supply. The 3.3 V power input is used to generate the 2.5 V regulator output. If 2.5 V is generated by an external circuit, the this pin must be connected to the external 2.5 V source.
VDD25_REG	4	AO	2.5 V regulator output. A 1 uF and several 0.1 uF capacitors are needed to stabilize this voltage.
VDD12_REG	7	OA	1.2 V regulator output. A 1 uF and several 0.1 uF capacitors are needed to stabilize this voltage
VDD20_REG	6	P	The power source for transformer central tap. When using external 3.3V as power input, the VDD20_REG will be 2.3V. When using external 2.6V as power input, the VEE20_REG will be 2.0V. A 1 uF and several 0.1 uF capacitors are needed to stabilize this voltage.
AVDDVCO	11	OA	Analog 1.2 V for PLL.
GND		P	Exposed Ground Pad at the bottom of the chip

The following table shows the interface summary relative to the AR8236's different modes.

Table 1-2. **MACO MII Pin Multiplex Table**

Pin name	Pin	MII PHY Mode	MII MAC Mode	MACO RMII
TXCLK	52	txclk_0(O)	rxclk_0(I)	ref_clk_0(O)
TXEN	48	txen_0	rxdv_0	txen_0
TXD0	51	txd0_0	rxd0_0	txd0_0
TXD1	50	txd1_0	rxd1_0	txd1_0
TXD2	64	txd2_0	rxd2_0	
TXD3	63	txd3_0	rxd3_0	
RXCLK	62	rxclk_0(O)	txclk_0(I)	
RXDV	55	rxdv_0	txen_0	rxdv_0
RXD0	54	rxd0_0	txd0_0	rxd0_0
RXD1	53	rxd1_0	txd1_0	rxd1_0
RXD2	59	rxd2_0	txd2_0	
RXD3	58	rxd3_0	txd3_0	
RMII_RXDV_1	60			
RMII_TXEN_1	61			

ummary relative to the AR8236's different modes.

Table 1-3. **MAC5 RMII MII PHY Mode Multiplex Table**

Pin name	Pin	MAC5 MII PHY Mode	MAC 5 RMII
TXCLK	52	txclk_5(O)	
TXEN	48		
TXD0	51	txd0_5	
TXD1	50	txd1_5	
TXD2	64	txd2_5	txd0_5
TXD3	63	txd3_5	txd1_5
RXCLK	62	rxclk_5(O)	ref_clk_5(O)
RXDV	55		
RXD0	54	rxd0_5	
RXD1	53	rxd1_5	
RXD2	59	rxd2_5	rxd0_5
RXD3	58	rxd3_5	rxd1_5
RMII_RXDV_1	60	rxdv_5	rxdv_5
RMII_TXEN_1	61	txen_5	txen_5

ummary relative to the AR8236's different modes.

Table 1-4. **PHY4 MII Pin Multiplex Table**

Pin name	Pin	PHY4 MII Mode	PHY4 RMII
TXCLK	52	phy_txclk_4(O)	
TXEN	48		
TXD0	51	phy_txd0_4	
TXD1	50	phy_txd1_4	
TXD2	64	phy_txd2_4	phy_txd0_4
TXD3	63	phy_txd3_4	phy_txd1_4
RXCLK	62	phy_rxclk_4(O)	ref_clk_4(O)
RXDV	55		
RXD0	54	phy_rxd0_4	
RXD1	53	phy_rxd1_4	
RXD2	59	phy_rxd2_4	phy_rxd0_4
RXD3	58	phy_rxd3_4	phyrxd1_4

Table 1-4. **PHY4 MII Pin Multiplex Table**

Pin name	Pin	PHY4 MII Mode	PHY4 RMII
RMII_RXDV_1	60	phy_rxdv_4	phy_rxdv_4
RMII_TXEN_1	61	phy_txen_4	phy_txen_4

2. Functional Description

The AR8236 supports many operating modes that can be configured using a low-cost serial EEPROM and/or the MDC/MDIO interface.

The AR8236 also supports a CPU header mode that appends two bytes to each frame. The CPU can use headers to configure the switch register, the address lookup table, VLAN and receive auto-cast MIB frames. The first port (port0) supports a MAC interface and can be configured in MII-PHY or RMII-PHY mode to connect to an external management CPU or an integrated CPU in a routing or xDSL/lln/PON engine.

The AR8236 contains a 1K entry address lookup table that employs two entries per bucket to avoid hash collision and maintain non-blocking forwarding performance. The address table provides read/write accesses from the serial and CPU interfaces; each entry can be configured as a static entry. The AR8236 supports 16 VLAN entries configurable as port-based VLANs or 802.1Q tag-based VLANs. The AR8236AR8236 also supports a QinQ function.

To provide non-blocking switching performance in all traffic environments, the AR8236 supports several types of QoS function with four-level priority queues based on port, IEEE 802.1p, IPv4 DSCP, IPv6 TC, 802.1Q VID, or MAC address. Back pressure and pause frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion. Meeting today's service provider requirements, the AR8236 switch uses the latest Atheros QoS switch architecture that supports ingress policing and egress rate limiting.

The AR8236 device supports IPv4 IGMP snooping and Ipv6 MLD snooping to significantly improve the performance of streaming media and other bandwidth-intensive IP multicast applications.

IEEE 802.3x full duplex flow control and back-pressure half duplex flow control schemes are supported to ensure zero packet loss during temporary traffic congestion. A broadcast storm control mechanism prevents the packets from flooding into other parts of the network. The AR8236 device has an intelligent switch engine to prevent Head-of- Line blocking problems on a per-CoS basis for each port.

AR8236 router application. This solution is a complete end-to-end 802.AP RJ-45-to-air router 802.11n wireless network processing solution. The AR8236 eliminates the external PHY for the WAN interface. Note that the AR8236 can also work as a one-arm router.

2.1 Basic Switch Operation

The AR8236 automatically learns the port number of an attached end station by looking at the source MAC address of all incoming packets at wire speed. If the source address is not found in the address table, the AR8236 device adds it to the table. Once the MAC address/port number mapping is learned, all packets directed to that end station's MAC address are forwarded to the learned port number only. When the AR8236 device receives incoming packets from one of its ports, it searches in its address table for the destination MAC address, then forwards the packet to the appropriate port within the VLAN group. If the destination MAC address is not found (i.e. A new, unlearned MAC address), the AR8236 handles the packet as a broadcast packet and transmits it to all ports within the VLAN group except to the port where it came in.

2.1.1 Lookup Engine

The AR8236 lookup engine or address resolution logic (ARL) retrieves the DA and SA from each frame received from each port. The ARL performs all address searching, learning, and aging functions at wire speed. The ARL engine uses a hashing algorithm for fast storage and retrieval of address entries. To avoid hash collision, the AR8236 uses a two entry bin per hash location that stores up to two MAC addresses at each hash location. The address database is stored in the embedded SRAM and has a size of 1024 entries.

2.1.2 Automatic Address Learning

Up to 1024 MAC address/port number mappings can be stored in the address table. A two-way hash algorithm allows a maximum of two different addresses with the same hash key to be stored simultaneously. The AR8236 searches for the SA of an incoming packet in the address table. If the SA is not found, the address is hashed and stored in the first empty bin found at the hashed location. If all two address bins are full, each entry's age time is examined to select the least recently used bin. If the SA is found, the aging value of the corresponding entry is reset to 0. If the DA is PAUSE, the AR8236 automatically disables the learning process.

2.1.3 Automatic Address Aging

Address aging supports network topology changes such as an end station disconnecting from the network or an address moving from one port to another. An address is removed (aged-out) from the address database after a specified amount of time since the last time it appeared in an incoming frame source address. The AR8236 has a default aging time of 5 minutes, but can be set in 17-second increments to a maximum of 20,000 minutes.

2.2 Media Access Controllers (MAC)

The AR8236 integrates six independent Fast Ethernet MACs that perform all functions in the IEEE 802.3 specifications, e.g., frame formatting, frame stripping, CRC checking, CSMA/CD, collision handling, and backpressure flow control. Each MAC supports 10 Mbps, or 100 Mbps operation in either fullduplex or half-duplex mode.

2.2.4 Port Status Configuration

The AR8236 supports flexible port status configuration on a group or per-port basis. Each port has status registers that provide information about the port interface. The first port (port 0) MAC behaves as a PHY to allow a direct connection to an external MAC (e.g. A management CPU or a MAC inside a router). In this mode, the AR8236 drives interface clocks from a RXCLK_0 pin at the desired frequency. Only full-duplex modes are supported and need to match the mode of the link partner's MAC.

2.2.1 Full-Duplex Flow Control

The AR8236 device supports IEEE 802.3x fullduplex flow control, force-mode full-duplex flow control, and half-duplex backpressure. If the link partner supports auto-negotiation, the 802.3x full-duplex flow control is autonegotiated between the remote node and the AR8236. If the full-duplex flow control is enabled, when the free buffer space is almost empty, the AR8236 sends out an IEEE 802.3x compliant PAUSE to stop the remote device from sending more frames.

2.2.2 Half-Duplex Flow Control

Half-duplex flow control regulates the remote station to avoid dropping packets in network congestion. Back pressure is supported for half duplex operations. When the free buffer space is almost empty, the AR8236 device transmits a jam pattern on the port and forces a collision. If the half-duplex flow control mode is not set, the incoming packet is dropped if there is no buffer space available.

2.2.3 Inter-Packet Gap (IPG)

The IPG is the idle time between any to successive packets from the same port. The typical IPG is 9.6 ms for 10 Mbps Ethernet and 960 ns for 100 Mbps Ethernet.

2.2.4 Illegal Frames

The AR8236 discards all illegal frames such as CRC error, oversized packets (length greater than maximum length), and runt packets (length less than 64 bytes).

2.3 Register Access

The MDIO interface allows users to access the Switch internal registers and MII registers. The figure shown below is the format to access MII registers in the embedded PHY. The Phy-address is from 0x00 up to 0x04. The Op code “10” indicates the read command and “01” is the write command.

start	Op	2'b0	Phy_addr[2:0]	reg_addr [4:0]	TA [1:0]	Data[15:0]

The Switch internal registers are 32-bits wide, but the MDIO access is only 16-bits wide. So it needs 2 times access to complete the internal registers access. Moreover the address spacing is more than 10 bits supported by MDIO, So it needs to write the upper address bits to internal registers, like page mode access method. For example, the register address bit 18 to 9 are treated as page address and will be written out first as High_addr[9:0], refer the Table 1 below. Then the register could be accessed via Table 2, where Low_addr[7:1] is the address bit [8:2] of register and Low_add[0] is 0 for Data[15:0] or Low_addr[0] is 1 for Data[31:16].

1. First, access high-address command.

Where High_Addr[9:0] is address[18:9] fo register

start	Op	2'b11	8'b0	TA [1:0]	6'b0	High_addr[9:0]

2. Second, re-access low-address command.

Table 2: where Low_Addr[7:1] is address [8:2] of register and Low_Addr[0] is 0 for Data[15:0], 1 for Data[31:16]

start	Op	2'b10	Low_addr[7:0]	TA [1:0]	Data[15:0]

2.4 LED Control

There are a total of 2 LED control rules, one for PHY0 through PHY3. The other is for the control of PHY4. Each PHY port has 1 LED, the default behaviour of these LEDs are link_activity. Other LED behaviours can be programed by modify the LED control register. Refer the register offset 0x0B0 ~ 0x0B4.

Each LED can be controlled by 16-bits shown in the following table.

Table 2-1. **LED Control**

Bit	Name	Description
15:14	PATTERN_EN	2’b00: LED always off 2’b01: LED blinking at 4 Hz 2’b10: LED always on 2’b11: LED controlled by the following bits
13	FULL_LIGHT_EN	1’b1: LED will light when link up in full-duplex
12	HALF_LIGHT_EN	1’b1: LED will light when link up at half-duplex
11	POWER_ON_LIGHT_EN	1’b1: module should enter POWER_ON_RESET status after reset.
10	LINK_1000M_LIGHT_EN	1’b1: LED will light when link up at 1000 Mbps
9	LINK_100M_LIGHT_EN	1’b1: LED will light when link up at 100 Mbps
8	LINK_10M_LIGHT_EN	1’b1: LED will light when link up at 10 Mbps
7	COL_BLINK_EN	1’b1: LED will blink when collision is detected
6	Reserved	Must be 1’b0
5	RX_BLINK_EN	1’b1: LED will blink when recieving frame
4	TX_BLINK_EN	1’b1: LED will blink when transmitting frame

3	Reserved	Must be 1'b0
2	LINKUP_OVER_EN	1'b1: RX/TX blinking should check with LINKUP speed, LINKUP LED is ON, allow blinking. Otherwise, OFF 1'b0: RX/TX blinking will ignore the LINKUP speed.
1:0	LED_BLINK_FREQ	LED blink frequency select 2'b00: 2 HZ 2'b01: 4 Hz 2'b10: 8 Hz if link up at 100Mbps, use 4 Hz if link up at 10 Mbps, use 2 Hz

Table 2-2. **LED Rule Default Value**

Bit	Name	LED_RULE_0/1
	Default Value	0xCB35
15:14	PATTERN_EN	2'b11
13	FULL_LIGHT_EN	1'b0
12	HALF_LIGHT_EN	1'b0
11	POWER_ON_LIGHT_EN	1'b1
10	LINK_1000M_LIGHT_EN	1'b0
9	LINK_100M_LIGHT_EN	1'b1
8	LINK_10M_LIGHT_EN	1'b1
7	COL_BLINK_EN	1'b0
6	Reserved	1'b0
5	RX_BLINK_EN	1'b1
4	TX_BLINK_EN	1'b1
3	Reserved	1'b0
2	LINKUP_OVER_EN	1'b1
1:0	LED_BLINK_RFREQ	1'b01: 4Hz

2.5 EEPROM Description

The AR8236 supports an optional external serial EEPROM device for programming its internal registers and phy registers. The EEPROM data will be read in once after reset. The AR8236 support 1K bits, 2K bits or 4K bits EEPROM devices. The external EEPROM device must be configured in x16 data organization mode.

The EEPROM device is read and processed in this way:

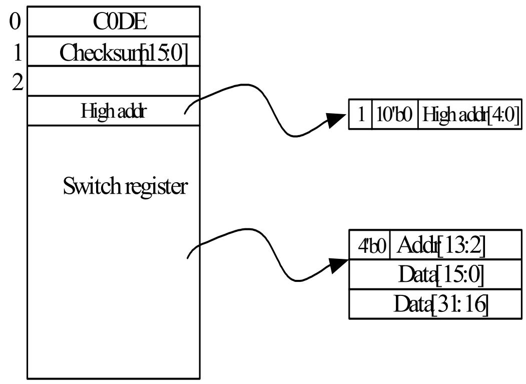
1.Start at EEPROM address 0x00, data in it should be 0xC0DE.

2.Read in address 0x01, is checksum result of EEPROM data.

3.read out next address, if bit15 is 1'b1, this address will set spi read high address in theAR8236. If bit 15 is 1'b0, this address is register address to be configured. Then the next to register address should be data[15:0] and data[31:16].

4.The last register to be configured in EEPROM must be register 0, and the LOAD_EEPROM bit must be set to 1'b0.

EEPROM Store:



2.6 VLANs

The AR8236 switch supports many VLAN options including IEEE 802.1Q and port-based VLANs. The AR8236 supports 16 VLAN entries, and the AR8236 device checks VLAN port membership from the VLAN ID, extracted from the tag header of the frame. Table 2-18 shows the AR8236-supported 802.1Q modes. The port-based VLAN is enabled according to the user-defined PORT VID value. The AR8236 supports optional discards of tagged, untagged frames, and priority tagged frames. The AR8236 also supports untagging of the VLAN ID for packets going out on untagged ports on a per-port basis.

2.6.1 Port-Based VLAN

The AR8236 switch supports port-based VLAN functionality used for non-management frames when 802.1Q is disabled on the ingress port. When FORCE_PORT_VLAN_EN is enabled, non-management frames conform to portbased configurations even if 802.1Q is enabled on the ingress port. Each ingress port contains a register that restricts the output (or egress) ports to which it can to send frames. This port-based VLAN register has a field called PORT_VID_MEM that contains the port based setting. If bit 0 of a port's PORT_VID_MEM is set to a one, the port is allowed to send frames to Port 0, bit [2] for Port 2, and so on. At reset, the PORT_VID_MEM for each port is set to a value of all 1s, except for each port's own bit, which clears to zero. Note that the CPU port is port 0.

2.6.2 802.1Q VLANs

The AR8236 supports a maximum of 16 entries in the VLAN table. The device supports 16 VLANs — ID range from 0 to 4095. The AR8236 only supports shared VLAN learning (SVL). This means that forwarding decisions are based on the frame's destination MAC address, which should be unique among all VLANs.

2.6.3 Leaky VLAN

The AR8236 support leaky vlan to enable specific frames to be forwarded across VLAN boundary. Totally three types of frames can be leaked across VLAN boundry: Unicast, Multicast and ARP, among which Unicast and Mulicast leaky are port or MAC address based and ARP is port based.

2.6.4 Egress Mode

The AR8236 supports per port egress VLAN mode:

1. Tag mode
2. Untag mode

The frame sent out with tagged or untagged will depend on the egress mode setting. The following table shows the tagging or untagging frame on different egress mode.

Table 2-3. **Egress Mode Settings**

EG_VLAN_ MODE	Egress VID=untagged	Egress VID=Priority tagged	Egress VID= tagged
Tag	Egress port default VID	Egress port default VID	Egress VID
unmodify	untagged	Priority tagged	Egress VID

untag	untagged	untagged	untagged
hybrid	untagged	untagged	if(egress VID = egress port default VID) untagged; else tagged;

2.6.5 VLAN Table

The AR8236 supports a 16 VLAN membership table. It also supports the following commands to access the VLAN table:

1. Search one entry
2. Use getnext read out whole table
3. Loading and purging of an entry
4. Flush all entries, flush all of one port's entries

2.7 IEEE Port Security

The AR8236 supports 802.1Q security features. Its switch discards ingress frames that do not meet security requirements and ensures those frames that do meet the requirements are sent to the designated ports only. Levels of security can be set differently on each port, and options are processed using the ingress frame's VID:

Mode	Description
Secure	The frame is discarded if the frame's VID is not in the VLAN table or the ingress port is not a member of the VLAN. The frame is allowed to exit only the ports that are members of the frame's VLAN.
Check	The frame is discarded if the frame's VID is not in the VLAN table. The frame is allowed to exit only the ports that are members of the frame's VLAN.
Fallback	If the frame's VID is in the VLAN table, the frame can exit only ports that are members of the frame's VLAN. Otherwise the switch decides forwarding policy based on the port-based VLAN. If a frame arrives untagged, the AR8236 forwards based on the port-based VLAN even if the ingress port's 802.1Q mode is enabled.
Egress	The AR8236 supports port-based egress, both unmodified and force untagged.

In this application case, the ports work as:

Port Number	Description
Port 0	CPU Port
Port 1	LAN A
Port 2	
Port 3	LANB
Port 4	
Port 5	WAN Port

In the application case, all LAN ports can directly send frames to each other but not to the WAN port. The CPU can send frames to all ports. A LAN port must go through the CPU port to send frames to the WAN port. Similarly, the WAN port must also go through the CPU to send frames to LAN ports,. Normally a firewall application runs in the CPU, causing traffic between the LANs and WAN to go through the host CPU. Figure 2-1 shows an application case.

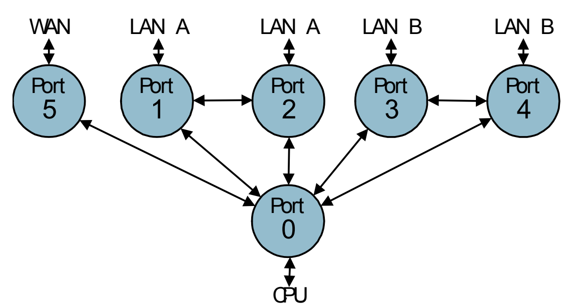


Figure 2-1. **Application Case**

2.7.1 Port Locking

The AR8236 supports port lock state in which a frame received with an SA that cannot be found in the ARL table or the registered egress port is the same as the ingress port, the frame will be dropped or redirected to the CPU port. In this way, the AR8236 can support MAC-based ingress control cooperated with LEARN_EN which can enable or disable the learning ability of a port. MAC-based egress control can be done by UNI_FLOOD_DP which can provide control if a frame with an unregistered unicast MAC address in its DA field can be egressed from a port.

2.7.2 802.1X

The AR8236 supports identifying EAPOL frames by their reserved group addresses. Combined with port security feature, the AR8236 can implement port based or MAC based access control.

Application Cases 1 and 2

Member	Application Case 1		Application Case 2	
	Ports	**Description**	**Ports**	**Description**
Ports	Each port configured in 802.1Q secure mode		Each port configured in 802.1Q secure mode	
	Ports	**Create For**	**Ports**	**Create For**
VLAN1	Port 0, 1, 2	Create for LAN A	Ports 0, 1, 2	LAN A
VLAN2	Ports 0, 3, 4	Create for LAN B	Ports 0, 3, 4	LAN B
VLAN3	Ports 0, 5	Create for WAN	—	—

2.8 Class/Quality of Service

The AR8236 switch identifies the packets' priority level based on several types of QoS priority information: port-based, 802.1p CoS, IPv4 TOS/Diffserv, and IPv6 TC. The AR8236 switch supports up to four queues per egress port. For tagged packets, the incoming packet priority can be mapped to one of the four CoS queues based on the priority field in the tag header or based on the result of classification lookup. For untagged packets, the CoS priority is derived either from a configurable field within the VLAN address tables or from the result of classification lookup. After the packets are mapped into an egress queue, they are forwarded using either strict priority or weighted fair queuing scheduler.

Mode	Description
Strict Priority (SP)	Any packets residing in the higher priority queues transmit first. Lower priority packets transmit once these queues are emptied.
Weighted Fair Queuing	Each queue is assigned a weight that determines how many packets are sent from each priority queue.
Mix Mode	The highest priority queue use SP and other queues conform to WRR at 4,2,1 weight

The AR8236 recognizes the QoS information of ingress frames and map to different egress priority levels. The AR8236 determines the priority of the frames based on DA, TOS/TC, VLAN, and port. Each has an enable bit that can be applied. When more than one type of priority is selected, the order in which the frame priority should be applied can be determined. Priority enable bits and select order bits are set by port base at 0x110 for port 0, 0x210 for port 1, and so on. When more than one priority enable bit is set to 1'b1, bits [7:0] in 0x110, 0x210, etc. (DA_PRI_SEL, IP_PRI_SEL, VLAN_PRI_SEL, PORT_PRI_SEL) can determine the order in which the frame priority should be applied. If *_PRI_SEL is set to 2'b0, frame priority is determined by that first. Otherwise, priority is determined by which *_PRI_SEL is set to 2'b01, then 2'b10, 2'b11, etc.

Priority Determined	Description
DA	Set DA_PRI_EN bit [18] to 1'b1 and add the address to the ARL table-set priority_over_en to 1'b1. ARL priority bits [59:58] can be used as DA priority.
TOS/TC	Set IP_PRI_EN bit [16] to 1'b1, and set the IP priority mapping register (0x60–0x6C).
VLAN	Set VLAN_PRI_EN (bit [17]) to 1'b1, and set the TAG priority mapping register (0x70).
Port's Default Authority	Set PORT_PRI_EN to 1'b1, and set port base register ING_PORT_PRIORITY (bits [19:28] in 0x108, 0x208, etc.).

When more than one priority enable bit is set to 1'b1, bits [7:0] in 0x110, 0x210, etc. (DA_PRI_SEL, IP_PRI_SEL, VLAN_PRI_SEL, PORT_PRI_SEL) can determine the order in which the frame priority should be applied. If *_PRI_SEL is set to 2'b0, frame priority is determined by that first. Otherwise, priority is determined by which *_PRI_SEL is set to 2'b01, then 2'b10, 2'b11, etc.

2.8.3 Priority Scheduling

The Priority scheduling support four mechanism:

•Strict priority mode: The Queue 3 has the highest priority, then Queue 2 and Queue 1, and the Queue 0 is the lowest priority.

•Mix priority mode I: The Queue 3 has the highest priority. While other Queues use the Weighted Round Robin scheme, the weight is fixed at 4:2:1.

•Mix priority mode II: The Queue 3 has the highest priority and the Queue 2 owns the second priority. While Queues 1 and 0 use the Weighted Round Robin scheme, the weight is fixed at 2:1.

•Weighted Round Robin Mode: All the four Queues use the Weighted Round Robin scheme, the weight is fixed at 8:4:2:1.

2.8.4 Rate Limiting

In triple-play applications, the switch may need to limit the rate for all frames but continue to maintain QoS policy. The AR8236 supports ingress and egress rate limiting requirements on a per-port basis by configuring the Port Rate Limit register. The AR8236 can also support per port-based egress rate limiting. Ingress rate limit can include or exclude the consideration of Management frames and registered multicast frames, while Egress rate limit can be configured to take management frames into account. The AR8236 can limit all frames and support rate limits from 32 Kbps to 1 Gbps at 32 Kbps granularity.

2.9 Mirroring

Mirroring monitors traffic for information gathering or troubleshooting higher-layer protocol operations. Users can specify that a desired mirrored-to port (sniffer port) receive a copy of all traffic passing through a designated mirrored port. The AR8236 supports mirror frames that:

- Come from an ingress specified port (ingress mirroring)
- Are destined for egress-specified port (egress mirroring)
- Mirror all ingress and egress traffic to a designated port
- Mirror frames to a specific MAC address

2.10 Broadcast/Multicast/unknown Unicast Storm Control

The AR8236 supports port based broadcast suppression which can include unregistered multicast, unregistered unicast and broadcast. If the broadcast/multicast strom control is enabled, all broadcast/multicast/unknown unicast packets beyond the default threshold of 10 ms (for 100 Mbps operations) and 100 ms (for 10 Mbps operations) are discarded.

2.11 IGMP/MLD Snooping

The AR8236 switch supports IPv4 IGMP snooping (v1/v2/v3 supported) and Ipv6 MLDv1/v2 snooping. By setting the IGMP_MLD_EN bit in the Port Control register, the AR8236 can look inside IPv4 and IPv6 packets and redirect IGMP/MLD frames to the CPU for processing. The AR8236 also supports hardware IGMP join and fast leave functions. By setting IGMP JOIN EN and IGMP LEAVE EN bits int he Port Control register, the AR8236 will update the ARL table automatically when the AR8236 receives IGMP/MLD join or leave packets, and then forward it to the router port directly in the case the CPU is not acting as a router or when enabling multicast VLAN LEAKY to bypass multicast traffic directly from WAN to LAN.

The hardware join/fast leave support the following packets:

1. IGMPv1 join

2. IGMPv2/MLDv1 join/leave

3. IGMPv3/MLDv2 report exclude NONE or include NONE.

2.12 Spanning Tree

IEEE 802.1D Spanning Tree allows bridges to automatically prevent and resolve Layer 2 forwarding loops. Switches exchange BPDUs and configuration messages and selectively enable and disable forwarding on specified ports. A tree of active forwarding links ensures an active path between any two nodes in the networks. Spanning Tree can be enabled globally or on a per-port basis by configuring the Port Status register.

2.13 MIB/Statistics Counters

The statistics counter block maintains a set of forty MIB counters per port. These counters provide a set of Ethernet statistics for frames received on ingress and transmitted on egress. A register interface allows the CPU to capture, read, or clear the counter values. All MIB counters are cleared when read.

The counters support:

- RMON MIB
- Ethernet-like MIB
- MIB II
- Bridge MIB
- RFC2819

The CPU interface supports:

- Autocast MIB counters after half-full
- Autocast MIB counters after time out
- Autocast MIB counters when requested
- Clearing all MIB counters

Table 2-21 describes the statistics counter for each port.

Table 2-4. **MIB Counters**

Counter	Width	Offset	Description
RxBroad	32bit	0x00	The number of good broadcast frames received
RxPause	32bit	0x04	The number of PAUSE frames received
RxMulti	32bit	0x08	The number of good multicast frames received
RxFcsErr	32bit	0x0c	The total number of frames received with a valid length, but an invalid FCS and an integral number of octets
RxAllignErr	32bit	0x10	The total number of frames received with a balid length that do not have an integral number of octets and an invalid FCS
RxRunt	32bit	0x14	The number of frames received that are less than 64 bytes long and have a bad FCS
RxFragement	32bit	0x18	The number of frames recdeived that are less than 64 bytes long and have a bad FCS
Rx64Byte	32bit	0x1C	The number of frames received that are exactly 64 bytes long including those with errors
Rx128Byte	32bit	0x20	The number of frames received whose length is between 65 and 127 bytes, including those with errors
Rx256Byte	32bit	0x24	The number of The number of frames received whose length is between 128and 255 bytes, including those with errors
Rx512Byte	32bit	0x28	The number of frames received whose length is between 256 and 511 bytes, including those with errors
Rx1024Byte	32bit	0x2C	The number of frames received whose length is between 512 and 1023 bytes, including those with errors
Rx1518Byte	32bit	0x30	The number of frames received whose length is between 1024 and 1518 bytes, including those with errors
RxMaxByte	32bit	0x34	The number of frames received whose length is between 1519 and maxlength, including those with errors (Jumbo)
RxTooLong	32bit	0x38	The number of frames received whose length exceeds maxlength including those with FCS errors

RxGoodByte	64bit	0x3C:0x40	Total data octets received in a frame with a valid FCS. All frame sizes are included.
RxBadByte	64bit	0x44:0x48	Total data octets received in frame with an invalid FCS. All frame sizes are included. Pause frame is included with a valid FCS.
RxOverFlow	32bit	0x4C	Total valid frames received that are discarded due to lack of buffer space
Filtered	32bit	0x50	Port disabled and unknown VID
TxBroad	32bit	0x54	Total good frames tranmitted with a broadcast Destination address
TxPause	32bit	0x58	Total good PAUSE frames transmitted
TxMulti	32bit	0x5C	Total good frames transmitted with a multicast Destination address
TxUnderRun	32bit	0x60	Total valid frames discarded that were not transmitted due to transmit FIFO buffer underflow
Tx64Byte	32bit	0x64	Total frames tranmitted with a length of exactly 64 bytes, including errors
Tx128Byte	32bit	0x68	Total frames tranmitted with a length between 65 and 127 bytes, including those with errors
Tx256Byte	32bit	0x6C	Total frames tranmitted with a length between 128 and 255 bytes, including those with errors
Tx512Byte	32bit	0x70	Total frames tranmitted with a length between 256 and 511 bytes, including those with errors
Tx1024Byte	32bit	0x74	Total frames tranmitted with a length between 512 and 1023 bytes, including those with errors
Tx1518Byte	32bit	0x78	Total frames transmitted with length between 1024 and 1518, including those with errors (Jumbo)
TxMaxByte	32bit	0x7C	Total frames transmitted with length between 1519 and Maxlength, including those with errors (Jumbo)
TxOverSize	32bit	0x80	Total frames over Maxlength but transmitted truncated with bad FCS
TxByte	64bit	0x84:0x88	Total data octets transmitted from counted, including those with a bad FCS
TxCollision	32bit	0x8C	Total collisions experienced by a port during packet transmission
TxAbortCol	32bit	0x90	Total number of frames not transmitted becase the frame experienced 16 transmission attempts and was discarded
TxMultiCol	32bit	0x94	Total nuber of successfully transmitted fromes that experienced more than one collision
TxSingalCol	32bit	0x98	Total number of successfully transmitted frames that experienced exactly one collision
TxExcDefer	32bit	0x9C	The number of frames that defered for an excessive period of time
TxDefer	32bit	0xA0	Total frames whose transmission was delayed on its first attempt because the medium way was busy
TXLateCol	32bit	0xA4	Total number of times a collision is detedted later than 512 bit-times into the transmission of a frame

2.14 Atheros Header Configuration

Table 2-5 Table 2-22 describes the Atheros header configuration. The Atheros header is a two-byte header that the CPU uses to configure the AR8236 switch. The Atheros header will be located after the SA of the packet.

Table 2-5. **Atheros Header Configuration**

<table>
<tr><th>Bit</th><th>Name</th><th colspan="8">Description</th></tr>
<tr><td>15:14</td><td>Version</td><td colspan="8">2’b10</td></tr>
<tr><td>13:12</td><td>PRIORITY</td><td colspan="8">Packet priority</td></tr>
<tr><td rowspan="14">11:8</td><td rowspan="14">TYPE</td><td colspan="8">Packet Type:</td></tr>
<tr><td>0</td><td>Normal Packet</td><td colspan="6">Normal packet from Ethernet include management. Destination port determined by ARL and the VLAN table</td></tr>
<tr><td>1</td><td>RES</td><td colspan="6">Reserved</td></tr>
<tr><td>2</td><td>MIB</td><td colspan="6">Auto-cast MIB frame</td></tr>
<tr><td>4:3</td><td>RES</td><td colspan="6">Reserved</td></tr>
<tr><td rowspan="3">5</td><td rowspan="3">READ_WRITE_REG</td><td colspan="6">Read or write register frame:</td></tr>
<tr><td>8-byte</td><td>4-byte</td><td>2-byte</td><td>0—12-byte</td><td>34—46-byte</td><td>4-byte</td></tr>
<tr><td>Command (low byte first)</td><td>data (low byte first)</td><td>header (high byte first)</td><td>data (low byte first)</td><td>Padding</td><td>CRC</td></tr>
<tr><td>6</td><td>READ_WRITE_REG_ACK</td><td colspan="6">Read or write register ACK frame from the CPU</td></tr>
<tr><td>7</td><td>IGMP</td><td colspan="6">Send IGMP frames to the CPU</td></tr>
<tr><td>8</td><td>MLD</td><td colspan="6">Send MLD frames to the CPU</td></tr>
<tr><td>9</td><td>802.1X</td><td colspan="6">Send 802.1x frames to the CPU.</td></tr>
<tr><td>10</td><td>ARP</td><td colspan="6">Send ARP frames to the CPU</td></tr>
<tr><td>11:15</td><td>RES</td><td colspan="6">Reserved</td></tr>
<tr><td>7</td><td>FROM_CPU</td><td colspan="8">This bit indicates the forwarding method:
1: Forwarding is based upon the PORT_NUM (bit6:0)
0: Forwarding is based upon the VLAN table result and PORT_NUM (bit 6:0)</td></tr>
<tr><td>6:0</td><td>PORT_NUM</td><td colspan="8">If the CPU is sending frames to the AR8236, and these bits indicate the “port map” on egress. Frames will be forwarded based upon bit[6:0] indicating the egress port from the port map.
If the CPU is receiving frames from the AR8236, and these bits indicate the “source port” on ingress.. See the description of bit[7] for more information.</td></tr>
</table>

Read or Write Register Frame

Value	Name	Description	
63:33	SEQ_NUM	Sequence number for CPU_DETECT	
31:29	CHECK_CODE	3'b101	
28	CMD	0	Write
		1	Read
27:24	CHECK_CODE	4b'0000	
23:20	LENGTH	Read/write length	
		4	Register length
		6	VLAN table length
		10	ARL table length
19	CHECK_CODE	1'b0	
18:0	ADDR	register offset address, must be DWORD aligned	

2.15 IEEE 802.3 Reserved Group Addresses Filtering Control

The AR8236 supports the ability to drop/ redirect/copy 802.1D specified reserved group MAC addresses: 01-80-C2-00-00-04 to 01-80-C2-00-00-0F by adding the address to ARL table.

2.16 Forwarding Unknown

The AR8236 can be configured to prevent the forwarding of unicast frames and multicast frames with unregistered destination MAC address on per port base. This can be done by setting UNI_FLOOD_DP and MULTI_FLOOD_DP where a bit represents a port of the AR8236.

2.17 Memory Map

The Memory Map is shown below:

Table 2-6. **Memory Map**

Global Register	Offset
Global Register	0x0000 ~ 0x000FC
Port Register	0x00100 ~ 0x0012C
MIB Register	0x020*00 ~ 0x02*A4

3. Register Descriptions

Table 3-1 shows the reset types used in this document.

Table 3-1. **Register Reset Types**

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to a register field takes effect without a software reset.
RES	Reserved for future use. All reserved bits are read as zero, unless otherwise noted.
RO	Read Only.
ROC	Read Only Clear. After a read, the register field is cleared to zero.
R/W	Read/Write.
RWC	Read/Write Clear on read. All bits are readable and writable. After a reset, or after the register is read, the register field is reset to zero.
RWR	Read/Write Reset. All bits are readable and writable. After a reset, or after the register is read, the register field is cleared to zero.
RWS	Read/Write Set. All bits are readable and writable. After a reset, the register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete.
Update	The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.
WO	Write Only. Reads to this type of register field returen undefined data.

3.1 *Global Control Registers 0x0000 —0x00FC*

Table 3-2 summarizes the global control registers.

Table 3-2. **Global Control Register Summary**

Offset	Description	Page
0x0000	Mask Control Register	page 31
0x0004	PORT0 PAD MODE CTRL	
0x0008	PORT5 PAD MODE CTRL	
0x00010	Power-on Strapping Register	
0x0010	Global Interrupt Register	page 35
0x0014	Global Interrupt Mask Register	page 36
0x0020 — 0x0024	Global MAC Address Register	page 37
0x0028	Loop Check Result Register	page 31
0x002C	Flood Mask Register	page 40

Table 3-2. **Global Control Register Summary (continued)**

Offset	Description	Page
0x0030	Global Control Register	page 40
0x0034	Flow Control Register 0	page 42
0x0038	Flow Control Register 1	page 42
0x003C	QM Control Register	page 43
0x0040 — 0x0044	VLAN Table Function Register	page 45
0x0050 — 0x0058	Address Table Function Register	page 50
0x005C	Address Table Control Register	page 50
0x0060 — 0x006C	IP Priority Mapping Register 2	page 51
0x0070	Tag Priority Register	page 54
0x0074	Service Tag Register	page 54
0x0078	CPU Port Register	page 55
0x0080	MIB Function Register	page 55
0x0098	MDIO Control Register	page 56
0x00B0 — 0x00B4	LED Control Register	page 57

3.2 Port Control Registers 0x0100 — 0x0124

Table 3-3 summarizes the Port Control Registers.

Table 3-3. **Port Control Registers — Summary**

Port	Offset	Name	Page
Port 0	***0x0100 - 0x01FC***	***Total Port 0 control register memory allocation***	
	0x0100	Port status register	page 60
	0x0104	Port control register	page 68
	0x0108	Port based VLAN register	page 64
	0x0110	Priority control register	page 68
	0x0114	Storm control register	page 68
	0x0118	Queue control register	page 69
	0x010C, 0x011C, 0x0120	Rate limit registers	page 71
Port 1	***0x0200 - 0x01FC***	***Total Port 1 control register memory allocation***	
	0x0200	Port status register	page 60
	0x0204	Port control register	page 68
	0x0208	Port based VLAN register	page 64
	0x0210	Priority control register	page 68
	0x0214	Storm control register	page 68
	0x0218	Queue control register	page 69
	0x020C, 0x021C, 0x0220	Rate limit registers	page 71
Port 2	***0x0300 - 0x03FC***	***Total Port 2 control register memory allocation***	
	0x0300	Port status register	page 60
	0x0304	Port control register	page 68
	0x0308	Port based VLAN register	page 64
	0x0310	Priority control register	page 68
	0x0314	Storm control register	page 68
	0x0318	Queue control register	page 69
	0x030C, 0x031C, 0x0320	Rate limit registers	page 71

Port	Offset	Name	Page
Port 3	***0x0400 - 0x04FC***	***Total Port 3 control register memory allocation***	
	0x0400	Port status register	page 60
	0x0404	Port control register	page 68
	0x0408	Port based VLAN register	page 64
	0x0410	Priority control register	page 68
	0x0414	Storm control register	page 68
	0x0418	Queue control register	page 69
	0x040C, 0x041C, 0x0420	Rate limit registers	page 71
Port 4	***0x0500 - 0x05FC***	***Total Port 4 control register memory allocation***	
	0x0500	Port status register	page 60
	0x0504	Port control register	page 68
	0x0508	Port based VLAN register	page 64
	0x0510	Priority control register	page 68
	0x0514	Storm control register	page 68
	0x0518	Queue control register	page 69
	0x050C, 0x051C, 0x0520	Rate limit registers	page 71
Port 5	***0x0600 - 0x06FC***	***Total Port 5 control register memory allocation***	
	0x0600	Port status register	page 60
	0x0604	Port control register	page 68
	0x0608	Port based VLAN register	page 64
	0x0610	Priority control register	page 68
	0x0614	Storm control register	page 68
	0x0618	Queue control register	page 69
	0x0600C, 0x061C, 0x0620	Rate limit registers	page 71

3.3 Mask Control Register

Address Offset: 0x0000

Table 3-4 summarizes the Mask Control Registers

Table 3-4. **Mask Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	W/SC	0	SOFT_RET	1'b1: software reset. This bit is set by the sofware to initate the hardware. It should be slef-cleared by the hardware after the initialization is done.
30:26	R/O	0	Reserved	
25:20	R/W	0	Reserved	
19:17	R/O	0	Reserved	
16	R/W	0	LOAD_EEPROM	load EEPROM enable. This bit is set to automatically load registers from an EEPROM. It should be cleared after the loading is complete.
15:8	RO	0x03	DEVICE_ID	Device identifier
7:0	RO	0x01	REV_ID	Revision identifier

NOTE: this register can only be reset by a hardware reset.

3.4 PORT0 PAD MODE CTRL Register

Address Offset: 0x0004

Table 3-4 summarizes the PORT0 PAD MODE CTRL Registers

Table 3-5. **PORT0 PAD MODE CTRL Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:20	R/O	0	Reserved	
19	R/W	0	MAC0_RMII_TXCLK_SEL	1'b1 select invert clock for RMII tx pipe
18	R/W	0	MAC0_RMII_RXCLK_SEL	1'b1 select invert clock for RMII rx pipe
17	R/W	0	MAC0_RMII_EN	1'b1 mac0 connected to cpu through RMII interface
16:12	R/O	0	Reserved	
11	R/W	0	Mac0_phy_mii_pipe_rxclk_sel	1'b1 select clock edge for rxpipe,default is invert
10	R/W	0	MAC0_PHY_MII_EN	1'b1 mac0 connected to cpu through MII interface, phy mode
9	R/W	0	MAC0_PHY_MII_TXCLK_SEL	1'b1 select invert clock output for port0 phymode ,MII interface txclk
8	R/W	0	MAC0_PHY_MII_RXCLK_SEL	1'b1 select invert clock output for port0 phymode ,MII interface rxclk
7	R/W	0	MAC0_200M_EN	1'b1 : mac0 work at speed 200M
6:3	R/O	0	Reserved	
2	R/W	0	MAC0_MAC_MII_EN	1'b1 mac0 connected to cpu through MII interface, mac mode
1	R/W	0	MAC0_MAC_MII_TXCLK_SEL	1'b1 select invert clock input for port0 macmode, MII interface txclk
0	R/W	0	MAC0_MAC_MII_RXCLK_SEL	1'b1 select invert clock input for port0 macmode, MII interface rxclk

NOTE: this register can only be reset by a hardware reset.

3.5 PORT5 PAD MODE CTRL Register

Address Offset: 0x0008

Table 3-4 summarizes the PORT5 PAD MODE CTRL Register

Table 3-6. **PORT5 PAD MODE CTRL Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	0	Reserved	
29	R/W	0	PHY4_RMII_EN	1'b1 phy4 connected to cpu through RMII interface
28	R/W	0	PHY4_MII_EN	1'b1 phy4 connected to cpu through MII interface
27:20	R/W	0	Reserved	
19	R/W	0	MAC5_RMII_TXCLK_SEL	1'b1 select invert clock for RMII tx pipe
18	R/W	0	MAC5_RMII_RXCLK_SEL	1'b1 select invert clock for RMII rx pipe
17	R/W	0	MAC5_RMII_EN	1'b1 Mac5 connected to cpu through RMII interface
16:12	R/W	0	Reserved	
11	R/W	0	Mac5_phy_mii_pipe_rxclk_sel	1'b1 select clock edge for rxpipe,default is invert
10	R/W	0	MAC5_PHY_MII_EN	1'b1 Mac5 connected to cpu through MII interface, phy mode
9	R/W	0	MAC5_PHY_MII_TXCLK_SEL	1'b1 select invert clock output for port5 phymode ,MII interface txclk
8	R/W	0	MAC5_PHY_MII_RXCLK_SEL	1'b1 select invert clock output for port5 phymode ,MII interface rxclk
7	R/W	0	MAC5_200M_EN	1'b1 : mac5 work at speed 200M
6:3	R/W	0	Reserved	
2	R/W	0	Reserved	
1	R/W	0	Reserved	
0	R/W	0	Reserved	

3.6 Power-on Strapping Register

Address Offset: 0x0010

Table 3-4 summarizes the Power-on Strapping Register

Table 3-7. **Power-on Strapping Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	POWER_ON_SEL	1'b1: use register config value to replace power on strip for bit 25:24
30:28	R/W	0	Reserved	
27	R/W	0	SPI_SIZE	
26	R/W	0	Reserved	
25	R/W	0	SPI_EN	1'b1: EEPROM is connected to the AR8236
24	R/W	1	LED_OPEN_EN	1'b1 LED PAD is open drain mode
23:21	R/W	0	Reserved	
20	R/W	0	Reserved	
19	R/W	0	Reserved	
18	R/W	1	Reserved	
17	R/W	1	Reserved	
16	R/W	0	Reserved	
15:14	R/W	0	Reserved	
13	R/W	0	Reserved	
12	R/W	1	Reserved	
11	R/W	1	Reserved	
10	R/W	0	Reserved	
9	R/W	1	Reserved	
8	R/W	1	Reserved	
7:6	R/W	0	Reserved	
5	R/W	1	Reserved	
4:2	R/W	0	Reserved	
1	R/W	0	PAD_CTRL[1]	
0	R/W	0	PAD_CTRL[0]	

NOTE: this register can only be reset by a hardware reset.

3.7 Global Interrupt Register

Address Offset: 0x0014

Table 3-8 Summarizes the Global Interrupt register

Table 3-8. **Global Interrupt Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	Reserved	
23:19	R/O	0	Reserved	
18	RW1C	0	LOOP_CHECK_INT	Interrupt when loop checked by hardware
17	R/W1C	0	Reserved	
16	R/W1C	0	Reserved	
15	R/O	0	Reserved	
14	R/W1C	1	HARDWARE_INI_DONE	Interrupt when hardware memory initialization is complete
13	R/W1C	1	MIB_INI_INT	Interrupt when MIB memory intialization is complete
12	R/W1C	0	MIB_DONE_INT	Interrupt when MIB access by CPU is complete
11	R/W1C	0	BIST_DONE_INT	Interrupt when BIST test is complete
10	R/W1C	0	VT_MISS_VIO_INT	Interrupt when the VID is not found in the VLAN table
9	R/W1C	0	VT_MEM_VIO_INT	Interrupt when the VID is in the VLAN table, but the source port is not a member of the VLAN
8	R/W1C	0	VT_DONE_INT	Interrupt when the CPU has completed an access of the VLAN table
7	R/W1C	1	QM_INI_INT	Interrupt when the QM memory intialization is complete
6	R/W1C	1	AT_INI_INT	Interrupt when the Address table initialization is complete
5	R/W1C	0	ARL_FULL_INT	Interrupt when a new address is "learned" by being added to the address table, but the two addresses are both valid
4	R/W1C	0	ARL_DONE_INT	Interrupt when the CPU access of the Address table is complete
3	R/W1C	0	MDIO_DONE_INT	Interrupt when MDIO access of the switch register is complete
2	R/W1C	0	PHY_INT	Physical layer interrupt
1	R/W1C	0	EEPROM_ERR_INT	Interrupt when an error is detected during the loading of an EEPROM
0	R/W1C	0	EEPROM_INT	Interrupt when the loading of an EEPROM is complete

3.8 Global Interrupt Mask Register

Address Offset: 0x0018

Each bit in this register is corresponding to GLOBAL INTERRUPT REGISTER. Interrupt is allowed to be sent out when both interrupt evernt and mask bit are set.

Table 3-9 Summarizes the Global Interrupt Mask register

Table 3-9. **Global Interrupt Mask Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:18	R/W	0	Reserved	
18	R/W	0	LOOP_CHECK_INT_EN	Enable loop check interrupt
17	R/W	0	Reserved	
16	R/W	0	Reserved	
15	R/O	0	Reserved	
14	R/W	0	HARDWARE_INI_DONE_EN	Enable interrupt when hardware memory initiation is complete
13	R/W	0	MIB_INI_INT_EN	MIB was accessed by the CPU
12	R/W	0	MIB_DONE_INT_EN	Enable the interrupt of MIB accesse done by CPU
11	R/W	0	BIST_DONE_INT_EN	Enable BIST test complete interrupt
10	R/W	0	VT_MISS_VIO_INT_EN	Interrupt when the VID of the received frame is not in the VLAN table
9	R/W	0	VT_MEM_VIO_INT_EN	Interrupt when the VID of the received frame is in the VLAN table, but the source port is not the member of the VID
8	R/W	0	VT_DONE_INT_EN	The VLAN table was accessed by the CPU
7	R/W	0	QM_INI_INT_EN	Enable interrupt when qm memory initiation is complete
6	R/W	0	AT_INI_INT_EN	Enable interrupt when address table initiation is complete
5	R/W	0	ARL_FULL_INT_EN	Interrupt when a new address to learn is in the address table, but the address's two entries are both valid
4	R/W	0	ARL_DONE_INT_EN	The address table was accessed by the CPU
3	R/W	0	MDIO_DONE_INT_EN	The MDIO access switch register was interrupted
2	R/W	0	PHY_INT_EN	Physical layer interrupt
1	R/W	0	EEPROM_ERR_INT_EN	Interrupt when an error occurred during load EEPROM
0	R/W	0	EEPROM_INT_EN	Interrupt when an EEPROM load has completed

3.8.5 Global MAC Address Register

Address Offset: 0x0020, 0x0024

Note: these registers can only be reset by hardware.

Table 3-10 Summarizes the Global MAC Address register

Table 3-10. **Global MAC Address Register**

Offset	Bit	R/W	Inital Value	Mnemonic	Description
0x0020	31:16	R/O	0	Reserved	
	15:8	R/W	0	MAC_ADDR_BYTE4	Station address of switch. Used as source address in pause frame or other management frames
	7:0	R/W	0x01	MAC_ADDR_BYTE5	
0x0024	31:24	R/W	0	MAC_ADDR_BYTE0	Station address of the switch, used as source address in pause frame or other management frames
	23:16	R/W	0	MAC_ADDR_BYTE1	
	15:8	R/W	0	MAC_ADDR_BYTE2	
	7:0	R/W	0	MAC_ADDR_BYTE3	

3.8.6 Loop Check Result

Address Offset: 0x0028

Note: these registers can only be reset by hardware.

Table 3-10 Summarizes the Loop Check Result register

Table 3-11. **loop Check Result Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:8	R/O	0	Reserved	
7:4	R/O	0	PORT_NUM_NEW	When hardware checked loop occur, these bits indicate MAC address new port num.
4:0	R/O	0	PORT_NUM_OLD	When hardware checked loop occur, these bits indicate MAC address old port num.

3.9 Flood Mask Register

Address Offset: 0x002C

Table 3-12 Summarizes the Flood Mask Register

Table 3-12. **Flood Mask Register**

Bit	R/W	Inital Value	Mnemonic	Description
30:25	R/W	0x3E	BROAD_DP	If mac received broadcast frame, use these bits to determine the destination port
24	R/W	0	ARL_UNI_LEAKY_EN	1’b1: USE LEAKY_EN bit in ARL table to control unicast fram leaky VLAN and ignore “UNI_LEAKY_EN” 1’b0: ignore LEAKY_EN bit in ARL table to control unicast frame leaky VLAN. Only use port-pased UNI_LEAKY_EN to control unicast frame leaky VLAN

Bit	R/W	Inital Value	Mnemonic	Description
23	R/W	0	ARL_MULTI_LEAKY_EN	1'b1: use LEAKY_EN bit in ARL table to control multicast frame leaky VLAN, and ignore "MULTI_LEAKY_EN". 1'b0: ignore LEAKY_EN bit in ARL table to control multicast frame leaky VLAN. Only use port base MULTI_LEAKY_EN to control multicast frame leaky VLAN.
21:16	R/W	0x3E	MULTI_FLOOD_DP	If MAC received unknown milticast frame which DA is not contained in the ARL table, use these bits to determine the destination port.
15:14	R/O	0	Reserved	
13:8	R/W	6′b0	IGMP_JOIN_LEAVE_DP	If MAC received IGMP/MLD fast join or leave frame, use these bits to determine the destination port
7:6	R/O	0	Reserved	
5:0	R/W	0x7E	UNI_FLOOD_DP	If MAC received unkonown unicast fram in which the DA is not contained in the ARL table, use these bits to determine the destination port

3.10 Global Control Register

Address Offset: 0x0030

Table 3-13 Summarizes the Global Control Register

Table 3-13. **Global Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	0	Reserved	
29	R/W	0	RATE_DROP_EN	drop packet enable due to rate limit. 1'b1: switch will drop frames due to rate limit. 1'b0: switch would use flow control to the source port due to rate limit, if the port won't stop switch will drop frame from that port.
28	R/W	1	Reserved	
27:26	R/W	0x2	Reserved	
25:24	R/W	0x1	ING_RATE_TIME_SLOT	Ingress rate limit control timer slot. 2'b00: 100us; 2'b01: 1ms 2'b10: 10ms 2'b11: 100ms Notes: if port rate limit set to less than 96kbps, don't select 100us as time slot.
23:20	R/W	0xF	RELOAD_TIMER	Reload EEPROM timer If the EEPROM can't be read from, the EEPROM should be reloaded when the timer is completed. The timer is set by multiplying the number here by 8ms. If these bits are zero, the EEPROM will not be reloaded
19	R/O	0	Reserved	
18	R/W	0	BROAD_DROP_EN	Broadcast storm control drop packet enable. 1'b1: switch will drop frames if broadcast storm occur. 1'b0: when broadcast storm occur, switch will use flow control to the source port first, if the port won't stop switch will drop frame.

Bit	R/W	Inital Value	Mnemonic	Description
17:14	R/O	0	Reserved	
13:0	R/W	'h5EE	MAX_FRAME_SIZE	Max frame sized can be received and tranmitted by MAC. If a packet's size is larger than MX_FRAME_SIZE, it will be dropped by the MAC. The value is for a normal packet. It should add 4 by MAC if VLANs are supported, add 8 for double VLANs, and add 2 for Atheros header. For Jumbo frames, the maximum frame size is 9 Kbytes.

3.11 Flow Control Register 0

Address Offset: 0x0034

Table 3-14 Summarizes the Flow Control Register 0

Table 3-14. **Flow Control Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	Reserved	
30:24	R/O	0	Reserved	
23:16	R/W	0x50	GOL_XON_THRES	Global-based transmit on threshold. When block memory used by all the ports is less that the value entered here, the MAC would send out a pause off frame and the link partner will start to transmit frames
15:8	R/O	0	Reserved	
7:0	R/W	0x80	GOL_XOFF_THRES	Global-based transmit off threshold. When block memory used by all the ports is more than the value entered here, the MAC will send out a pause on frame, and the link partner will stop transmitting frames

3.12 Flow Control Register 1

Address Offset: 0x0038

Table 3-15 Summarizes the Flow Control Register 1

Table 3-15. **Flow Control Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	0	Reserved	
23:16	R/W	0x16	PORT_XON_THRES	Port-based transmit on threshold. When bolck memory used by one port is less than this value, the MAC will send out a pause off frame and the link partner will begin to transmit frames
15:8	R/O	0	Reserved	
7:0	R/W	0x20	PORT_XOFF_THRES	Port-based transmit off threshold. When block memory used by one port is more than this value, the MAC will send out a pause on frame and the link partner will stop transmitting frames

3.12.7 QM Control Register

Address Offset: 0x003C

Table 3-16 Summarizes the QM Register

Table 3-16. **QM Register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	1'b1	Reserved	
30	R/W	1'b1	Reserved	
29:28	R/O	0	Reserved	
27:24	R/W	4'hF	IGMP_JOIN_STATUS	Use for igmp packet learn in arl table, define the status 4'h0: Inticates entry is empty 4'h1 ~ 7: indicatesentry is dynamic and valid 4'h8 ~ 4'hE: Reverved for future use 4'F: Indicates entry is static and won't be aged out or changed by the hardware
23	R/W	1'b0	IGMP_JOIN_LEAKY_EN	IGMP join address leaky vlan enable. 1'b1: igmp join address should be set the leaky_en bit in ARL table 1'b0: igmp join address should be clear the leaky_en bit in ARL table
22	R/W	0	IGMP_JOIN_NEW_EN	1'b1: enable hardware add new address to ARL table when received IGMP/ MLD join frame and remove address from ARL when received IGMP/MLD leave frame.
21	R/W	0	Reserved	
20	R/W	1'b0	PPPOE_REDIRECT_EN	Enable sending PPPoE discovery frames to the CPU. If this bit is set to 1, PPPoE discovery frames are sent to the CPU port. If this bit is set to 0, PPPoE discovery frames are transmitted as normal frames
19	R/W	1'b0	IGMP_V3_EN	1'b1: hardware acknowledge IGMP v3 frame and MLD v2 frame, and multicast address can be hardware join or leave
18	R/W	1'b0	IGMP_JOIN_PRI_REMAP_EN	Use for igmp packet learn in arl table, define DA priority remap enable

Bit	R/W	Inital Value	Mnemonic	Description
17:16	R/W	2’b00	IGMP_JOIN_PRI	Use for igmp packet learn in arl table, define DA priority when IGMP_JOIN_PRI_REMAP_EN is enable.
15	R/W	1’b0	ARP_EN	ARP frame acknowledge enable
14	R/W	1’b0	ARP_REDIRECT_EN	1'b1: ARP frame redirect to cpu port 1'b0: ARP frame copy to cpu
13	R/W	1’b0	RIP_COPY_EN	1'b1 : rip v1 frame copy to cpu 1'b0: don't copy rip v1 frame to cpu
12	R/W	1’b0	EAPOL_REDIRECT_EN	1'b1:802.1x frame redirect to cpu 1'b0: 802.1x frame copy to cpu
11	R/W	0	IGMP_COPY_EN	1’b1: QM will copy IGMP/MLD frames to the CPU port 1’b0: QM will redirect IGMP/MLD frames to the CPU port
10	R/W	0	PPPOE_EN	1’b1: hardware acknowledge PPPoE frame enable
9	R/O	0	Reserved	
8	R/W	0	Reserved	
7	R/W	0	FLOW_DROP_EN	1'b1: packet could be drop due to flow control except the highest priority packet. 1'b0: switch won't drop packets due to flow control
6	R/W	1	MANAGE_VID_VIO_DROP_EN	1'b1: management frame should be drop if vlan violation occur 1'b0: management frame transmit out if vlan violation occur.
5:0	R/W	‘hE	FLOW_DROP_CNT	Max free queue could be use after the port has been flow control. Then packets should be drop except the highest priority. Default value 'hE is set to normal packets which length is no more than 1518 bytes. For jumbo frame, 'd33 is commanded.

3.13 VLAN Table Function Register 0

Address Offset: 0x0040

Table 3-17 Summarizes the VLAN Table Function Register 0

Table 3-17. **VLAN Table Function Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	VT_PRI_EN	when VT_PRI_EN is set, then VT_PRI will replace VLAN priority in the frame as its QoS classification
30:28	R/W	0	VT_PRI	when VT_PRI_EN is set, the VT_PRI will replace VLAN priority in the frame as its QoS classification
27:16	R/W	0	VID	VLAN ID to be added or purged
15:12	R/O	0	Reserved	
11:8	R/W	0	VT_PORT_NUM	Port number to be removed
7:5	R/O	0	Reserved	
4	R/W1C	0	VT_FULL_VIO	VLAN table full violation. This bit is set to 1'b1 if the VLAN table is full when cpu wants to add a new VID to the VLAN table.
3	R/W	0	VT_BUSY	VLAN table is busy. This bit must be set to 1 to start a VT operation and cleared to 0 after the operation is done. If this bit is set to 1, the CPU can not request another operation
2:0	R/W	0	VT_FUNC	VLAN table operation control 3'b000: no operation 3'b001: flush all entries 3'b010: load an entry. If these bits are set, the CPU will load an entry form the VLAN table 3'b011: purge an entry. If these bits are set, the CPU will purge an entry form the VLAN table 3'b100: remove a port form the VLAN table. The port umber which will be removed is indicted in VT_PORT_NUM 3'b101: get next VID if VID is 12'b0 and VT_BUSY is set by software, hardware will search for the first valid entry in the VLAN table If VID is 12'b0 and VT_Busy is reset by hardware, then there is no valid entry from VID set by the software 3'b110: read one entry

3.14 VLAN Table Function Register 1

Address Offset: 0x0044

Table 3-18 Summarizes the VLAN Function Register 1

Table 3-18. **VLAN Function Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:12	R/O		Reserved	
11	R/W		VT_VALID	1: indicated entry is valid 0: indicates the entry is empty
10:7	R/O		Reserved	
6:0	R/W	0	VID_MEM	VID member in the VLAN table. These bits are used to indicate which ports are members of the VLAN. Bit 0 is assigned to port0, 1 to port1, 2, to port2, and so on.

3.15 Address Table Function Register 0

Address Offset: 0x0050

Table 3-19 Summarizes the Address Table Function Register 0

Table 3-19. **Address Table Function Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	0	AT_ADDR_BYTE4	Byte 4 of the address
23:16	R/W	0	AT_ADDR_BYTE5	the last byte of the address
15:13	R/O	0	Reserved	
12	R/W 1C	0	AT_FULL_VIO	ARL table-full violation. This bit is set to 1 if the ARL table is full when the CPU wants to add a new entry to the ARL table. can also be set to 1 if the ARL table is empty when the CPU wants to purge and entry to the ARL table
11:8	R/W	0	AT_PORT_NUM	Port number to be flushed. If "AT_FUNC" is set to 3'b101, lookup module must flush all the unicast entries for the port (or flush the port from the ARL table)
7:5	R/O	0	Reserved	

Bit	R/W	Inital Value	Mnemonic	Description
4	R/W	0	FLUSH_STATIC_EN	1'b1: when AT_FUNC is set to 3'b101, all static entries in the ARL table can be flushed. 1'b0: when AT_Func is set to 3'b101, only dynamic entries in the ARL table will be flushed
3	R/W	0	AT_BUSY	Address table busy. This bit must be set to 1 to start an AT operation and cleared to 0 when the operation is complete. If this bit is set to 1, the CPU can not request another operation
2:0	R/W	0	AT_FUNC	Address table function 3'b000: no operation 3'b001: flush all entries 3'b010: load an entry. If these bits are set to 3'b010, the CPU will load an entry into the ARL table 3'b011: purge an entry. If these bits are set, the CPU will purge an entry fromthe ARL table. 3'b100: flush all unlocked entries in the ARL 3'b101: flush one port from the ARL table 3'b110: get the next valid or static entr in the ARL table If the address and AT_STATUS are all zero, the hardware will search for the first valid entry from entry0 If the address and AT_STATUS is not zero, the hardware will search for the next valid entry whose address is 48'h0. If hardware returns with the address and AT_STATUS all zero, there is no next valid entry in the ARL table. 3'b111: search MAC address

3.16 Address Table Function Register 1

Address Offset: 0x0054

Table 3-20 Summarizes the Address Table Function Register 1

Table 3-20. **Address Table Function Register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	0	AT_ADDR_BYTE0	The first byte of the address to operate. This byte is the highest byte of the MAC address fo the MSB.
23:16	R/W	0	AT_ADDR_BYTE1	The second byte of the address
15:18	R/W	0	AT_ADDR_BYTE2	The third byte of the address
7:0	R/W	0	AT_ADDR_BYTE3	The forth byte of the address

3.17 Address Table Function Register 2

Address Offset: 0x0058

Table 3-21 Summarizes the Address Table Function Register 2

Table 3-21. **Address Table Function Register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31:27	R/O	0	Reserved	
26	R/W	0	COPY_TO_CPU	1'b1: packet received with this address will be copied to the CPU port
25	R/W	0	REDIRECT_TO_CPU	1'b1: packet reveived with this address will be redirected to the CPU port. If no CPU is connected to the switch, this packet will be discarded
24	R/W	0	LEAKY_EN	1'b1: enables leaky VLANs for this MAC address This bit can be used for unicast and multicast frames, control by ARL_UNI_LEAKY_EN and ARL_MULTI_LEAKY_EN
23:20	R/O	0	Reserved	

Bit	R/W	Inital Value	Mnemonic	Description
19:16	R/W	0	AT_STATUS	Destination address status, associated to “status” bits in the Address Table 4’h0: indicates entry is empty 4’h1 ~ 7: indicates the entry is dynamic and valid 4’h8 ~ 4’hE: reserved for future use 4’hF: indicates entry is static ane won’t be aged out or changed by the hardware.
15	R/W	0	MAC_CLONE	MAC clone address. 1’b1: this address is set to MAC clone. CPU can not age-out. Other ports learn and age as normal. If DA and VID result is CPU port, send the packet to normal ports only.
14	R/W	0	SA_DROP_EN	SA drop enable Drop packe enable when source address in in this entry. If this bit is set to 1’b1, the packet with an SA of this entry will be dropped
13	R/W	0	MIRROR_EN	Port mirror enable 1: indicates packets will be sent to the mirror port and the destination port. 0: indicates packet will be sent only to the destination port
12	R/W	0	AT_PRIORITY_EN	DA priority enable 1: indicates AT_PRIORITY can override any other priority determined by the frame’s data
11:10	R/W	0	AT_PRIORITY	DA priority These priority bits can be used as a frame’s priority when AT_PRIORITY_EN is set to one.
9	R/W	0	HASH_HIGH_ADDR	Mac hash addr max bit use for cpu_func (get next valid)
8	R/W	0	CROSS_PORT_STATE_EN	1'b1, cross port_state enable.
7:6	R/W	0	Reserved	
5:0	R/W	0	DES_PORT	Destination port bits for address. These bits indicate which ports are associated with the MAC address when they are set to one. Bit 0 is assigned to port 0, 1 to port1, 2 to port2, and so on.

3.18 Address Table Control Register

Address Offset: 0x005C

Table 3-22 Summarizes the Address Table Register

Table 3-22. **Address Table Control Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:27	R/O	0	Reserved	
26:24	R/W	0	LOOP_CHECK_TIMER	3'h0: disable loop back check 3'h1: 1ms 3'h2: 10ms 3'h3: 100ms 3'h4: 500ms 3'h5~7: reserved
23	R/O	0	Reserved	
22	R/W	0	VID_4095_DROP_EN	1'b1: if frame with vid='d4095, will be dropped by switch.
21	R/W	0	SWITCH_STAG_MODE	Select switch work vlan mode. 1'b1: S-TAG mode 1'b0: C-TAG mode
20	R/W	0	Reserved	
19	R/W	1	Reserved	
18	R/W	0	LEARN_CHANGE_EN	1'b1: enable new mac address change old one if hash violation occur when learning 1'b0: if hash violation occur when learning, no new address be learned to arl.
17	R/W	1	AGE_EN	Enable age operation. 1'b1: lookup module can age the address in the address table.
16	R/O	0	Reserved	
15:0	R/W	'h2B	AGE_TIME	Address Table Age Timer. These bits determine the time that each entry remains valid in the address table, since last accessed. For the time is times 7s, maximum age time is about 10,000 minutes. The default value is 'h2B for five minutes. If AGE_EN is set to 1'b1, these bits shouldn't be set to zero.

3.19 IP Priority Mapping Register 2

Address Offset: 0x0060,0x0064,0x0068,0x006C

Table 3-23 Summarizes the IP Priority Mapping Register 2

Table 3-23. **IP Priority Mapping Register 2**

Offset	Bit	R/W	Inital Value	Mnemonic	Description
0x0060	31:30	R/W	0	IP_0x3C	Priority mapping value of ipv4 TOS or ipv6 TC field. Bit7 to bit2 are used to map queue priority, but bit1 and bit0 are ignord. If TOS[7:2] or TC[7:2] is equal to 0x3C, the queue priority should be mapped to value of these bits.
	29:28	R/W	0	IP_0x38	
	27:26	R/W	0	IP_0x34	
	25:24	R/W	0	IP_0x30	
	23:22	R/W	0	IP_0x2C	
	21:20	R/W	0	IP_0x28	
	19:18	R/W	0	IP_0x24	
	17:16	R/W	0	IP_0x20	
	15:14	R/W	0	IP_0x1C	
	13:12	R/W	0	IP_0x18	
	11:10	R/W	0	IP_0x14	
	9:8	R/W	0	IP_0x10	
	7:6	R/W	0	IP_0x0C	
	5:4	R/W	0	IP_0x08	
	3:2	R/W	0	IP_0x04	
	1:0	R/W	0	IP_0x00	

Offset	Bit	R/W	Inital Value	Mnemonic	Description
0x0064	31:30	R/W	0x1	IP_0x7C	Priority mapping value of IPV4 TOS or IPV6 TC field Bits [7:2] map queue priority, but bits [1:0] are ignored. If TOS[7:2] or TC[7:2] is equal to 0x3C, the queue priority should be mapped to value of these bits.
	29:28	R/W	0x1	IP_0x78	
	27:26	R/W	0x1	IP_0x74	
	25:24	R/W	0x1	IP_0x70	
	23:22	R/W	0x1	IP_0x6C	
	21:20	R/W	0x1	IP_0x68	
	19:18	R/W	0x1	IP_0x64	
	17:16	R/W	0x1	IP_0x60	
	15:14	R/W	0x1	IP_0x5C	
	13:12	R/W	0x1	IP_0x58	
	11:10	R/W	0x1	IP_0x54	
	9:8	R/W	0x1	IP_0x50	
	7:6	R/W	0x1	IP_0x4C	
	5:4	R/W	0x1	IP_0x48	
	3:2	R/W	0x1	IP_0x44	
	1:0	R/W	0x1	IP_0x40	
0x0068	31:30	R/W	0x2	IP_0xBC	Priority mapping value of IPV4 TOS or IPV6 TC field Bits [7:2] map queue priority, but bits [1:0] are ignored. If TOS[7:2] or TC[7:2] is equal to 0x3C, the queue priority should be mapped to value of these bits.
	29:28	R/W	0x2	IP_0xB8	
	27:26	R/W	0x2	IP_0xB4	
	25:24	R/W	0x2	IP_0xB0	
	23:22	R/W	0x2	IP_0xAC	
	21:20	R/W	0x2	IP_0xA8	
	19:18	R/W	0x2	IP_0xA4	
	17:16	R/W	0x2	IP_0xA0	
	15:14	R/W	0x2	IP_0x9C	
	13:12	R/W	0x2	IP_0x98	
	11:10	R/W	0x2	IP_0x94	
	9:8	R/W	0x2	IP_0x90	
	7:6	R/W	0x2	IP_0x8C	
	5:4	R/W	0x2	IP_0x88	
	3:2	R/W	0x2	IP_0x84	
	1:0	R/W	0x2	IP_0x80	

Offset	Bit	R/W	Inital Value	Mnemonic	Description
0x006C	31:30	R/W	0x3	IP_0xFC	Priority mapping value of IPV4 TOS or IPV6 TC field Bits [7:2] map queue priority, but bits [1:0] are ignored. If TOS[7:2] or TC[7:2] is equal to 0x3C, the queue priority should be mapped to value of these bits.
	29:28	R/W	0x3	IP_0xF8	
	27:26	R/W	0x3	IP_0xF4	
	25:24	R/W	0x3	IP_0xF0	
	23:22	R/W	0x3	IP_0xEC	
	21:20	R/W	0x3	IP_0xE8	
	19:18	R/W	0x3	IP_0xE4	
	17:16	R/W	0x3	IP_0xE0	
	15:14	R/W	0x3	IP_0xDC	
	13:12	R/W	0x3	IP_0xD8	
	11:10	R/W	0x3	IP_0xD4	
	9:8	R/W	0x3	IP_0xD0	
	7:6	R/W	0x3	IP_0xCC	
	5:4	R/W	0x3	IP_0xC8	
	3:2	R/W	0x3	IP_0xC4	
	1:0	R/W	0x3	IP_0xC0	

3.20 Tag Priority Mapping Register

Address Offset: 0x0070

Table 3-24 Summarizes the Tag Priority Mapping Register

Table 3-24. **Tag Priority Mapping Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	Reserved	
15:14	R/W	0x3	TAG_0X07	Priority mapping value of TAG. If pri[2:0] in the tag is equal to 0x07, the queue priority should be mapped to value of these bits.
13:12	R/W	0x3	TAG_0X06	
11:10	R/W	0x2	TAG_0X05	
9:8	R/W	0x2	TAG_0X04	
7:6	R/W	0x1	TAG_0X03	
5:4	R/W	0x1	TAG_0X02	
3:2	R/W	0	TAG_0X01	
1:0	R/W	0	TAG_0X00	

3.21 Service Tag Register

Address Offset: 0x0074

Table 3-25 Summarizes the Service Tag Register

Table 3-25. **Service Tag Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:16	R/O	0	Reserved	
15:0	R/W	0x88A8	SERVICE_TAG	Service tag. These bits are used to recognize double tag at ingress and insert double tag at egress.

3.22 CPU Port Register

Address Offset: 0x0078

Table 3-26 Summarizes the CPU Port Register

Table 3-26. **CPU Port Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:9	R/O	0	Reserved	
8	R/W	0	CPU_PORT_EN	1''b1: cpu is connected to port0; 1'b0: no cpu is connected to switch.
7:4	R/W	0xF	MIRROR_PORT_NUM	Port number which packet should be mirrored to. 4'h0 is port0, 4'h1 is port1,etc. If the value is more than 5, no mirror port connected to switch
3:0	R/O	0x0	Reserved	

3.23 MIB Function Register 0

Address Offset: 0x0080

Table 3-27 Summarizes the MIB Function register 0

Table 3-27. **MIB Function Register 0**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	Reserved	
30	R/W	0	MIB_EN	1'b1: mib count enable. If this bit set to zero, mib module won't count.
29:27	R/O	0	Reserved	
26:24	R/W	0	MIB_FUNC	3'b000: no operation; 3'b001: flush all counters for all ports; 3'b010: reserved for future. 3'b011: capture all counters for all ports and auto-cast to cpu port; 3'b1xx:reserved for future.
23:18	R/O	0	Reserved	

Bit	R/W	Inital Value	Mnemonic	Description
17	R/W	0	MIB_BUSY	1'b1: mib module is busy now, and can't access another new command. 1'b0: mib module is empty now, and can access new command
16	R/W	1’b0	MIB_AT_HALF_EN	MIB auto-cast enable due to half flow. If this bit is set to 1'b1, MIB would be auto-cast when any counter's highest bit count to 1'b1.
15:0	R/W	15’h0	MIB_TIMER	MIB auto-cast timer. If these bits are set to zero, MIB won't auto-cast due to timer time out. The timer is times of 8.4ms, recommended value is 'h100.

3.24 MDIO Control Register

Address Offset: 0x0098

Table 3-28 Summarizes the MDIO Control register

Table 3-28. **MDIO Control register**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	MDIO_BUSY	1'b1: internal mdio interface is busy. This bit should be set to 1'b1 when cpu read or write phy register through internal mdio interface, and should be clear after hardware finish the command.
30	R/W	0	MDIO_MASTER_EN	1''b1: use mdio master to config phy register. Mdc should be changed to internal mdc to phy.
29:28	R/O	0	Reserved	
27	R/W	0	MDIO_CMD	1'b0: write 1'b1: read
26	R/W	0	MDIO_SUP_PRE	1'b1: suppose preamble enable
25:21	R/W	0	PHY_ADDR	Phy address
20:16	R/W	0	REG_ADDR	Phy register address
15:0	R/W	0	MDIO_DATA	When write, these bits are data written to phy register. When read, these bits are data read out from phy register.

3.25 LED Control Register

Address Offset: 0x00B0, 0x00B4

Table 3-29 Summarizes the LED Control register

Table 3-29. **LED Control register**

Note: This register can be hardware reset only

Offset	Bit	R/W	Inital Value	Mnemonic	Description
0x00B0	31:16	R/W	0xCB35	LED_CTRL_RULE_1	PHY 4 LED_4 control rule
	15:0	R/W	0xCB35	LED_CTRL_RULE_0	PHY 0~3 LED_[3:0] control rule
0x00B4	31:22	R/W		Reserved	
	21:20	R/W	2'b11	LED_PATTERN_EN_1	Pattern enable for port1 LED.
	19:18	R/W	2'b11	LED_PATTERN_EN_2	Pattern enable for port2 LED.
	17:16	R/W	2'b11	LED_PATTERN_EN_3	Pattern enable for port3 LED.
	15:2	R/W	00	Reserved	
	1:0	R/W	0	BLINK_HIGH_TIME	When led blinking, these bits determine led light time. 2'b00: 50% of blinking period. 250ms for 2Hz, 125ms for 4Hz, 62.5ms for 8Hz.. 2'b01: 12.5% 2'b10: 25% 2'b11: 75%

3.26 Port Control Registers — Summary for all Ports

Table 3-30 summarizes the Port Congrol Registers

Table 3-30. **Port Control Registers**

Port	Offset	Name
Port 0	***0x0100 - 0x01FC***	***Total Port 0 control register memory allocation***
	0x0100	Port status register
	0x0104	Port control register
	0x0108	Port based VLAN register
	0x010C, 0x011C, 0x0120, 0x0124	Rate limit registers
	0x0110	Priority control register
	0x0114	Storm control register
	0x0118	Queue control register
Port 1	***0x0200 - 0x01FC***	***Total Port 1 control register memory allocation***
	0x0200	Port status register
	0x0204	Port control register
	0x0208	Port based VLAN register
	0x020C, 0x021C, 0x0220, 0x0224	Rate limit registers
	0x0210	Priority control register
	0x0214	Storm control register
	0x0218	Queue control register
Port 2	***0x0300 - 0x03FC***	***Total Port 2 control register memory allocation***
	0x0300	Port status register
	0x0304	Port control register
	0x0308	Port based VLAN register
	0x030C, 0x031C, 0x0320, 0x0324	Rate limit registers
	0x0310	Priority control register
	0x0314	Storm control register
	0x0318	Queue control register

Table 3-30. **Port Control Registers (continued)**

Port	Offset	Name
Port 3	***0x0400 - 0x04FC***	***Total Port 3 control register memory allocation***
	0x0400	Port status register
	0x0404	Port control register
	0x0408	Port based VLAN register
	0x040C, 0x041C, 0x0420, 0x0424	Rate limit registers
	0x0410	Priority control register
	0x0414	Storm control register
	0x0418	Queue control register
Port 4	***0x0500 - 0x05FC***	***Total Port 4 control register memory allocation***
	0x0500	Port status register
	0x0504	Port control register
	0x0508	Port based VLAN register
	0x050C, 0x051C, 0x0520, 0x0524	Rate limit registers
	0x0510	Priority control register
	0x0514	Storm control register
	0x0518	Queue control register
Port 5	***0x0600 - 0x06FC***	***Total Port 5 control register memory allocation***
	0x0600	Port status register
	0x0604	Port control register
	0x0608	Port based VLAN register
	0x020C, 0x021C, 0x0620, 0x0624	Rate limit registers
	0x0210	Priority control register
	0x0614	Storm control register
	0x0618	Queue control register

3.27 Port Status Register

Address Offset: 0x0100 - ***Port 0***, 0x0200 - ***Port 1***, 0x0300 - ***Port 2***, 0x0400 - ***Port 3***, 0x0500 - ***Port 4,*** 0x0600 - ***Port 5***
Access: R/W

Table 3-31 Summarizes the Port Status register

Table 3-31. **Port Status register**

Bit	R/W	Inital Value	Mnemonic		Description
31:13	R/O		Reserved		
12	R/W	1	FLOW_LINK_EN		Phy link mode enable. 1'b1: enable mac flow control config auto-neg with phy 1'b0: mac can be config by software
11	R/O	0	LINK_ASYN_PAUSE_EN		Link partner support asyn flow control
10	R/O	0	LINK_PAUSE_EN		Link partner support flow control
9	R/W	0	LINK_EN		PHY link mode enable
				0	Software can configure the MAC
				1	Enable PHY link status to configure the MAC
8	RO	0	LINK		Link status
				0	PHY link down
				1	PHY link up
7	R/W	1	TX_HALF_FLOW_EN		1’b1: transmit flow conrol enable in half-duplex mode
6	R/W	0	DUPLEX_MODE		Duplex mode
				0	Half-duplex mode
				1	Full-duplex mode
5	R/W	0	RX_FLOW_EN		RXMAC Flow Control enable
4	R/W	0	TX_FLOW_EN		TXMAC Flow Control enable
3	R/W	0	RXMAC_EN		RXMAC enable
2	R/W	0	TXMAC_EN		TXMAC enable
1:0	R/W	00	SPEED		Speed mode
				00	10 Mbps
				01	100 Mbps
				10	Reserved
				11	Error speed mode

3.28 Port Control Register

Address Offset: 0x0104 - ***Port 0***, 0x0204 - ***Port 1***, 0x0304 - ***Port 2***, 0x0404 - ***Port 3***, 0x0504 - ***Port 4***, 0x0604 - ***Port 5***
Table 3-32 Summarizes the Port Control register

Table 3-32. **Port Control register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O	0	Reserved	
23	R/W	0	EAPOL_EN	1'b1: hardware acknowledge 802.1x frame, and send frame copy or redirect to cpu controlled by "EAPAL_REDIRECT_EN"
22	R/W	0	ARP_LEAKY_EN	1'b1: if mac receive ARP frame from this port, it can cross all VLAN (include port base VLAN and 802.1q). 1'b0: ARP frame can't cross vlan
21	R/W	0	IGMP_LEAVE_EN	1'b1: enable IGMP/MLD fast leave.
20	R/W	0	IGMP_JOIN_EN	1'b1: enable MLD hardware join.
19	R/W	0	DHCP_EN	1'b1: acknowledge DHCP frame enable
18	R/W	0	IPG_DEC_EN	1'b1: mac will decrease two bytes of IPG when send out frame and receive check.
17	R/W	0	ING_MIRROR_EN	Ingress port mirror. If this bit is set to 1'b1, all packets received from this port should be copied to mirror port.
16	R/W	0	EG_MIRROR_EN	Egress port mirror. If this bit is set to 1'b1, all packets send out through this port should be copied to mirror port.
15	R/W	0	Reserved	
14	R/W	0x1	LEARN_EN	Enable learn operation. 1'b1: lookup module can learn new address into address table.
13	R/W	0	Reserved	
12	R/W	0	MAC_LOOP_BACK	1'b1: enable mac loop back at mii interface
11	R/W	0	HEAD_EN	Frames transmitted out and received in with atheros header enable. If this bit is set to 1'b1, all frames transmitted and received will be added 2 bytes Atheros header.
10	R/W	0	IGMP_MLD_EN	IGMP/MLD snooping enable. If this bit is set to 1'b1, the port will examine all received frames and copy or redirect to cpu port controlled by IGMP_COPY_EN.

Bit	R/W	Inital Value	Mnemonic	Description
9:8	R/W	0	EG_VLAN_MODE	Egress VLAN mode. 2'b00: egress should transmit frames unmodified. 2'b01: egress should transmit frames without VLAN 2'b10: egress should transmit frames with VLAN 2’b11: hybrid mode
7	R/W	0	LEARN_ONE_LOCK	1'b1: this port shouldn't learn SA except first packet, and locked the address to static. 1'b0: normal learning mode.
6	R/W	0	PORT_LOCK_EN	1'b1: enable port lock. All packet received with SA not in ARL table or SA in ARL but port member is not the source port, should be redirect to cpu or drop, controlled by LOCK_DROP_EN.
5	R/W	0	LOCK_DROP_EN	1'b1: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be dropped when PORT_LOCK_EN is set to 1'b1. 1'b0: if SA is not in ARL table or SA in ARL but port member is not the source port, packet should be redirect to cpu when PORT_LOCK_EN is set to 1'b1.

Bit	R/W	Inital Value	Mnemonic	Description
4:3	R/O	0	Reserved	
2:0	R/W	3'b100	PORT_STATE	Port State. These bits are used to manage the port to determine what kind of frames are allowed to enter or leave the port for simple bridge loop detection or 803.1D Spanning Tree. 3'b000: Disable mode. The port is completely disable, and can't receive or transmit any frames. 3'b001: Blocking Mode. In this state, the port forwards received management frames to the designed port only. Any other frames can't be transmitted or received by the port, and without learning any SA address. 3'b010: Listening Mode. In this state, the port will receive and transmit only management frames, but without learning any SA address. Any other frames can't be transmitted or received by the port. 3'b011: Learning Mode. In this state, the port will learning all SA, and discard all frames except management frames, and only management frames allowed to be transmitted out. 3'b100: Forward Mode. In this state, the port will learning all SA, transmit and receive all frames like normal.

3.29 Port-based VLAN Register

Address Offset: 0x0108 - ***Port 0***, 0x0208 - ***Port 1***, 0x0308 - ***Port 2***, 0x0408 - ***Port 3***, 0x0508 - ***Port 4***, 0x0608 - ***Port 5***
Table 3-33 Summarizes the Port-based VLAN register

Table 3-33. **Port-based VLAN register**

Bit	R/W	Inital Value	Mnemonic	Description
31:29	R/W	0	ING_PORT_PRI	Port default priority for received frames.
28	R/W	0	FORCE_PORT_VLAN_EN	1'b1: force to use port base vlan enable. If this bit is set to 1'b1, use port base vlan & vlan table result to determine destination port.
27:16	R/W	0x1	PORT_DEFAULT_VID	Port Default VID. This field is used as Tagged VID added to untagged frames when transmitted from this port.
15:13	R/W	0	RES	Reserved
12	R/W	0	FORCE_DEFAULT_VID_EN	1'b1: force to use port default VID and priority for received frame, when 802.1Q mode is not disable. 1'b0: use frame tag only.
11:0	R/W	0x0	RES	Reserved

3.30 Port-based VLAN Register2

Address Offset: 0x010C - ***Port 0***, 0x020C - ***Port 1***, 0x030C - ***Port 2***, 0x040C - ***Port 3***, 0x050C - ***Port 4***, 0x060C - ***Port 5***
Table 3-33 Summarizes the Port-based VLAN register

Table 3-34. **Port-based VLAN register**

Bit	R/W	Inital Value	Mnemonic	Description
31:30	R/W	2'b00	802.1Q_MODE	802.1Q mode for this port 2'b00: 802.1Q disable. Use port base VLAN only. 2'b01: fallback. Enable 802.1Q for all received frames. Don't discard ingress membership violation and use the port base VLAN if the frame's VID isn't contained in VLAN Table. 2'b10: check. Enable 802.1Q for all received frames. Don't discard ingress membership violation but discard frames which VID isn't contained in VLAN Table. 2'b11: secure. Enable 802.1Q for all received frames. Discard frames with ingress membership violation or whose VID isn't contained in the VLAN Table.
29	R/W	0	CORE_PORT_EN	1'b0: egde port 1'b1: core port
28:27	R/W	0	ING_VLAN_MODE	2'b00: all frame can be received in, include untagged and tagged 2'b01: only frame with tag can be received by this port. 2'b10: only frame untagged can be received by this port, include no vlan and priority vlan. 2'b11: reserved for future.
26:24	R/W	0	Reserved	
23	R/W	0	VLAN_PRI_PRO_EN	1'b1: VLAN priority propagation enable

Bit	R/W	Inital Value	Mnemonic	Description
22:16	R/W	Port0: 111110 Port1: 111101 ……	PORT_VID_MEM	Port Base VLAN Member. Each bit restrict which port can send frames to. To send frames to port0, bit 16 must be set to 1'b1, etc. These bits are set to one after reset except the port's bit. This prevents frames going out the port they were received in.
15	R/O	0	Reserved	
14	R/W	0	UNI_LEAKY_EN	unicast frame leaky VLAN enable. Also use ARL_UNI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_UNI_LEAKY_EN is set to zero, only UNI_LEAKE_EN control unicast frame leaky VLAN. If ARL_UNI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore UNI_LEAKY_EN. If mac receive unicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base and 802.1q).
13	R/W	0	MULTI_LEAKY_EN	Multicast frame leaky VLAN enable. Also use ARL_MULTI_LEAKY_EN and LEAKY_EN bit in ARL table to control unicast leaky VLAN. When ARL_MULTI_LEAKY_EN is set to zero, only MULTI_LEAKE_EN control multicast frame leaky VLAN. If ARL_MULTI_LEAKY_EN is set to 1'b1, only frame with DA in ARL table and LEAKY_EN bit is set to 1'b1 can be forward as leaky VLAN, ignore MULTI_LEAKE_EN. If mac receive multicast frame from this port which should forward as leaky VLAN, the frame could be switched to destination port defined in ARL table and cross all VLAN (include port base VLAN and 802.1q).
12:0	R/O	0	Reserved	

3.31 Rate Limit Register

Address Offset: 0x0110 - ***Port 0***, 0x0210 - ***Port 1,*** 0x0310 - ***Port 2***, 0x0410 - ***Port 3***, 0x0510 - ***Port 4***, 0x0610 - ***Port 5***

Table 3-37 Summarizes the Storm Control register

Table 3-35. **Rate Limit Register**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/W	b'h18	ADD_RATE_BYTE	Byte number should be added to frame when calculate rate limit. Default is 24 bytes for IPG, preamble, crc and SFD.
23	R/W	0	RES	Reserved
22	R/W	0	EGRESS_MANAGE_RATE_EN	Enable management frame to be calculate to egress rate limit .
21	R/W	0	INGRESS_MANAGE_RATE_EN	Enable management frame to be calculate to ingress rate limit .
20	R/W	0	INGRESS_MULTI_RATE_EN	Enable multicast frame which da can be found in ARL table to be calculate to ingress rate limit .
19:13	R/O	0	Reserved	
12:0	R/W	0x1FFF	ING_RATE	Ingress Rate Limit for all priority. Rate is limited to times of 32kbps. Default 13'h1FFF is for disable rate limit for ingress. if these bits are set to 13'h0, no frame should be received in from this port.

3.32 Priority Control Register

Address Offset: 0x0114 - ***Port 0***, 0x0214 - ***Port 1***, 0x0314 - ***Port 2***, 0x0414 - ***Port 3***, 0x0514 - ***Port 4,*** 0x0614 - ***Port 5***

Table 3-36 Summarizes the Priority Control register

Table 3-36. **Priority Control register**

Bit	R/W	Inital Value	Mnemonic	Description
31:20	R/O	0	Reserved	
19	R/W	1	PORT_PRI_EN	1'b1: port base priority can be used for QOS.
18	R/W	0	DA_PRI_EN	1'b1: DA priority can be used for QOS.
17	R/W	0	VLAN_PRI_EN	1'b1: VLAN priority can be used for QOS.
16	R/W	0	IP_PRI_EN	1'b1: TOS/TC can be used for QOS.
15:8	R/O		Reserved	
7:6	R/W	0	DA_PRI_SEL	DA priority selected level for QOS. There are five levels priority for QOS. The highest is priority in packet header. The others are selected by these bits. If these bits are set to zero, DA priority is selected after header. If these bits are set to n, DA priority is selected after the priority set to n-1.
5:4	R/W	1	VLAN_PRI_SEL	VLAN priority selected level for QOS.
3:2	R/W	2	IP_PRI_SEL	IP priority selected level for QOS.
1:0	R/W	3	PORT_PRI_SEL	Port base priority selected level for QOS

3.33 Storm Control Register

Address Offset: 0x0118 - ***Port 0***, 0x0218 - ***Port 1***, 0x0318 - ***Port 2***, 0x0418 - ***Port 3***, 0x0518 - ***Port 4***, 0x0618 - ***Port 5***

Table 3-37 Summarizes the Storm Control register

Table 3-37. **Storm Control register**

Bit	R/W	Inital Value	Mnemonic	Description
31:26	R/O	0	Reserved	
25:24	R/W	0	Reserved	
23:11	R/O	0	Reserved	
10	R/W	0	MULTI_STORM_EN	1'b1: enable unknown multicast frame calculate to storm control.

Bit	R/W	Inital Value	Mnemonic	Description
9	R/W	0	UNI_STORM_EN	1'b1: enable unknown unicast frame calculate to storm control.
8	R/W	0	BROAD_STORM_EN	1'b1: enable broadcast frame calculate to storm control.
7:4	R/O	0	Reserved	
3:0	R/W	0	STORM_RATE	Storm control rate. - 4'h0: storm control disable 4'h1: 1k frame per second 4'h2: 2k frame per second 4'h3: 4k frame per second 4;h4: 8k frame per second 4;h5: 16k frame per second 4'h6: 32k frame per second 4'h7: 64k frame per second …….. 4'hB: 1M frame per second.

3.34 Queue Control Register

Address Offset: 0x011C - ***Port 0***, 0x021C - ***Port 1***, 0x031C - ***Port 2***, 0x041C - ***Port 3***, 0x051C - ***Port 4***, 0x061C - ***Port 5***
Table 3-38 Summarizes the Queue Control register

Table 3-38. **Queue Control register**

Bit	R/W	Inital Value	Mnemonic	Description
31:28	R/O	0x0	Reserved	
27:26	R/O	0	Reserved	
25	R/W	0x1	PORT_QUEUE_CTRL_EN	1'b1: enable use PORT_QUEUE_NUM to control queue depth in this port.
24	R/W	0x1	PRI_QUEUE_CTRL_EN	1'b1: enable use PRI*_QUEUE_NUM to control queue depth in this port.
23:22	R/O		Reserved	
21:16	R/W	0x2A	PORT_QUEUE_NUM	Most buffer can be used for this port. Buffer number is times of 4. 6'h0: 0 6'h1: no more than 4 6'h2: no more than 8 …… 6'h31F: no more than 252

Bit	R/W	Inital Value	Mnemonic	Description
15:12	R/W	0x8	PRI3_QUEUE_NUM	Most buffer can be used for priority 3 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60
11:8	R/W	0x8	PRI2_QUEUE_NUM	Most buffer can be used for priority 2 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60
7:4	R/W	0x8	PRI1_QUEUE_NUM	Most buffer can be used for priority 1 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60
3:0	R/W	0x8	PRI0_QUEUE_NUM	Most buffer can be used for priority 0 queue. Buffer number is times of 4. 4'h0: 0 4'h1: no more than 4 4'h2: no more than 8 …… 4'hF: no more than 60

3.35 Rate Limit Register 1

Address Offset: 0x0120 - ***Port 0***, 0x0220 - ***Port 1***, 0x0320 - ***Port 2***, 0x0420 - ***Port 3***, 0x0520 - ***Port 4***, 0x0620 - ***Port 5***

Table 3-39 Summarizes the Rate Limit register 1

Table 3-39. **Rate Limit register 1**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/O	0		
30:16	R/O	0	Reserved	
15	R/O	0		
12:0	R/W	0x1FFF	EG_PRI_RATE	Egress Rate Limit for priority 0. Rate is limited to times of 32kbps. Default 13'h1FFF is for disable rate limit for egress. If these bits are set to 13'h0, no egress frame should be send out from this port.

3.36 Rate Limit Register 3

Address Offset: 0x0128 - ***Port 0***, 0x0228 - ***Port 1***, 0x0328 - ***Port 2***, 0x0428 - ***Port 3***, 0x0528 - ***Port 4***, 0x0628 - ***Port 5***

Table 3-40 Summarizes the Rate Limit register 3

Table 3-40. **Rate Limit register 3**

Bit	R/W	Inital Value	Mnemonic	Description
31:24	R/O		Reserved	
23:22	R/W	2'b00	Reserved	
21:20	R/W	2'b00	Reserved	
19:18	R/W	2'b00	Reserved	
17:16	R/W	2'b01	Reserved	

Bit	R/W	Inital Value	Mnemonic	Description
15:3	R/O	0	Reserved	
2:0	R/W	0x2	EG _TIME_SLOT	Egress rate limit time slot control register. 3'h0: 1/128 ms 3'h1: 1/64 ms 3'h2: 1/32 ms 3'h3: 1/16 ms 3'h4: 1/4 ms 3'h5: 1 ms 3'h6: 10 ms 3'h7: 100 ms

3.37 Round-Robin Register

Address Offset: 0x012C - ***Port 0***, 0x022C - ***Port 1***, 0x032C - ***Port 2***, 0x042C - ***Port 3***, 0x052C - ***Port 4***, 0x062C - ***Port 5***

Table 3-40 Summarizes the Rate Limit register 2

Table 3-41. **Rate Limit register 2**

Bit	R/W	Inital Value	Mnemonic	Description
31	R/W	0	Reserved	
30:29	R/W	2'b00	WEIGHT_PRI_CTRL	2'b00: strict priority 2'b01: only highest queue use strick priority, others use weighted fair queuing schme 2'b10: the highest two queues use strick priority, other two queues use weighted fair queuing schme. 2'b11: all queues use weighted fair queuing schme 8:4:2:1.
28:0	R/O	0	Reserved	

4. PHY Control Registers

Table 3-2 summarizes the PHY Control registers.

Table 4-1. **PHY Register Summary**

Offset	Description	Page
0	Control Register	page 74
1	Status Register	page 76
2	PHY Identifier	page 78
3	PHY Identifier 2	page 79
4	Auto-negotiation Advertisement Register	page 80
5	Link Partner Ability Register	page 84
6	Auto-negotiation Expansion Register	page 80
7	Reserved	
8	Reserved	
9	Reserved	
10	Reserved	
11	Reserved	
12	Reserved	
13	Reserved	
14	Reserved	
15	Reserved	
16	PHY-specific Control Register	page 89
17	PHY-specific Status Register	page 89
18	Interrupt Enable Register	page 91
19	Interrupt Status Register	page 93
20	Extended PHY-specific Register	page 95
21	Receive Error Counter Register	page 96
22	Virtual Cable Tester Control Register	page 96
23	Reserved	
24	LED Control Register	
25	Manual LED Override Register	
26	Reserved	
27	Reserved	
28	Virtual Cable Tester Status Register	page 97
29	Debug port 1 (Address Offset)	page 98
30	Reserved	
31	Reserved	

4.38 Control Register

Address Offset: 0x00

Table 4-2 summarizes the Registers

Table 4-2. **Control Register**

Bit	Symbol	Type		Description
15	Reset	Mode	R/W	PHY Software Reset. Writing a "1" to this bit causes the PHY the reset operation is done , this bit is cleared to "0" automatically. The reset occurs immediately. 1= PHY reset 0 =Normal operation
		HW Rst	0	
		SW Rst	SC	
14	Loopback	Mode	R/W	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. 1 = Enable Loopback 0 = Disable Loopback
		HW Rst	0	
		SW Rst	0	
13	Speed Selection	Mode	R/W	(00:10Mbps,01:100Mbps,10:Reserved,11:Reserved)
		HW Rst		
		SW Rst		
12	Auto-negotiation	Mode	R/W	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
		HW Rst		
		SW Rst		
11	Power Down	Mode	R/W	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0.9) are not set by the user. 1 = Power down 0 = Normal operation
		HW Rst	0	
		SW Rst	0	
10	Isolate	Mode	R/W	The MII output pins are tri-stated when this bit is set to 1. The MII inputs are ignored. 1 = Isolate 0 = Normal operation
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
9	Restart Auto-negotiation	Mode	R/W, SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
		HW Rst	0	
		SW Rst	SC	
8	Duplex Mode	Mode	R/W, SC	1:Full Duplex 0 :Half Duplex
		HW Rst		
		SW Rst		
7	Collision Test	Mode	R/W	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
		HW Rst	0	
		SW Rst	0	
6	Speed Selection (MSB)	Mode	R/W	See bit 0.13
		HW Rst	See Desc.	
		SW Rst		
5:0	Reserved	Mode	RO	Will always be 00000.
		HW Rst	000000	
		SW Rst	00000	

4.39 Status Register

Address Offset: 0x01, or 0d01

Table 4-3 summarizes the Registers

Table 4-3. **Status Register**

Bit	Symbol	Type		Description
15	100Base-T4	Mode	RO	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
		HW Rst	Always 0	
		SW Rst	Always 0	
14	100Base-TX	Mode	RO	Capable of 100-Tx Full Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
13	10 Mbps Full-Duplex	Mode	RO	Capable of 100-Tx Full Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
12	10 Mbps Full-Duplex	Mode	RO	Capable of 100-Tx Full Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
11	100Base-T2 Half-Duplex	Mode	RO	Capable of 100-Tx Full Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
10	100Base-T2 Full-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst	Always 0	
		SW Rst	Always 0	
9	100Base-T2 Half-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst	Always 0	
		SW Rst	Always 0	
8	Reserved	Mode	RO	Always 0
		HW Rst	Always 0	
		SW Rst	Always 0	
7	Reserved	Mode	RO	Always 0
		HW Rst	Always 0	
		SW Rst	Always 0	
6	MF Preamble Suppression	Mode	RO	PHY accepts management frames with preamble suppressed
		HW Rst	Always 1	
		SW Rst	Always 1	

Bit	Symbol	Type		Description
5	Auto-negotiation Complete	Mode	RO	1: Auto negotiation process complete 0:Auto negotiation process not complete
		HW Rst	0	
		SW Rst	0	
4	Remote Fault	Mode	RO, LH	1: Remote fault condition detected 0:Remote fault condition not detected
		HW Rst	0	
		SW Rst	0	
3	Auto-negotiation Ability	Mode	RO	1 : PHY able to perform auto negotiation
		HW Rst	Always 1	
		SW Rst	Always 1	
2	Link Status	Mode	RO, LL	This register bit indicates whether the link was lost since the last read. For the current link status, read register bit 17.10 Link Real Time. 1 = Link is up 0 = Link is down
		HW Rst	0	
		SW Rst	0	
1	Jabber Detect	Mode	RO, LH	1: Jabber condition detected 0: Jabber condition not detected
		HW Rst	0	
		SW Rst	0	
0	Extended Capability	Mode	RO	1: Extended register capabilities
		HW Rst	Always 1	
		SW Rst	Always 1	

4.40 PHY Identifier

Address Offset: 0x02 or 0d02

Table 4-4 summarizes the Registers

Table 4-4. **PHY Identifier**

Bit	Symbol	Type		Description
15:0	Organizationally Unique Identifer Bit 3:18	Mode	RO	Organizationally Unique Identifier bits 3:18
		HW Rst	Always 16'h004d	
		SW Rst	Always 16'h004d	

4.41 PHY Identifier 2

Address Offset: 0x03, or 0d03

Table 4-5 summarizes the Registers

Table 4-5. **PHY Identfier 2**

Bit	Symbol	Type		Description
15	OUI LSB Model Number Revision Number	Mode	RO	Organizationally Unique Identifier bits 19:24
		HW Rst	Always 16'hd043	
		SW Rst	Always 16'hd043	

4.42 Auto-negotiation Advertisement Register

Address Offset: 0x04, or 0d04

Table 4-6 summarizes the Registers

Table 4-6. **Auto-negotiation Advertisement Register**

Bit	Symbol	Type		Description
15	Reserved	Mode	R/W	Always 0
		HW Rst	0	
		SW Rst	0	
14	Ack	Mode	RO	Must be 0
		HW Rst	Always 0	
		SW Rst	Always 0	
13	Remote Fault	Mode	R/W	1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
		HW Rst	Always 0	
		SW Rst	Always 0	
12	Reserved	Mode	RO	Always 0.
		HW Rst	Always 0	
		SW Rst	Always 0	
11	Asymmetric Pause	Mode	R/W	The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs: Software reset is asserted (register 0.15) Restart Auto-Negotiation is asserted (register 0.9) Power down (register 0.11) transitions from power down to normal operation Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause (this bit has added the pad control and can be set from the F001 top, its default value is one)
		HW Rst	1	
		SW Rst	Update	

<table>
<tr><th>Bit</th><th>Symbol</th><th colspan="2">Type</th><th>Description</th></tr>
<tr><td rowspan="3">10</td><td rowspan="3">PAUSE</td><td>Mode</td><td>R/W</td><td rowspan="3">The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs:

Software reset is asserted (register 0.15)

Restart Auto-Negotiation is asserted (register 0.9)

Power down (register 0.11) transitions from power down to normal operation

Link goes down

1 = MAC PAUSE implemented
0 = MAC PAUSE not implemented
(this bit has added the pad control and can be set from the F001 top, its default value is one)</td></tr>
<tr><td>HW Rst</td><td>1</td></tr>
<tr><td>SW Rst</td><td>Update</td></tr>
<tr><td rowspan="3">9</td><td rowspan="3">100Base-T4</td><td>Mode</td><td>RO</td><td rowspan="3">Not able to perform 100BASE-T4</td></tr>
<tr><td>HW Rst</td><td>Always 0</td></tr>
<tr><td>SW Rst</td><td>Always 0</td></tr>
<tr><td rowspan="3">8</td><td rowspan="3">100Base -TX</td><td>Mode</td><td>R/W</td><td rowspan="3">The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs:

Software reset is asserted (register 0.15)

Restart Auto-Negotiation is asserted (register 0.9)

Power down (register 0.11) transitions from power down to normal operation

Link goes down

1 = Advertise
0 = Not advertised</td></tr>
<tr><td>HW Rst</td><td>1</td></tr>
<tr><td>SW Rst</td><td>Update</td></tr>
</table>

Bit	Symbol	Type		Description
7	100BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs: Software reset is asserted (register 0.15) Restart Auto-Negotiation is asserted (register 0.9) Power down (register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
6	10BASE-TX Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing to this register. But the value written to this bit does not takes effect until any one of the following occurs: Software reset is asserted (register 0.15) Restart Auto-Negotiation is asserted (register 0.9) Power down (register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	

Bit	Symbol	Type		Description
5	10BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: Software reset is asserted (register 0.15) Restart Auto-Negotiation is asserted (register 0.9) Power down (register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
4:0	Selector Field	Mode	RO	Selector Field mode 00001 = 802.3
		HW Rst	Always 00001	
		SW Rst	Always 00001	

4.43 Link Partner Ability Register

Address Offset: 0x05, or 0d05

Table 4-7 summarizes the Registers

Table 4-7. **Link Partner Ability Register**

Bit	Symbol	Type		Description
15	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
14	Ack	Mode	RO	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
		HW Rst	0	
		SW Rst	0	
13	Remote Fault	Mode	RO	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
		HW Rst	0	
		SW Rst	0	
12	Reserved	Mode	RO	Technology Ability Field Received Code Word Bit 12
		HW Rst	0	
		SW Rst	0	
11	Asymmetric Pause	Mode	RO	Technology Ability Field Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
		HW Rst	0	
		SW Rst	0	
10	PAUSE	Mode	RO	Technology Ability Field Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
		HW Rst	0	
		SW Rst	0	
9	100BASE-T4	Mode		Technology Ability Field Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
		HW Rst		
		SW Rst		

Bit	Symbol	Type		Description
8	100BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
		HW Rst	0	
		SW Rst	0	
7	100BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
		HW Rst	0	
		SW Rst	0	
6	10BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
		HW Rst	0	
		SW Rst	0	
5	10BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
		HW Rst	0	
		SW Rst	0	
4:0	Selector field	Mode	RO	Selector Field Received Code Word Bit 4:0
		HW Rst	00000	
		SW Rst	00000	

4.44 Auto-negotiation Expansion Register

Address Offset: 0x06, or 0d06

Table 4-8 summarizes the Registers

Table 4-8. **Auto-negotiation Expansion Register**

Bit	Symbol	Type		Description
15:5	Reserved	Mode	RO	Reserved. Must be 0.
		HW Rst	Always 0x000	
		SW Rst	Always 0x000	
4	Parallel Detection Fault	Mode	RO, LH	1: a fault has been detect 0: no fault has been detected
		HW Rst	0	
		SW Rst	0	
3	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
2	Reserved	Mode	R/W	
		HW Rst	1	
		SW Rst	1	
1	Reserved	Mode	RO, LH	Always 0
		HW Rst	0	
		SW Rst	0	
0	Link Partner Auto-negotiation Able	Mode	RO	1: Link partner is auto negotiation able 0: Link partner is not auto negotiation able
		HW Rst	0	
		SW Rst	0	

4.45 Function Control Register

Address Offset: 0x10, or 0d16

Table 4-9 summarizes the Registers

Table 4-9. **Function Control Register**

Bit	Symbol	Type		Description
15:12	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
11	Assert CRS on Transmit	Mode	R/W	11
		HW Rst	0	
		SW Rst	Retain	
10	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
9:8	Energy Detect	Mode	R/W	0x = Off 10 = Sense only on Receive (Energy Detect) 11 = Sense and periodically transmit NLP
		HW Rst	0	
		SW Rst	0	
6:5	MDI Crossover Mode	Mode	R/W	Changes to these bits are disruptive to the normal operation; therefore any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
		HW Rst	11	
		SW Rst	Updage	
4:3	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
2	SQE Test	Mode	R/W	SQE Test is automatically disabled in full-duplex mode. 1 = SQE test enabled 0 = SQE test disabled
		HW Rst	0	
		SW Rst	Retain	
1	Polarity Reversal	Mode	R/W	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled
		HW Rst	0	
		SW Rst	Retain	

Bit	Symbol	Type		Description
0	Disable Jabber	Mode	R/W	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function
		HW Rst	0	
		SW Rst	Retain	

4.46 PHY Specific Status Register

Address Offset: 0x11, or 0d17

Table 4-10 summarizes the Registers

Table 4-10. **PHY Specific Status Register**

Bit	Symbol	Type		Description
15:14	Speed	Mode	RO	These status bits are valid when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = Reserved 01 = 100 Mbps 00 = 10 Mbps
		HW Rst	00	
		SW Rst	Retain	
13	Duplex	Mode	RO	This status bit is valid only Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
		HW Rst	0	
		SW Rst	Retain	
12	Page Received (Real Time)	Mode	RO	1 = Page received 0 = Page not received
		HW Rst	0	
		SW Rst	Retain	
11	Speed and Duplex Resolved	Mode	RO	When Auto-Negotiation is not enabled for force speed mode. 1 = Resolved 0 = Not resolved
		HW Rst	0	
		SW Rst	0	
10	Link (Real Time)	Mode	RO	1 = Link up 0 = Link down
		HW Rst	0	
		SW Rst	0	
9:7	Reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
6	MDI Crossover Status	Mode	RO	This status bit is valid only when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = MDIX 0 = MDI
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed downgrade	Mode	RO	1 = Downgrade 0 = No Downgrade
		HW Rst	0	
		SW Rst	0	

Bit	Symbol	Type		Description
4	Energy Detect Status	Mode	RO	1 = Sleep 0 = Active
		HW Rst	0	
		SW Rst	0	
3	Transmit Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disabled
		HW Rst	0	
		SW Rst	0	
2	Receive Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
		HW Rst	0	
		SW Rst	Retain	
1	Polarity (Real Time)	Mode	RO	1 = Reversed 0 = Normal
		HW Rst	0	
		SW Rst	0	
0	Jabber (Real Time)	Mode	RO	1 = Jabber 0 = No jabber
		HW Rst	0	
		SW Rst	Retain	

4.47 Interrupt Enable Register

Address Offset: 0x12, or 0d18

Table 4-11 summarizes the Registers

Table 4-11. **Interrupt Enable Register**

Bit	Symbol	Type		Description
15	Auto-Negotiation Error Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
14	Speed Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
13	Duplex Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
12	Page Received Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
11	Auto-Negotiation Completed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
10	Link Status Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
9	Symbol Error Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
8	False Carrier Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
7	FIFO Over/ Underflow Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
6	MDI Crossover Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	

Bit	Symbol	Type		Description
5	Wirespeed-downgrade Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
4	Energy Detect Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
3:2	Reserved	Mode	R/W	Always 00
		HW Rst	0	
		SW Rst	Retain	
1	Polarity Changed Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
0	Jabber Interrupt Enable	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	

4.48 Interrupt Status Register

Address Offset: 0x13, or 0d19

Table 4-12 summarizes the Registers

Table 4-12. **Interrupt Status Register**

Bit	Symbol	Type		Description
15	Auto-Negotiation Error	Mode	RO, LH	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error
		HW Rst	0	
		SW Rst	Retain	
14	Speed Changed	Mode	RO, LH	1 = Speed changed 0 = Speed not changed
		HW Rst	0	
		SW Rst	Retain	
13	Duplex Changed	Mode	RO, LH	1 = Duplex changed 0 = Duplex not changed
		HW Rst	0	
		SW Rst	Retain	
12	Page Received	Mode	RO	1 = Page received 0 = Page not received
		HW Rst	0	
		SW Rst	Retain	
11	Auto-Negotiation Completed	Mode	RO	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
		HW Rst	0	
		SW Rst	Retain	
10	Link Status Changed	Mode	RO, LH	1 = Link status changed 0 = Link status not changed
		HW Rst	0	
		SW Rst	Retain	
9	Symbol Error	Mode	RO, LH	1 = Symbol error 0 = No symbol error
		HW Rst	0	
		SW Rst	Retain	
8	False Carrier	Mode	RO, LH	1 = False carrier 0 = No false carrier
		HW Rst	0	
		SW Rst	Retain	
7	FIFO Over/Underflow	Mode	RO, LH	1 = Over/Underflow Error 0 = No FIFO Error Not implement, always 0.
		HW Rst	0	
		SW Rst	Retain	

Bit	Symbol	Type		Description
6	MDI Crossover Changed	Mode	RO, LH	1 = Crossover changed 0 = Crossover not changed
		HW Rst	0	
		SW Rst	Retain	
5	Wirespeed-downgrade Interrupt	Mode	RO, LH	1 = Wirespeed-downgrade detected. 0 = No Wirespeed-downgrade.
		HW Rst	0	
		SW Rst	Retain	
4	Energy Detect Changed	Mode	RO, LH	1 = Energy Detect state changed 0 = No Energy Detect state change detected Not implement, always 0.
		HW Rst	0	
		SW Rst	Retain	
3:2	Reserved	Mode	RO, LH	Always 0
		HW Rst	0	
		SW Rst	Retain	
1	Polarity Changed	Mode	RO, LH	1 = Polarity Changed 0 = Polarity not changed
		HW Rst	0	
		SW Rst	Retain	
0	Jabber	Mode	RO, LH	1 = Jabber 0 = No jabber
		HW Rst	0	
		SW Rst	Retain	

4.49 Receive Error Counter Register

Address Offset: 0x15, or 0d21

Table 4-13 summarizes the Registers

Table 4-13. **Status Register**

Bit	Symbol	Type		Description
15:0	Receive Error Count	Mode	RO	Counter will peg at 0xFFFF and will not roll over. (when rx_dv is valid, count rx_er numbers) (in this version, only for 100Base-T and 1000Base-T)
		HW Rst	0x0000	
		SW Rst	Retain	

4.50 Virtual Cable Tester Control Register

Address Offset: 0x16, or 0d22

Table 4-14 summarizes the Registers

Table 4-14. **Virtual Cable Tester Contol Register**

Bit	Symbol	Type		Description
15:10	Reserved	Mode	RO	Reserved
		HW Rst	Always 0	
		SW Rst	Always 0	
9:8	MDI Pair Select	Mode	R/W	Virtual Cable Tester™ Control registers. Use the Virtual Cable Tester Control Registers to select which MDI pair is shown in the Virtual Cable Tester Status register. 00 = MDI[0] pair 01 = MDI[1] pair 10 = MDI[2] pair 11 = MDI[3] pair
		HW Rst	00	
		SW Rst	Retain	
7:1	Reserved	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
0	Enable Test	Mode	R/W	When set, hardware automatically disable this bit when VCT is done. 1 = Enable VCT Test 0 = Disable VCT Test
		HW Rst	0	
		SW Rst	Retain	

4.51 Virtual Cable Tester Status Register

Address Offset: 0x1C, or 0d28

Table 4-15 summarizes the Registers

Table 4-15. **Virtual Cable Tester Status Register**

Bit	Symbol	Type		Description
15:10	Reserved	Mode	RO	Reserved.
		HW Rst	Always 0	
		SW Rst	Always 0	
9:8	Status	Mode	RO	The content of the Virtual Cable Tester Status Registers applies to the cable pair selected in the Virtual Cable Tester™ Control Registers. 11 = linkup state, no open or short in cable. 00 = Valid test, normal cable (no short or open in cable) 10 = Valid test, open in cable for MDI pair 01 = Valid test, short in cable for MDI pair
		HW Rst	00	
		SW Rst	00	
7:0	Delta_Time	Mode	R/W	Delta time to indicate distance. Length = Delta_Time * 0.824
		HW Rst	0	
		SW Rst	0	

4.52 Debug Port (Address Offset)

Address Offset: 0x1D, or 0d29

Table 4-16 summarizes the Registers

Table 4-16. **Debug Port (Address Offset)**

Bit	Symbol	Type		Description
15:6	Reserved	Mode	RO	
		HW Rst	0	
		SW Rst	0	
5:0	Address Offset	Mode	R/W	The address index of the register will be write or read.
		HW Rst	0	
		SW Rst	0	

4.53 Debug Port 2 (R/W Port)

Address Offset: 0x1E, or 0d20

Table 4-17 summarizes the Registers

Table 4-17. **Debug Port 2 (R/W Port)**

Bit	Symbol	Type		Description
15:0	Debug Data Port	Mode	R/W	The data port of debug register. Before access this register, must set the address offset first.
		HW Rst	0	
		SW Rst	0	

4.54 Debug Register — Analog Test Control

Address Offset: 0x00, or 0d00

Table 4-16 summarizes the Registers

Table 4-18. **Debug Register — Analog Test Control**

Bit	Symbol	Type		Description
15	RES			
14:10	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	0	
9	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
8	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
7	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
6	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
5	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
4	10_ClassA	Mode	R/W	This bit is 10BT Class AB, class A select bit:
		HW Rst	0	
		SW Rst	Retain	1'b0 : 10BT in Class AB mode; 1'b1 : 10BT in Class A mode.
3:1	RES	Mode	R/W	Reserved
		HW Rst	3'b111	
		SW Rst	0	
0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	

4.55 Debug Register — System Mode Control

Address Offset: 0x05, or 0d05

Table 4-16 summarizes the Registers

Table 4-19. **Debug Register — System Control Mode**

Bit	Symbol	Type		Description
15	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
14	RES	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
13	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
12	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
11	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
10	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
9	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
8	RES			Reserved
7	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
6	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	

Bit	Symbol	Type		Description
5:4	RES	Mode	R/W	Reserved
		HW Rst	2'b00	
		SW Rst	Retain	
3	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	
2	RES	Mode	R/W	Reserved
		HW Rst	1	
		SW Rst	Retain	
1	100_ClassA	Mode	R/W	This bit is 100BT ClassA and ClassAB mode select bit. 0: 100BT ClassAB; 1: 100BT ClassA;
		HW Rst	1	
		SW Rst	Retain	
0	RES	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Retain	

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1 summarizes the absolute maximum ratings and Table 5-2 lists the recommended operating conditions for the AR8236. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 5-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
AVDD2P5	2.5 V analog supply voltage	3.0	V
AVDD	1.2 V digital core supply voltage	1.6	V
DVDD_IO	2.5 V digital supply voltage	3.0	V
DVDD	1.2 V digital supply voltage	1.6	V
VDD3P3	3.3 V digital I/O supply voltage	4.0	V
T_{store}	Storage temperature	–65 to 150	°C
ESD	Electrostatic discharge tolerance	2000	V

5.2 Recommended Operating Conditions

Table 5-2. **Recommended Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit
VDD3P3	3.3 V I/O voltage	3.0	3.3	3.6	V
AVDD2P5/DVDD_IO	2.5 V analog/digital	2.40	2.62	2.75	V
AVDD/DVDD	1.2 V analog/digital	1.14	1.2	1.26	V
$T_{ambient}$	Ambient Temperature	0	—	70	°C
T_J	Junction Temperature	0	—	120	°C
Ψ_{JT}	Junction to Top Center	—	3	—	°C/W

5.3 MII Characteristics

Table 5-3 shows the MII DC characteristics.

Table 5-3. **MII DC Characteristics**

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high voltage	2.0	—	V
V_{OL}	Output low voltage	—	0.4	V
I_{IH}	Input high current	—	–0.4	mA
I_{IL}	Input low current	0.4	—	mA
VIH	Input high voltage	1.7	—	V
VIL	Input high voltage	—	0.7	V

5.4 *Power-on Strapping*

Table 5-4 shows the pin-to-PHY core configuration signal power-on strapping.

Table 5-4. **Power-On Strapping**

Pin Name	Pin Signal	Pin	Description	
MDIO_EN	SPI_DO	46	0	UART interface
			1	MDIO interface
SPI_SIZE	RXD0_0	54	0	1K
			1	4K or 2K
FUNC_MODE0	SPI_CS	45	00	Normal Operation
FUNC_MODE1	SPI_CLK	44	01	Test Mode
			10	
			11	
LED_OPEN_EN	RXD1_1	58	0	Driver
			1	Open Drain
SPI_EN	RXD0_1	59	0	No EEPROM connected
			1	EEPROM enable
PWR_SEL	RXD1	53	0	2.6V Power Input
			1	3.3V Power Input

5.4.8 *Power-on-Reset Timing*

Figure 5-2 shows the Power-on-Reset timing diagram.

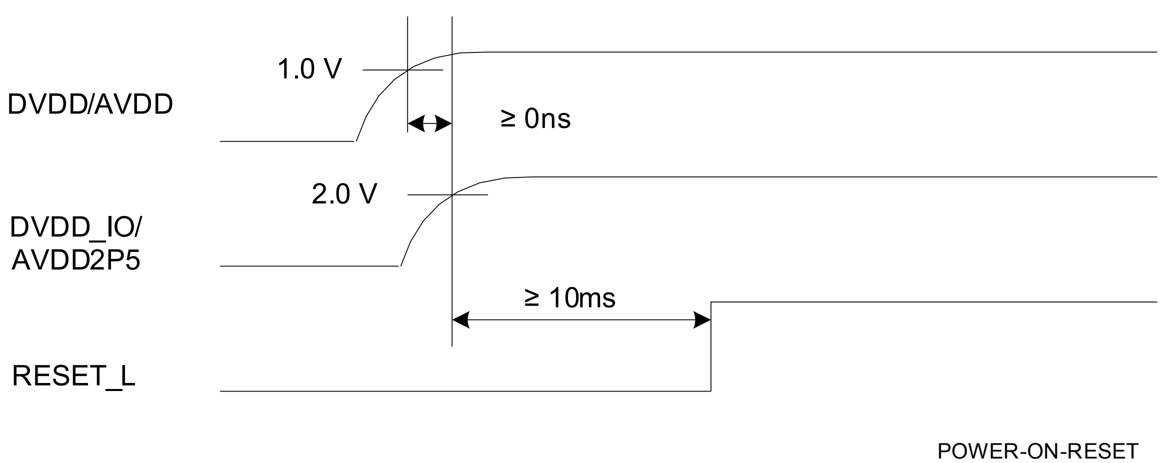


Figure 5-1. **Power-on-Reset Timing Diagram**

5.5 AC Timing

5.5.9 OSC Timing

Figure 5-2 shows the OSC timing diagram.

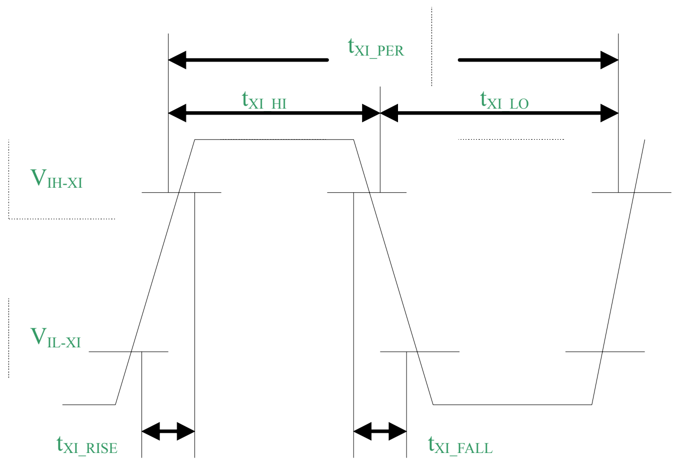


Figure 5-2. **OSC Timing Diagram**

Table 5-5. **OSC Timing**

Symbol	Parameter	Min	Typ	Max	Unit
T_XI_PER	XI/OSCI Clock Period	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
T_XI_HI	XI/OSCI Clock High	14	20.0		ns
T_XI_LO	XI/OSCI Clock Low	14	20.0		ns
T_XI_RISE	XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min)			4	ns
T_XI_FALL	XI/OSCI Clock Fall time, V_{IL} (max) to V_{IH} (min)			4	ns
V_IH_XI	The XTLI input high level	0.8		1.4	V
V_IL_XI	The xtli input low lever voltage	-0.3		0.15	V

NOTE: The timing specification above is for the OSC input signal

5.5.10 MII Timing

Figure 5-3 shows the MII timing diagram.

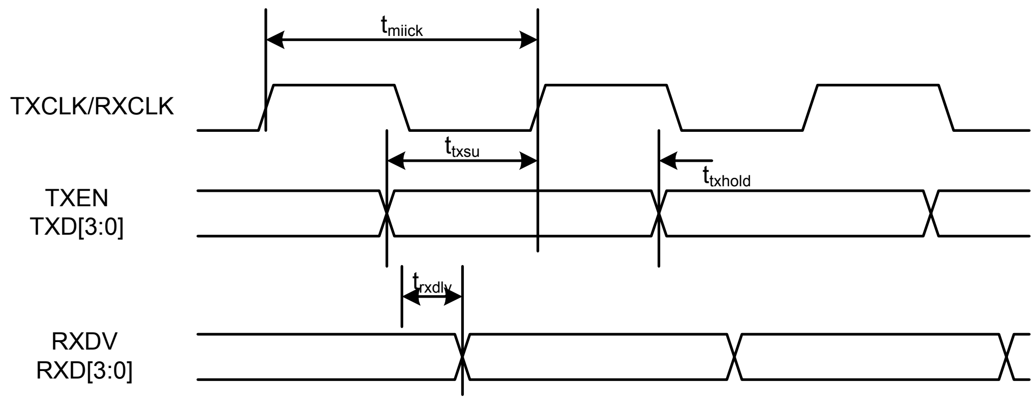


Figure 5-3. **100BASE-TX MII Input Timing Diagram**

Table 5-6. **MII Timing**

Symbol	Parameter	Min	Typ	Max	Unit
tmiick	TXCLK/RXCLK Period		40		ns
ttxsu	TXEN and TXD to TXCLK rising setup	10			ns
ttxhold	TXEN and TXD to TXCLK rising hold	10			ns
ttxdly	RXCLK falling to RXDV, and RXD Output Delay	0		8	ns

5.5.11 RMII Timing

Figure 5-3 shows the RMII timing diagram.

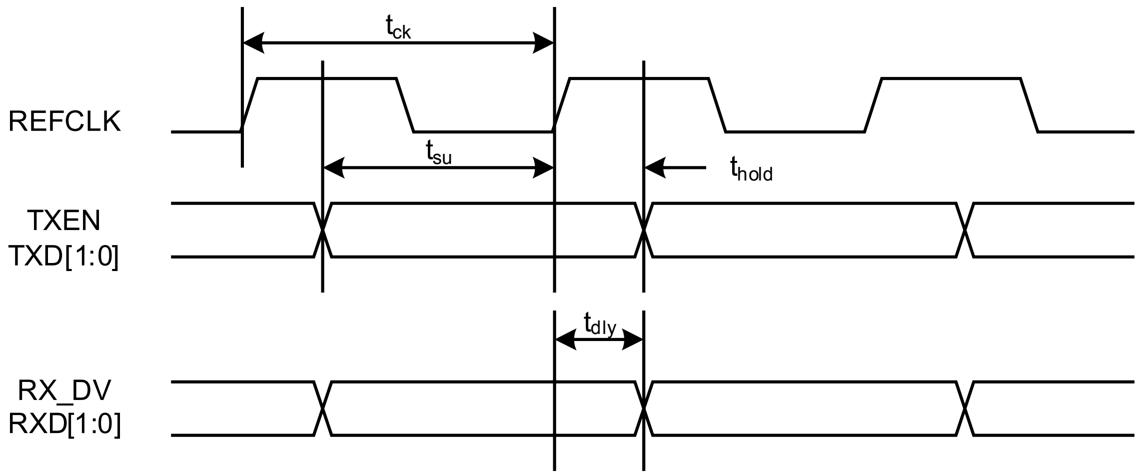


Figure 5-4. **RMII Input Timing Diagram**

Table 5-7. **RMII Timing**

Symbol	Parameter	Min	Typ	Max	Unit
Tck	REFCLK Period	—	20	—	ns
Tsu	TXEN and TXD to REFCLK rising setup time	4	—	—	ns
Thold	TXEN and TXD to REFCLK rising hold time	2	—	—	ns
Tdly	REFCLK to RX_DV, and RXD Output Delay	3	—	14	ns

5.5.12 SPI Timing

Figure 5-5 shows the SPI timing diagram.

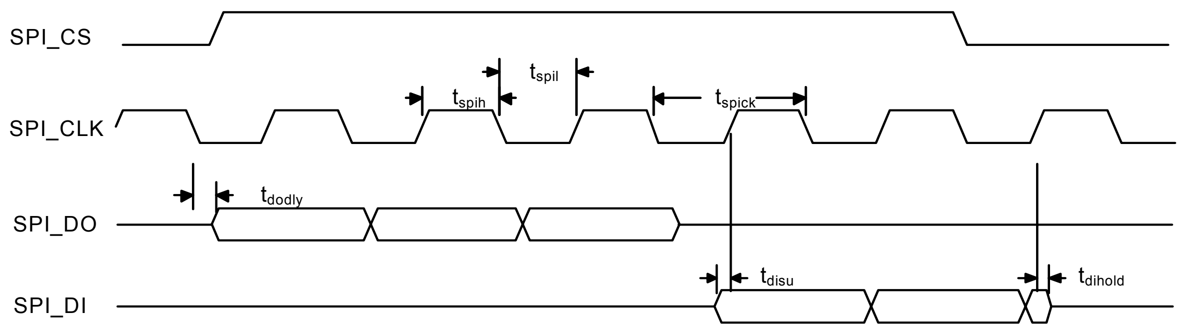


Figure 5-5. **EEPROM Interface Timing Diagram**

Table 5-8. **EEPROM Interface Timing**

Symbol	Parameter	Min	Typ	Max	Unit
tspick	SPI_CLK Period		TBD		ns
tspil	SPI_CLK Low Period	-		-	ns
tspih	SPI_CLK High Period	-		-	ns
tdisu	SPI_DI to SPI_CLK Rising Setup Time	10			ns
tdihold	SPI_DI to SPI_CLK Rising Hold Time	10			ns
tdodly	SPI_CLK Falling to SPI_DO Output Delay Time			20	ns

5.5.13 MDIO Timing

Figure 5-6 shows the MDIO timing diagram.

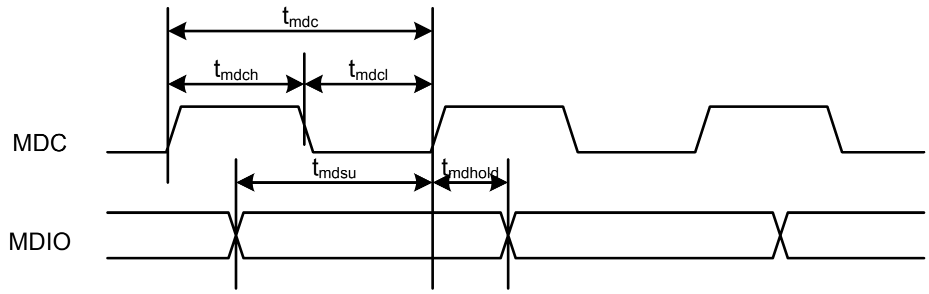


Figure 5-6. **MDIO Timing Diagram**

Table 5-9. **MDIO Timing**

Symbol	Parameter	Min	Typ	Max	Unit
tmdc	MDC Period	100			ns
tmdcl	MDC Low Period	40			ns
tmdch	MDC High Period	40			ns
tmdsu	MDIO to MDC rising setup time	2			ns
tmdhold	MDIO to MDC rising hold time	16			ns

5.6 *Typical Power Consumption Parameters*

The following conditions apply to the typical characteristics unless otherwise specified:

VDD3P3 = 3.3V

Table 5-10 shows the typical power drain on each of the on-chip power supply domains as a function of the AR8236's operating mode.

Table 5-10. **Total System Power**

3.3 V Supply (mA)	Total (mW)	Condition
49	161.7	no link
380	1254.0	All ports Linked at 100 Mbps
383	1263.9	All ports Active at 100 Mbps
69	227.7	All ports Linked at 10 Mbps
389	1283.7	All ports Linked and Active at 10 Mbps

NOTE: PHY LED x5 and 3.3V power LED x1

NOTE: POS used a 10K Ω resistor and an LED serial 510 Ω resistor

NOTE: 3.3V power input, 2.5V, 2.0V, and 1.2V supplies generated internally

NOTE: 100 meter Ethernet Cable

6. Package Dimensions

The AR8236 is packaged in a 68-pin QFN (8 x 8 mm) package. This package is available in two types — the Punch-type and the Saw-type. The Punch-type package drawings and dimensions are provided in Figure 6-1 and Table 6-1.

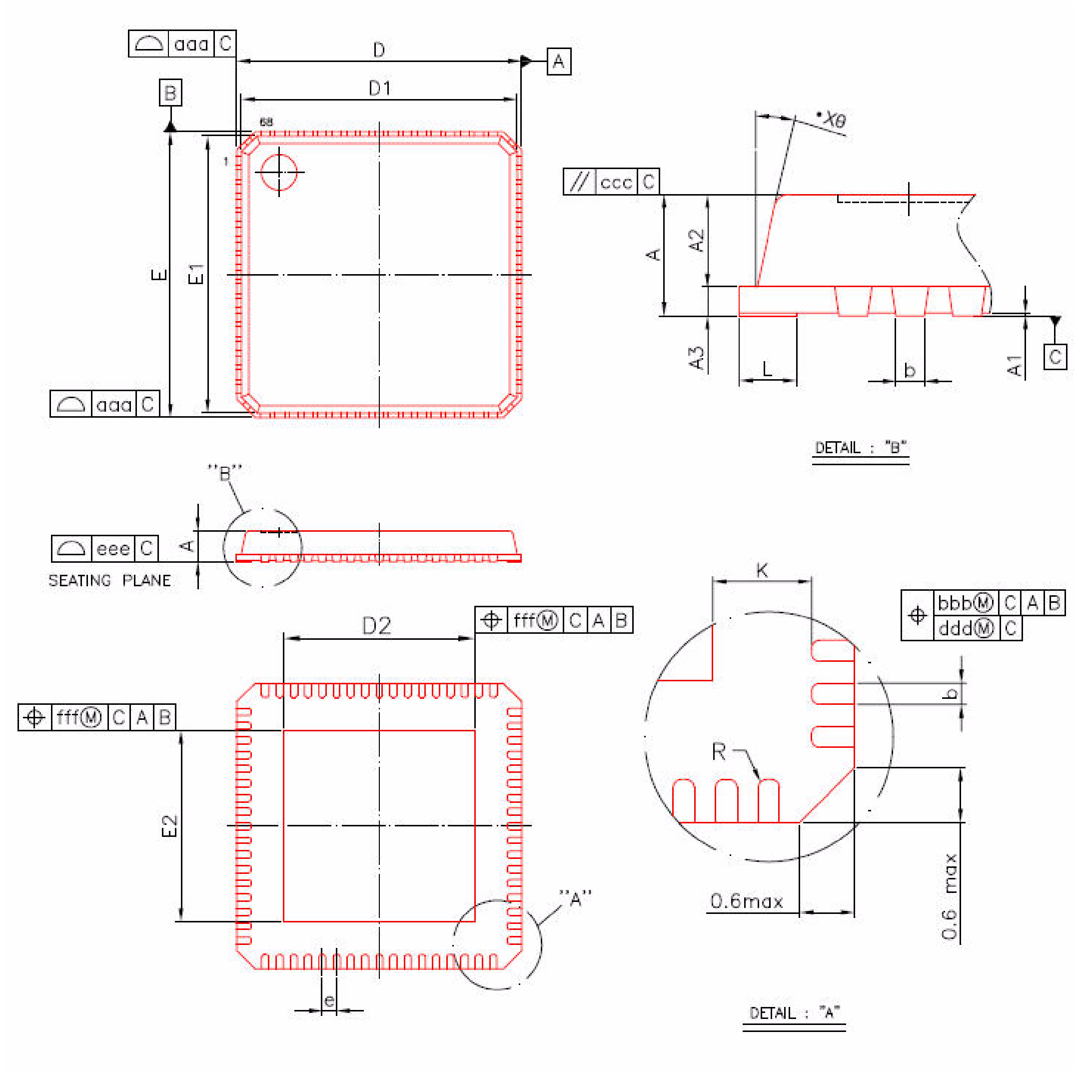


Figure 6-1. **68 pin QFN Punch Package Drawing**

Table 6-1. **Package Dimensions — Punch Type**

Dimension Label	Min	Nom	Max	Unit
A	0.80	0.85	1.00	mm
A1	0.00	0.02	0.05	mm
A2	0.60	0.65	0.80	mm
A3	0.20 REF			
b	0.15	0.20	0.25	mm
D/E	8.00 BSC			mm
D1/E1	7.75 BSC			mm
D2/E2	5.49 BSC			mm
e	0.40 BSC			mm
L	0.30	0.40	0.50	mm
θ	0	—	14	Deg
R	0.075	—	—	mm
K	0.20	—	—	mm
aaa	—	—	0.10	mm
bbb	—	—	0.07	mm
ccc	—	—	0.10	mm
ddd	—	—	0.05	mm
eee	—	—	0.08	mm
fff	—	—	0.10	mm

The AR8236 is packaged in a 68-pin QFN (8 x 8 mm) package. This package is available in two types — the Punch-type and the Saw-type. The Saw-type package drawings and dimensions are provided in Figure 6-2 and Table 6-2.

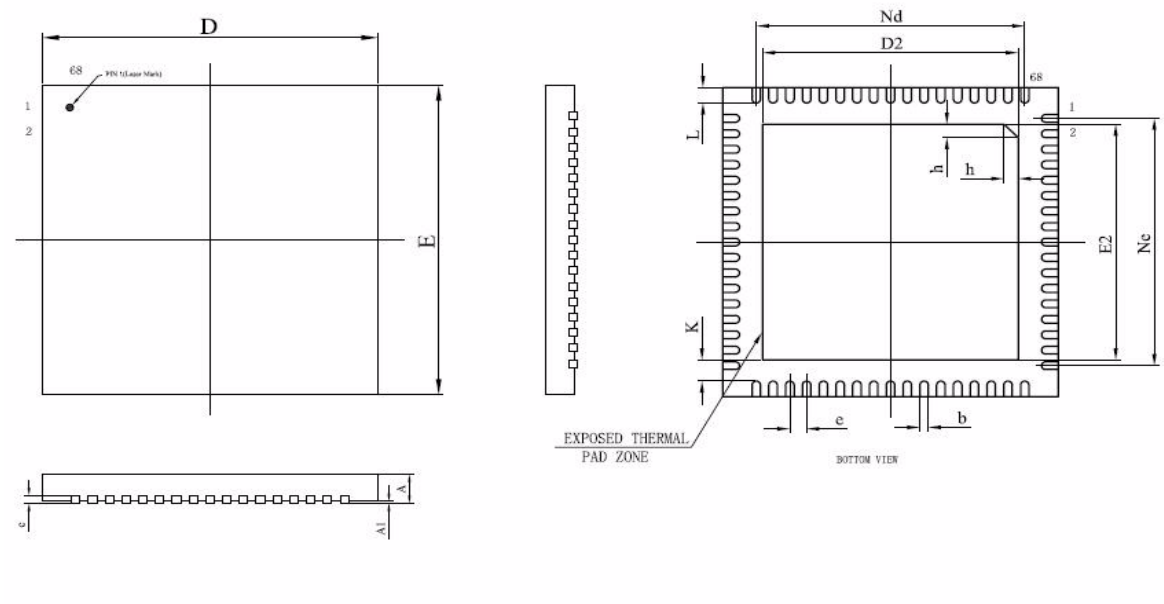


Figure 6-2. **68 pin QFN SAW Package Drawing**

Table 6-2. **Package Dimensions — SAW Type**

Dimension Label	Min	Nom	Max	Unit
A	0.70	0.75	0.80	mm
A1	—	0.02	0.05	mm
b	0.15	0.20	0.25	mm
c	0.18	0.20	0.25	mm
D	7.90	8.00	8.10	mm
D2	5.39	5.49	5.59	mm
e	0.40 BSC			
Nd	6.40 REF			
E	7.90	8.00	8.10	mm
E2	5.39	5.49	5.59	mm
Ne	6.40 REF			
L	0.30	0.40	0.45	mm
K	0.20	—	—	mm
h	0.30	0.35	0.40	mm

7. Ordering Information

The order number AR8236–1L1E specifies an Engineering, lead-free version of the AR8236.

The order number AR8236–AL1A specifies a mass production, lead-free version of the AR8236.

Document Number: 981-00077-001 MKG-0675 Rev. 1

Atheros Communications, Incorporated
5480 Great America Parkway
Santa Clara, CA 95054
t: 408/773-5200
f: 408/773-9940
www.atheros.com

Ethernet. Atheros Engineered.