MITSUBISHI MICROCOMPUTERS

M5L8243P

6249828 MITSUBISHI(MICMPTR/MIPRC) 91D 11663 D

INPUT/OUTPUT EXPANDER

T-52-33-03

DESCRIPTION

The M5L8243P is an input/output expander fabricated using N-channel silicon-gate EDMOS technology. This device is designed specifically to provide a low-cost means of I/O expansion for the Series MELPS 8-48 single-chip microcomputers and Series MELPS 8-41 slave microcomputers.

FEATURES

- 16 input/output pins (I_{OL} = 5.0mA(max.))
- Simple interface to Series MELPS 8-48, Series MELPS 8-41
- Single 5V power supply
- Low power dissipation ..... 50mW(typ.)
- Interchangeable with I8243 in pin configuration and electrical characteristics

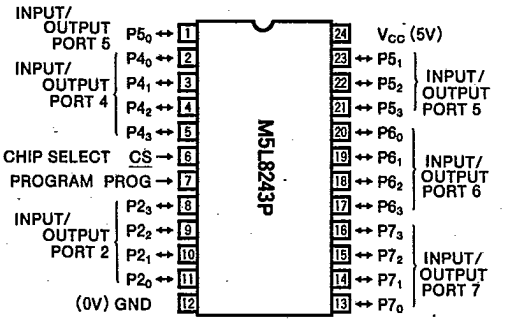
APPLICATION

I/O expansion for the Series MELPS 8-48 single-chip microcomputers and Series MELPS 8-41 slave microcomputers.

FUNCTION

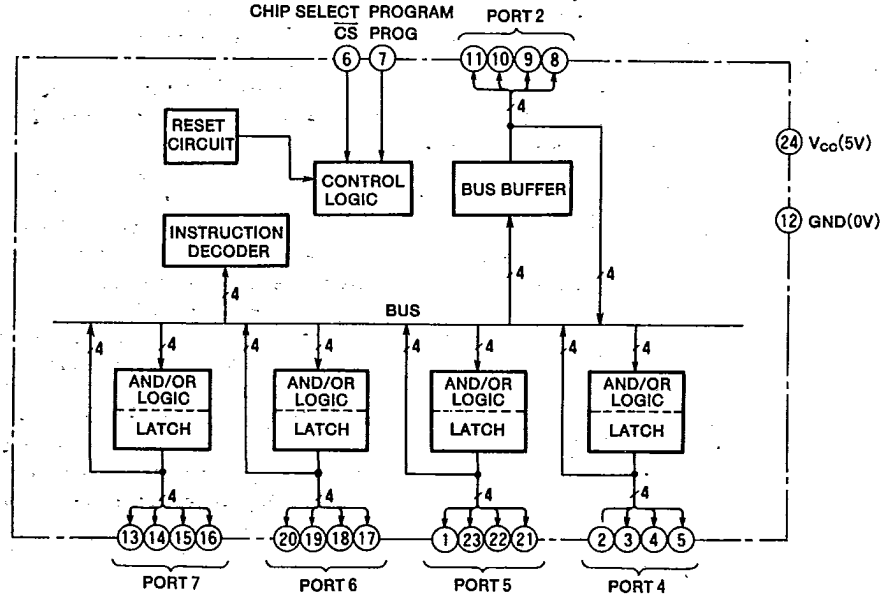
The M5L8243P is designed to provide a low-cost means of I/O expansion for the Series MELPS 8-41 and the Series MELPS 8-48. The M5L8243P consists of four 4-bit bidirectional static I/O ports and one 4-bit port which serves as an interface to the Series MELPS 8-41 and Series MELPS 8-48. Thus multiple M5L8243Ps can be added to a single master. Using the original instruction set of the master, the M5L8243P serves as the in resident I/O facility. Its I/O ports are accessed by instructions MOVD, ANLD and ORLD.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4

BLOCK DIAGRAM



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PIN DESCRIPTION

Symbol	Name	Input or output	Function
$\overline{CS}$	Chip select	In	Chip select input. A high on $\overline{CS}$ causes PROG input to be regarded high inside the M5L8243P, then this inhibits any change of output or internal status.
PROG	Program	In	A high-to-low transition on PROG signifies that address (PORT 4-7) and control are available on PORT 2, and a low-to-high transition signifies that the designated data is available on the disignated port through PORT 2. The designation is shown in Table 1.
$P2_0 \sim P2_3$	Input/output port 2	In/out	The 4-bit bidirectional port contains the address and control bits shown in Table 1 on a high-to-low transition of PROG. During a low-to-high transition it contains the input (output) data on this port.
$P4_0 \sim P4_3$ $P5_0 \sim P5_3$ $P6_0 \sim P6_3$ $P7_0 \sim P7_3$	Input/output port 4 Input/output port 5 Input/output port 6 Input/output port 7	In/out	The 4-bit bidirectional I/O port. May be programmed to be input, low-impedance latched output or a three-state. This port is automatically set output mode when it is written. ANLed or ORLed then continues its mode until next read operation. After reset on a read operation, this port is in high-impedance and input mode.

OPERATION

The M5L8243P is an input/output expander designed specifically for the Series MELPS 8-41 and Series MELPS 8-48. The Series MELPS 8-41 and Series MELPS 8-48 already have instructions and PROG pin to communicate with the M5L8243P.

An example of the M5L8243P and the Series MELPS 8-41 or Series MELPS 8-48 is shown in Fig. 1. The following description of the M5L8243P basic operation is made according to Fig. 1.

Upon initial application of power supply to the device, and then about 500μs after, resident bias circuits become stable and each device is ready to operate. And each port of the M5L8243P is set input mode (high-impedance) by means of a resident power-on initialization circuit.

When the microcomputer begins to execute a transfer instruction

MOVD A, PI i = 4, 5, 6, 7

which means the value on the port Pi is transferred to the accumulator, then the signals are sent out on the pins PROG and $P2_0 \sim P2_3$ as shown in Timing Diagram.

On the high-to-low transition of the pin PROG, the M5L8243P latches the instructions (ex. 0000) into itself from pins $P2_0 \sim P2_3$ and transfers them to the instruction register (① in Timing Diagram). During the low-level of PROG, the M5L8243P continuously outputs the contents of the specified input (output) port (in this case port P_4) to pins $P2_0 \sim P2_3$ (② in Timing Diagram). The microcomputer, at an appropriate time, latches the level of pins $P2_0 \sim P2_3$ and resumes high-level of PROG.

The next example is the case in which the microcomputer executes

MOVD PI, A i = 4, 5, 6, 7

the transfer (output) instruction.

In this case, as in the previous case, on the high-to-low transition of the pin PROG, the M5L8243P latches the instructions (ex. 0110) into itself from pins $P2_0 \sim P2_3$ and transfers them to the instruction register (① in Timing Diagram). After this, the microcomputer sends out high to the pin PROG, transferring the data to pin $P2_0 \sim P2_3$ which is an output data to input/output port. Then the M5L8243P transfers the data of pins $P2_0 \sim P2_3$ to the port latch of the designated input/output port (in this case P_6). In a few seconds after a low-to-high transition on the PROG, the designated port (P_6) becomes in an output mode and the data of the port latch are transferred to the port pins (③ in Timing Diagram).

When instructions

ANLD PI, A
ORLD PI, A i = 4, 5, 6, 7

are executed, the microcomputer generally operates as same function as MOVD PI, A.

It only differs in that the data of port latch after ④ in the Timing Diagram is ANDed or ORed with the data of port latch before ④ and the data of pins $P2_0 \sim P2_3$.

When instructions

MOVD PI, A
ANLD PI, A
ORLD PI, A i = 4, 5, 6, 7

are executed toward the port in an output mode, the outputs are generated on the port as soon as low-to-high transition on the PROG occurs.

When the mode of the output port is going to be changed during the execution and the instruction

MOVD A, PI i = 4, 5, 6, 7

is executed, it is preferable to execute one dummy instruction. Because it takes a little time to turn the designated port into a high-impedance state after high-to-low transition on the PROG, the result may be that the first instruction is not read correctly.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_I	Input voltage		−0.5~7	V
V_O	Output voltage		−0.5~7	V
P_d	Maximum power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating free-air temperature range		−20~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −20~75℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage	−0.5		0.8	V

ELECTRICAL CHARACTERISTICS (T_a = −20~75℃, V_{CC} = 5 V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OL1}	Low-level output voltage, ports 4~7	I_{OL} = 5mA			0.45	V
V_{OL2}	Low-level output voltage, port 7	I_{OL} = 20 mA			1	V
V_{OL3}	Low-level output voltage, port 2	I_{OL} = 0.6mA			0.45	V
V_{OH1}	High-level output voltage, ports 4~7	I_{OH} = −240μA	2.4			V
V_{OH2}	High-level output voltage, port 2	I_{OH} = −100μA	2.4			V
I_{I1}	Input leakage current, ports 4~7	0V ≦ V_{in} ≦ V_{CC}	−10		20	μA
I_{I2}	Input leakage current, port 2, CS, PROG	0V ≦ V_{in} ≦ V_{CC}	−10		10	μA
I_{CC}	Supply current from V_{CC}			10	20	mA
I_{OL}	Sum of all I_{OL} from 16 outputs	I_{OL} = 5mA (V_{OL} = 0.45V) Each pin			80	mA

Table 1 Instruction and address codes

Instruction code	$P2_3$	$P2_2$	Address code	$P2_1$	$P2_0$
Read	0	0	port 4	0	0
Write	0	1	port 5	0	1
ORLD	1	0	port 6	1	0
ANLD	1	1	port 7	1	1

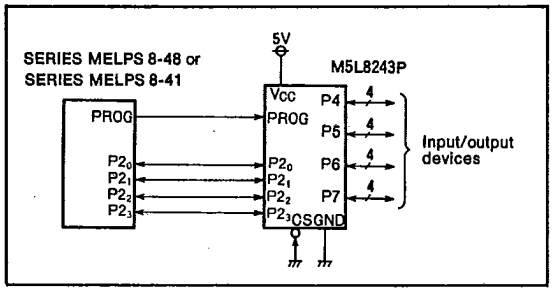

Fig.1 Basic connection

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TIMING REQUIREMENTS (T_a = −20~75℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{SU(INST-PR)}$	Instruction code setup time before PROG	t_A	80pF Load	100			ns
$t_{h(PR-INST)}$	Instruction code hold time after PROG	t_B	20pF Load	60			ns
$t_{SU(DQ-PR)}$	Data setup time before PROG	t_C	80pF Load	200			ns
$t_{h(PR-DQ)}$	Data hold time after PROG	t_D	20pF Load	20			ns
$t_{W(PR)}$	PROG pulse width	t_K		700			ns
$t_{SU(CS-PR)}$	Chip-select setup time before PROG	t_{CS}		50			ns
$t_{h(PR-CS)}$	Chip-select hold time after PROG	t_{CS}		50			ns
$t_{SU(PORT-PR)}$	Port setup time before PROG	t_{IP}		100			ns
$t_{h(PR-PORT)}$	Port hold time after PROG	t_{IP}		100			ns

SWITCHING CHARACTERISTICS (T_a = −20~75℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(PR)}$	Data access time after PROG	t_{ACC}	80pF Load	0		650	ns
$t_{dv(PR)}$	Data valid time after PROG	t_H	20pF Load	0		150	ns
$t_{PHL(PR)}$ $t_{PLH(PR)}$	Output valid time after PROG	t_{PO}	100pF Load			700	ns
$t_{PZX(PR)}$ $t_{PXZ(PR)}$	Input/output switching time	—				800	ns

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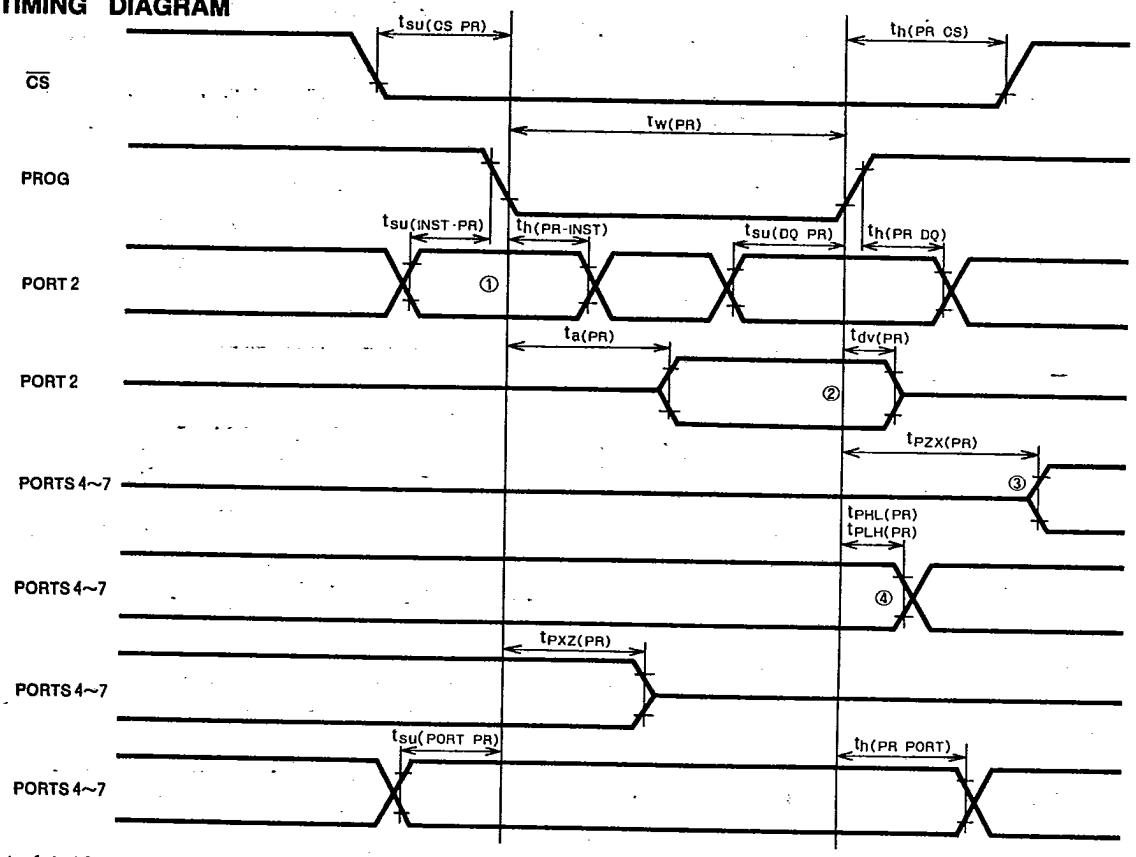
TIMING DIAGRAM



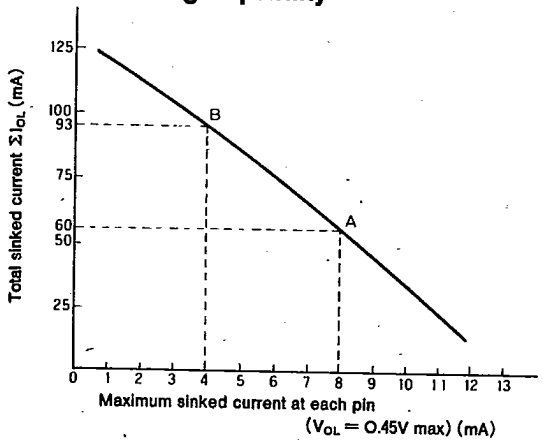
Note 1 : AC test conditions

Input pulse level ..... 0.45~2.4V
Input pulse rise time tr (10%~90%) 20ns
Input pulse fall time tf (10%~90%) 20ns

Reference voltage for switching characteristic measurement.

Output V_{OH} 2V
V_{OL} 0.8V

Current Sinking Capability



Each of the 16 I/O lines of the M5L8243P is capable of sinking 5mA simultaneously (V_{OL} = 0.45V max). However, the drive capacity of each line depends upon whether all lines are sinking current simultaneously and on the degree of loading. This is illustrated in the curve shown.

Example

Assuming that the remaining pins are not loaded, how many pins would be able to accommodate 20LSTTL loads (0.4mA) ?

I_{OL} = 0.4mA × 20 = 8mA (sink current for each pin)

ΣI_{OL} = 60mA from curve (POINT A)
(total sinking current)

Number of pins = 60mA ÷ 8mA = 7.5>7

For this case, each of the 7 lines could sink 8mA for a total of 56mA. Since 4mA reserve sinking capability exists, 9 of the I/O lines of the M5L8243P can be divided arbitrarily.

Example

To use 20mA sinking capability at port 7, find the effects on the sinking capabilities of the other I/O lines.

Assume the M5L8243P is driving loads as shown below.

3 lines: -20mA ($V_{OL} = 1.0$V max, port 7 only)

4 lines: -4mA ($V_{OL} = 0.45$V max)

9 lines: -1.6mA ($V_{OL} = 0.45$V max)

Is this within the allowable limit ?

$\Sigma I_{OL} = (20\text{mA} \times 3) + (4\text{mA} \times 4) + (1.6\text{mA} \times 9) = 90.4\text{mA}$

From the curve we see that with respect to $I_{OL} = 4$mA, I_{OL} is 93mA (Point B) and that the above load of 90.4mA is within the limit of 93mA.

Note: The sinking current of ports 4 ~ 7 must not exceed 30mA regardless of the value of V_{OL}.

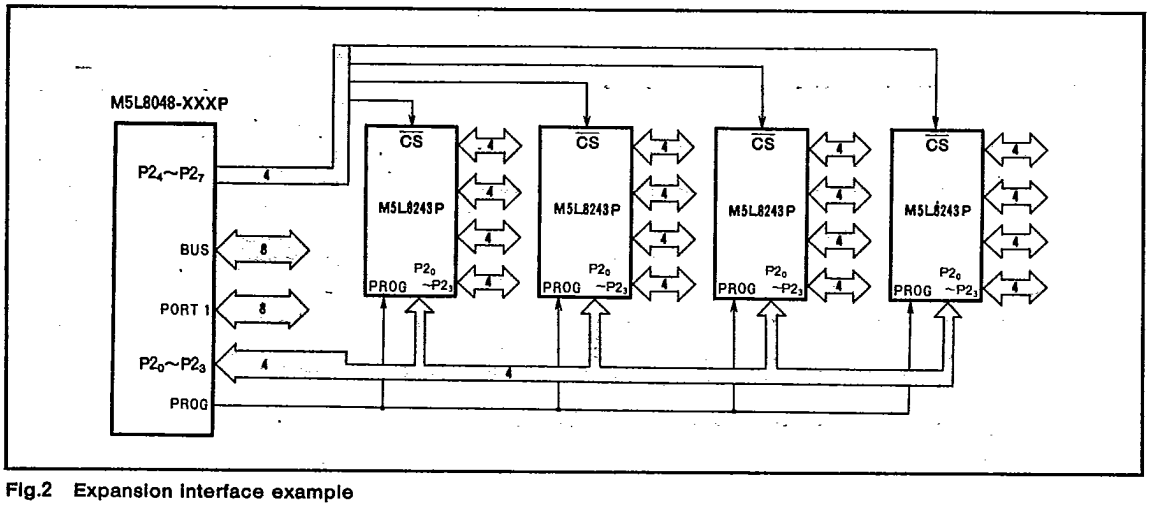


Fig.2 Expansion interface example