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# HM628128B Series

131,072-word  $\times$  8-bit High speed CMOS Static RAM

# HITACHI

ADE-203-243B (Z)  
Rev. 2.0  
Mar. 20, 1995

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## Description

The Hitachi HM628128B is a CMOS static RAM organized 131,072-word  $\times$  8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8  $\mu$ m Hi-CMOS shrink process technology. It offers low power standby power dissipation, therefore, it is suitable for battery backup systems. The device, packaged in a 525 mil SOP or a 8 mm  $\times$  20 mm TSOP or a 600 mil plastic DIP is available.

## Features

- High speed
  - Fast access time: 70/85ns (max)
- Low power
  - Standby: 10  $\mu$ W (typ) (L/L-SL version)
  - Operation: 50 mW/MHz (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Capability of battery backup operation (L/L-SL version)
  - 2 chip selection for battery backup

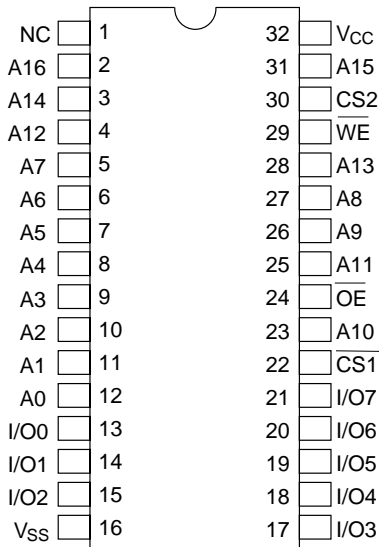
# HM628128B Series

## Ordering Information

Type No.	Access Time	Data Retention Current	Package
HM628128BLP-7	70 ns	50 $\mu$ A	600-mil 32-pin plastic DIP (DP-32)
HM628128BLP-8	85 ns	50 $\mu$ A	
HM628128BLP-7SL	70 ns	15 $\mu$ A	
HM628128BLP-8SL	85 ns	15 $\mu$ A	
HM628128BLFP-7	70 ns	50 $\mu$ A	525-mil 32-pin plastic SOP (FP-32D)
HM628128BLFP-8	85 ns	50 $\mu$ A	
HM628128BLFP-7SL	70 ns	15 $\mu$ A	
HM628128BLFP-8SL	85 ns	15 $\mu$ A	
HM628128BLT-7	70 ns	50 $\mu$ A	Normal-bend type 32-pin plastic 8 mm $\times$ 20 mm TSOP (TFP-32D)
HM628128BLT-8	85 ns	50 $\mu$ A	
HM628128BLT-7SL	70 ns	15 $\mu$ A	
HM628128BLT-8SL	85 ns	15 $\mu$ A	
HM628128BLR-7	70 ns	50 $\mu$ A	Reverse-bend type 32-pin plastic 8 mm $\times$ 20 mm TSOP (TFP-32DR)
HM628128BLR-8	85 ns	50 $\mu$ A	
HM628128BLR-7SL	70 ns	15 $\mu$ A	
HM628128BLR-8SL	85 ns	15 $\mu$ A	

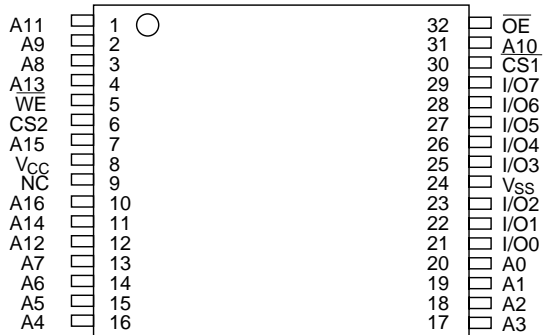
## Pin Arrangement

HM628128BP/BFP Series



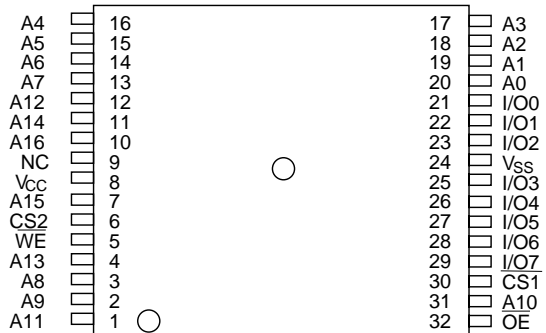
(Top View)

HM628128BT Series (Normal Type TSOP)



(Top View)

HM628128BR Series (Reverse Type TSOP)

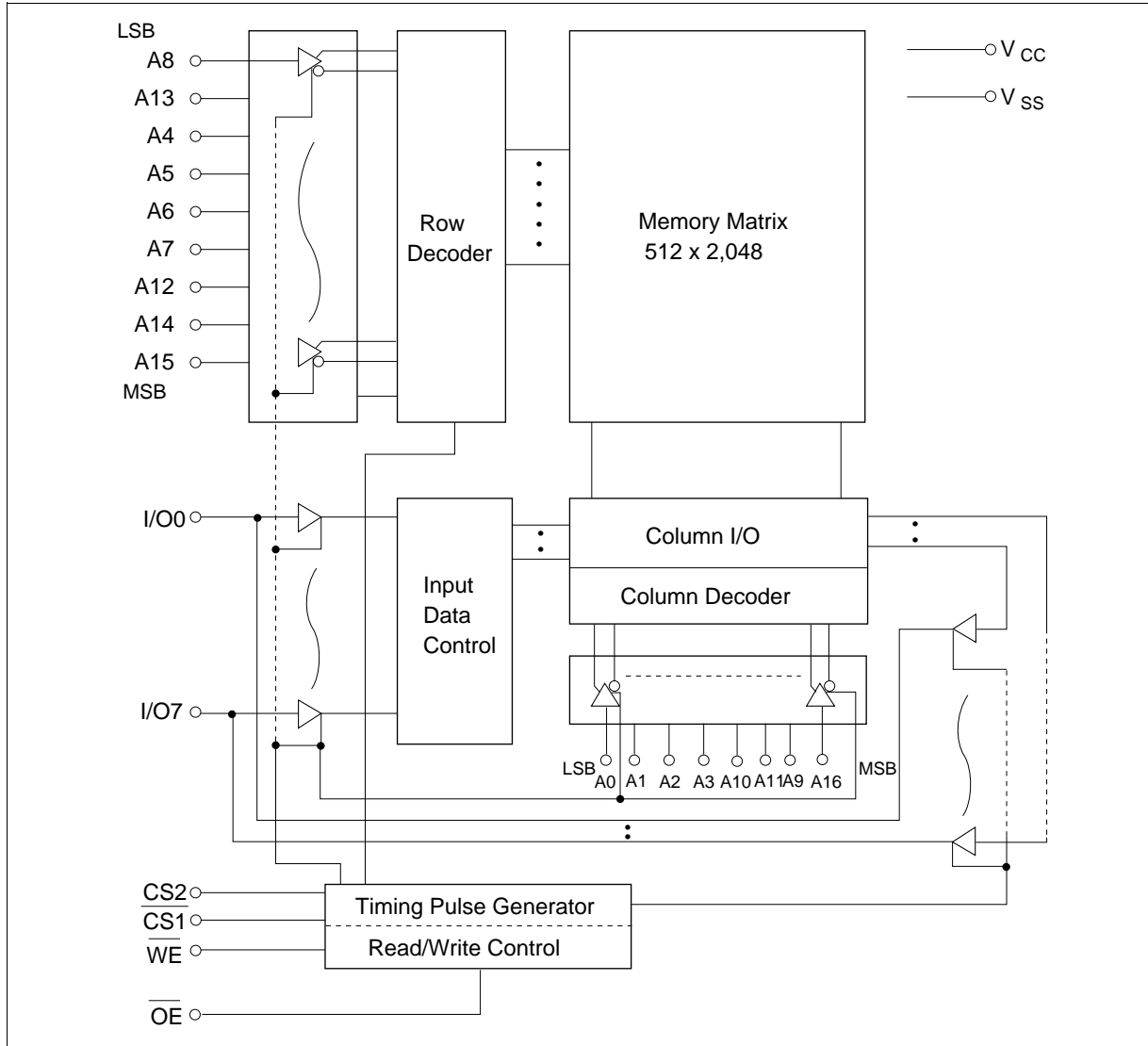


(Top View)

## Pin Description

Pin Name	Function
A0 - A16	Address
I/O0 - I/O7	Input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
NC	No connection
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

## Block Diagram



**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +7.0	V
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 <sup>1</sup> to $V_{CC} + 0.3$ <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-10 to +85	°C

Notes: 1. -3.0 V for pulse half-width  $\leq 30$  ns

2. Maximum voltage is 7.0 V.

**Function Table**

$\overline{WE}$	$\overline{CS1}$	$CS2$	$\overline{OE}$	Mode	$V_{CC}$ Current	I/O Pin	Ref. Cycle
X	H	X	X	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
X	X	L	X	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	H	Output disable	$I_{CC}$	High-Z	—
H	L	H	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	H	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: 1. X: H or L

**Recommended DC Operating Conditions ( $T_a = 0$  to +70°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input high voltage ( logic 1 )	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V
Input low voltage ( logic 0 )	$V_{IL}$	-0.3 <sup>1</sup>	—	0.8	V

Note: 1. -3.0 V for pulse half-width  $\leq 30$ ns

# HM628128B Series

## DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5V ± 10 %, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Typ <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	—	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	—	1	μA	$\overline{CS1} = V_{IH}$ or CS2 = V <sub>IL</sub> or OE = V <sub>IH</sub> or WE = V <sub>IL</sub> , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating power supply current : DC	I <sub>CC</sub>	—	15	25	mA	$\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0mA
Operating power supply current	I <sub>CC1</sub>	—	35	70	mA	Min.cycle, duty = 100 %, $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA
	I <sub>CC2</sub>	—	10	20	mA	Cycle time = 1 μs, duty = 100 % I <sub>I/O</sub> = 0 mA, $\overline{CS1} \leq 0.2$ V CS2 ≥ V <sub>CC</sub> - 0.2 V, Others = V <sub>IH</sub> /V <sub>IL</sub> V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IL</sub> ≤ 0.2 V
Standby V <sub>CC</sub> current : DC	I <sub>SB</sub>	—	1	2	mA	CS2 = V <sub>IL</sub> or CS2 = V <sub>IH</sub> , $\overline{CS1} = V_{IH}$
Standby V <sub>CC</sub> current (1): DC	I <sub>SB1</sub>	—	2 <sup>2</sup>	100 <sup>2</sup>	μA	0V ≤ V <sub>in</sub> ≤ V <sub>CC</sub> , (1) 0 V ≤ CS2 ≤ 0.2V or (2) CS2 ≥ V <sub>CC</sub> - 0.2V , CS1 ≥ V <sub>CC</sub> - 0.2V
		—	2 <sup>3</sup>	50 <sup>3</sup>	μA	
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1.0 mA

- Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.  
 2. For L-version  
 3. For L-SL version

## Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C <sub>in</sub> <sup>1</sup>	—	—	8	pF	V <sub>in</sub> = 0 V
Input/output capacitance	C <sub>I/O</sub> <sup>1</sup>	—	—	10	pF	V <sub>I/O</sub> = 0 V

- Note: 1. This parameter is sampled and not 100 % tested.

**AC Characteristics** (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ±10%, unless otherwise noted.)

**Test Conditions**

- Input pulse levels : 0.8 V to 2.4 V
- Input rise and fall time : 5 ns
- Input and output timing reference levels : 1.5 V
- Output load : 1 TTL Gate and C<sub>L</sub> ( 100 pF ) ( Including scope and jig )

**Read Cycle**

Parameter	Symbol	HM628128B				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
Read cycle time	t <sub>RC</sub>	70	—	85	—	ns	
Address access time	t <sub>AA</sub>	—	70	—	85	ns	
Chip selection to output valid	t <sub>CO1</sub>	—	70	—	85	ns	
	t <sub>CO2</sub>	—	70	—	85	ns	
Output enable to output valid	t <sub>OE</sub>	—	35	—	45	ns	
Chip selection to output in low-Z	t <sub>LZ1</sub>	10	—	10	—	ns	2, 3
	t <sub>LZ2</sub>	10	—	10	—	ns	2, 3
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t <sub>HZ1</sub>	0	25	0	30	ns	1, 2, 3
	t <sub>HZ2</sub>	0	25	0	30	ns	1, 2, 3
Output disable to output in high-Z	t <sub>OHZ</sub>	0	25	0	30	ns	1, 2, 3
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns	

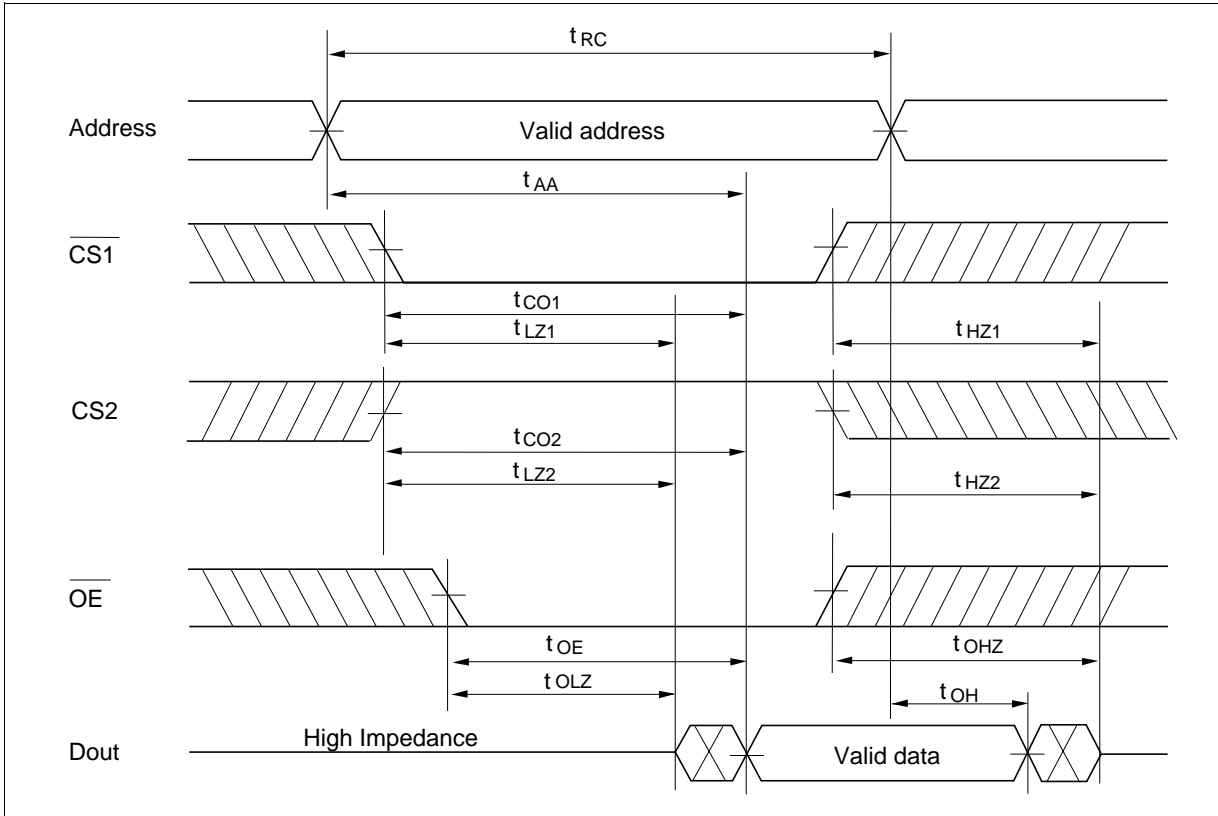
Notes: 1. t<sub>HZ</sub> and t<sub>OHZ</sub> are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. At any given temperature and voltage condition, t<sub>HZ</sub> max is less than t<sub>LZ</sub> min both for a given device to device.

3. This parameter is sampled and not 100% tested.

# HM628128B Series

## Read Cycle Timing ( $\overline{WE} = V_{IH}$ )



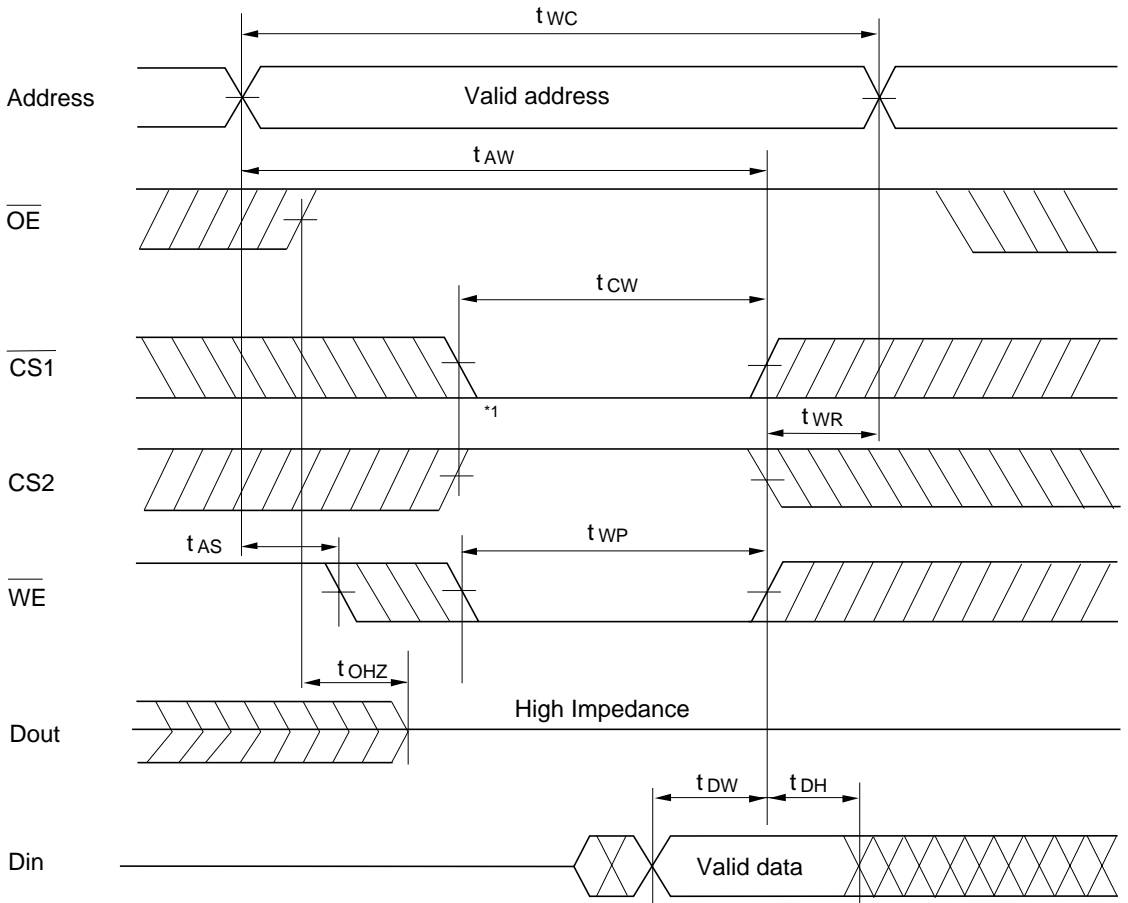


Write Cycle

Parameter	Symbol	HM628128B				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	70	—	85	—	ns	
Chip selection to end of write	$t_{CW}$	60	—	75	—	ns	2
Address setup time	$t_{AS}$	0	—	0	—	ns	3
Address valid to end of write	$t_{AW}$	60	—	75	—	ns	
Write pulse width	$t_{WP}$	50	—	55	—	ns	1, 7
Write recovery time	$t_{WR}$	0	—	0	—	ns	4
Write to output in high-Z	$t_{WHZ}$	0	25	0	30	ns	5, 6
Data to write time overlap	$t_{DW}$	30	—	35	—	ns	
Write hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	ns	6
Output disable to output in High-Z	$t_{OHZ}$	0	25	0	25	ns	5

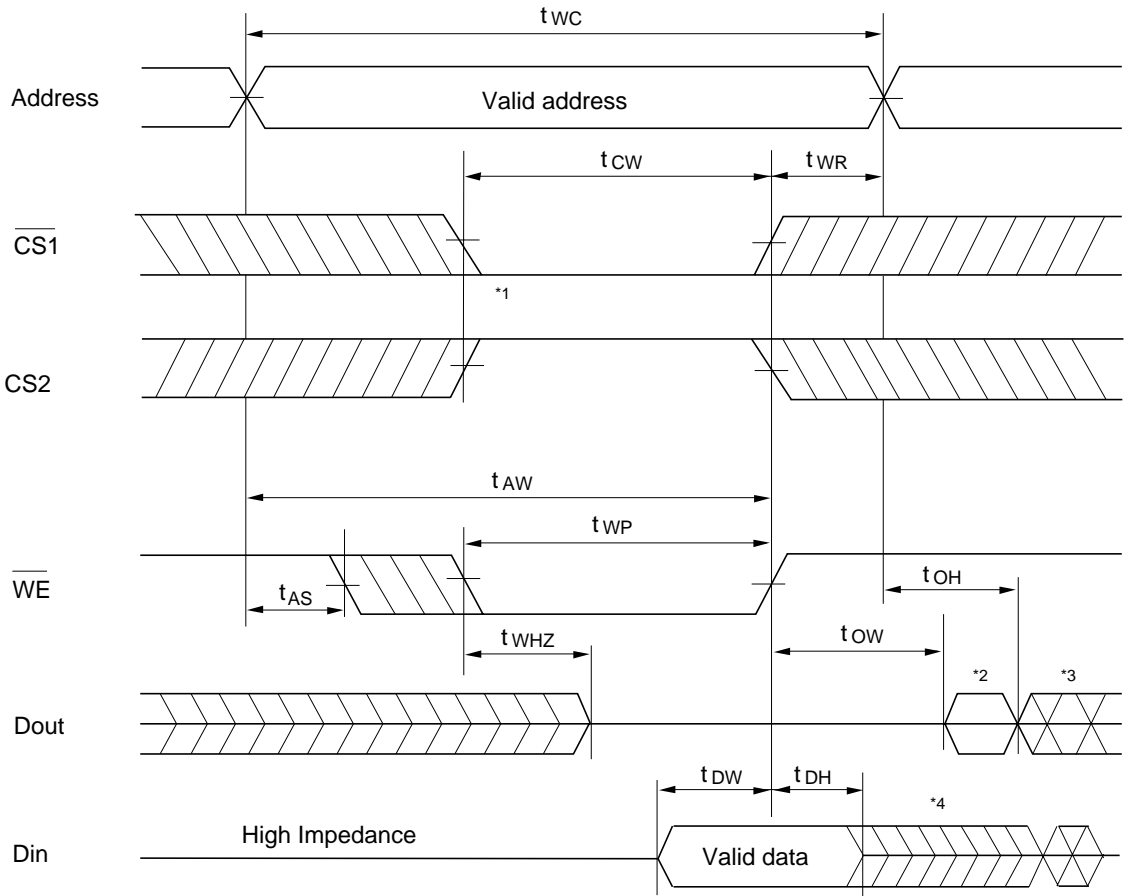
- Notes:
1. A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2, and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high, and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low, and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  2.  $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
  3.  $t_{AS}$  is measured from the address valid to the beginning of write.
  4.  $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low to the end of write cycle.
  5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
  6. This parameter is sampled and not 100% tested.
  7. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention,  $t_{WP} \geq t_{DW} (\text{min}) + t_{WHZ} (\text{mix})$ .

## Write Cycle Timing (1) ( $\overline{\text{OE}}$ Clock)



Note: 1. If the  $\overline{\text{CS1}}$  goes low or  $\overline{\text{CS2}}$  goes high simultaneously with  $\overline{\text{WE}}$  going low or after the  $\overline{\text{WE}}$  going low, the outputs remain in a high impedance state.

Write Cycle Timing (2) ( $\overline{OE}$  low fix)



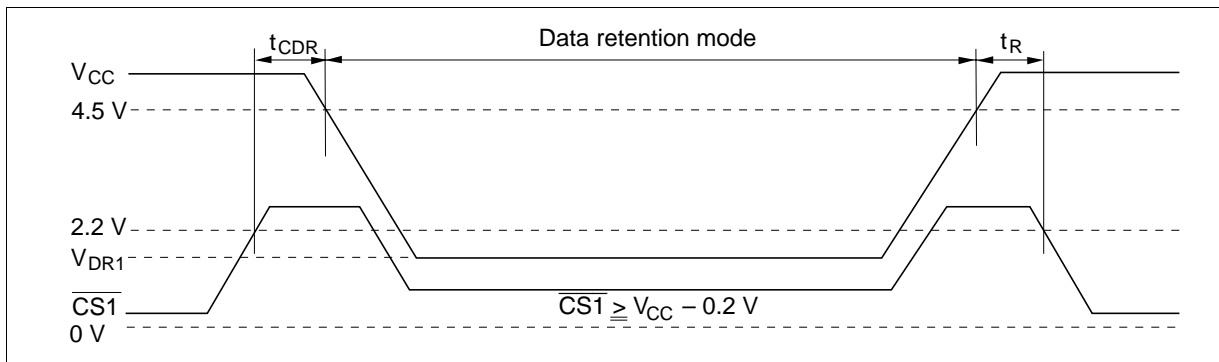
- Notes: 1. If the  $\overline{CS1}$  goes low or CS2 goes high simultaneously with  $\overline{WE}$  going low or after the  $\overline{WE}$  going low, the outputs remain in a high impedance state.  
 2. Dout is the same phase of the latest written data in this write cycle.  
 3. Dout is the read date of next address.  
 4. If  $\overline{CS1}$  is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

## Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ )

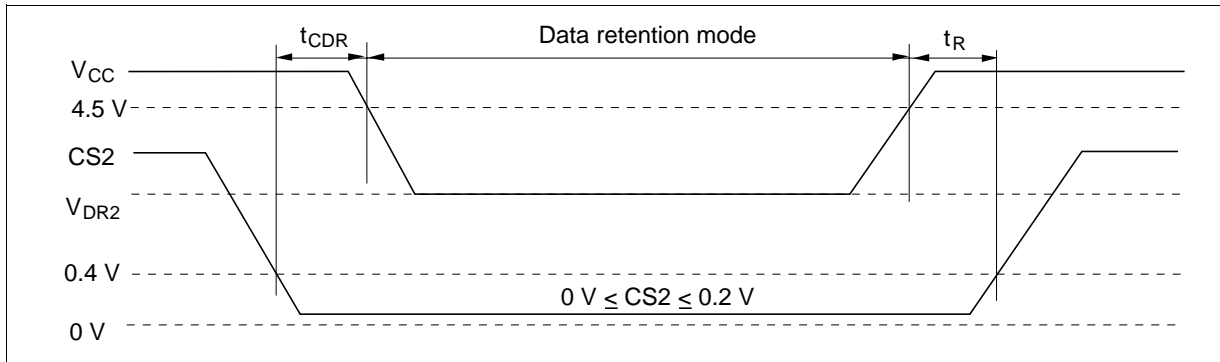
Parameter	Symbol	Min	Typ <sup>3</sup>	Max	Unit	Test conditions <sup>4</sup>
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$0\text{ V} \leq V_{in} \leq V_{CC}$ , (1) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$ or (2) $CS2 \geq V_{CC} - 0.2\text{ V}$ , $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$
Data retention current	$I_{CCDR}$ (L)	—	1	$50^{*1}$	$\mu\text{A}$	$V_{CC} = 3\text{ V}$ , $0\text{ V} \leq V_{in} \leq 3\text{ V}$ (1) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$ or (2) $CS2 \geq V_{CC} - 0.2\text{ V}$ , $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$
	(L-SL)	—	1	$15^{*2}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	—	ms	

- Notes: 1. This characteristics is guaranteed only for L-version, 20  $\mu\text{A}$  max at  $T_a = 0$  to  $40^\circ\text{C}$ .  
 2. This characteristics is guaranteed only for L-SL version, 3  $\mu\text{A}$  max at  $T_a = 0$  to  $40^\circ\text{C}$ .  
 3. Typical values are at  $V_{CC} = 3.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.  
 4. CS2 controls address buffer,  $\overline{WE}$  buffer,  $\overline{CS1}$  buffer,  $\overline{OE}$  buffer, and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CS1}$ , I/O) can be in the high impedance state. If  $\overline{CS1}$  controls data retention mode, CS2 must be  $CS2 \geq V_{SS} - 0.2\text{ V}$  or  $0\text{ V} \leq CS2 \leq 0.2\text{ V}$ . The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.

### Low $V_{CC}$ Data Retention Waveform (1) ( $\overline{CS1}$ Controlled)



Low  $V_{CC}$  Data Retention Waveform (2) (CS2 Controlled)

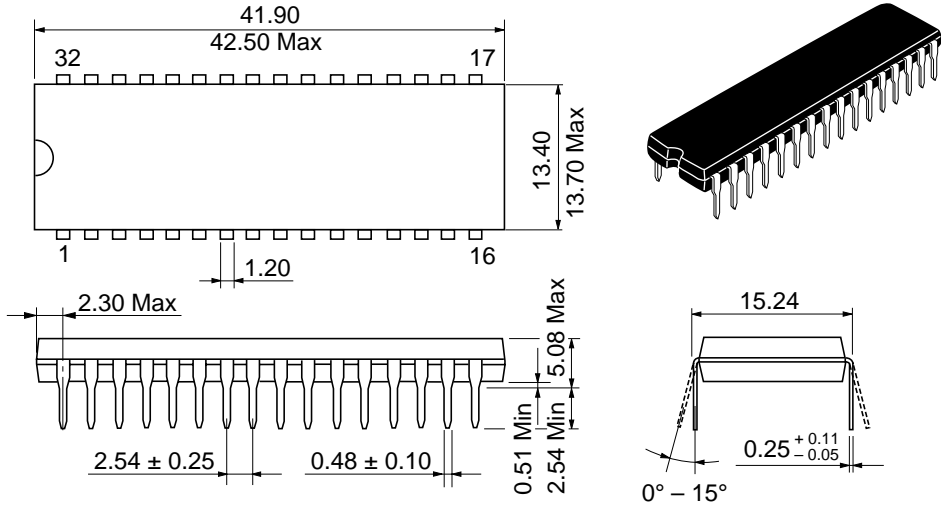


# HM628128B Series

## Package Dimensions

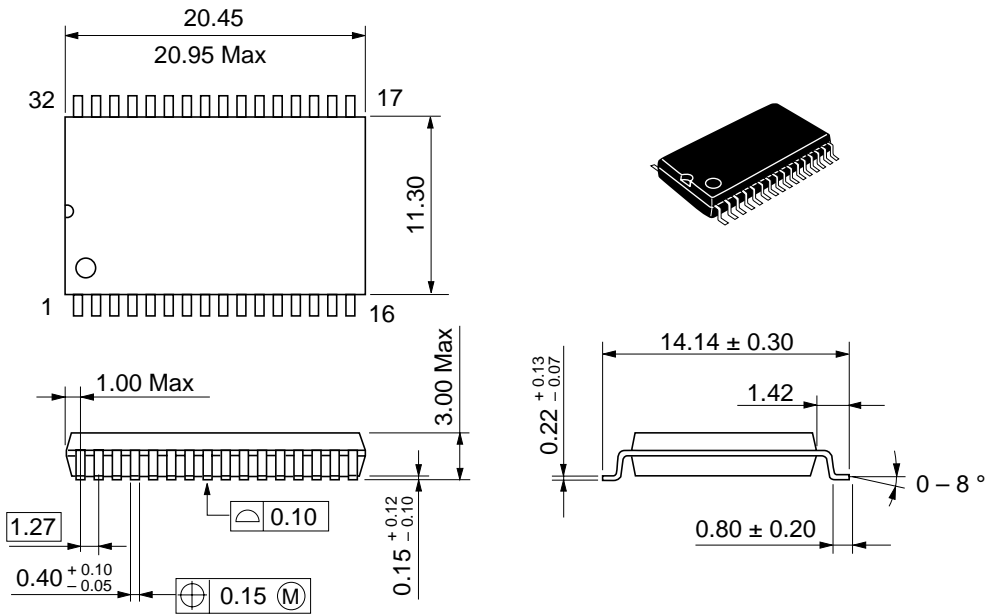
HM628128BLP Series (DP-32)

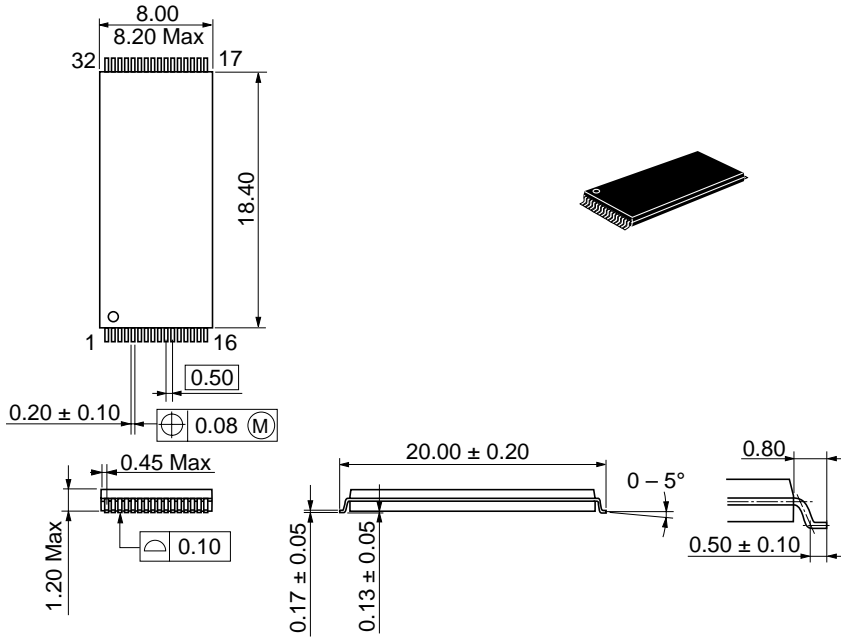
Unit: mm



HM628128BLFP Series (FP-32D)

Unit: mm





# HM628128B Series

HM628128BLR Series (TFP-32DR)

Unit: mm

