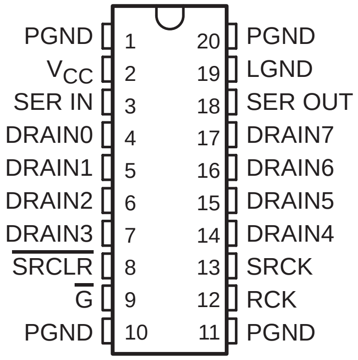
- **Low $r_{DS(on)}$ . . . 1.3 Ω Typical**
- **Avalanche Energy . . . 75 mJ**
- **Eight Power DMOS Transistor Outputs of 250-mA Continuous Current**
- **1.5-A Pulsed Current Per Output**
- **Output Clamp Voltage at 45 V**
- **Devices Are Cascadable**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)

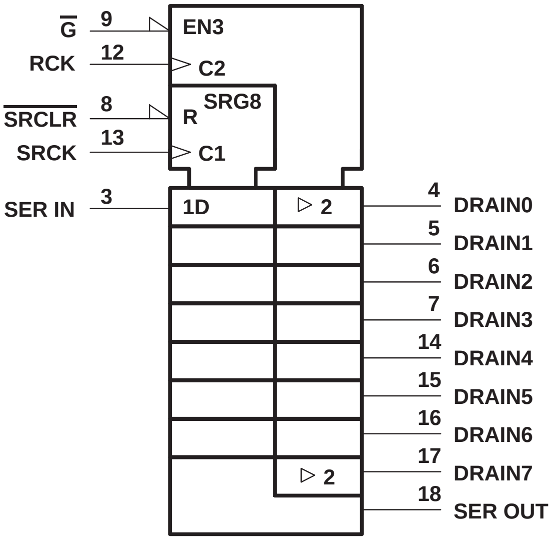


description

The TPIC6595 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK) respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{\text{SRCLR}}$) is high. When $\overline{\text{SRCLR}}$ is low, the input shift register is cleared. When output enable ($\overline{\text{G}}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{\text{G}}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

logic symbol†



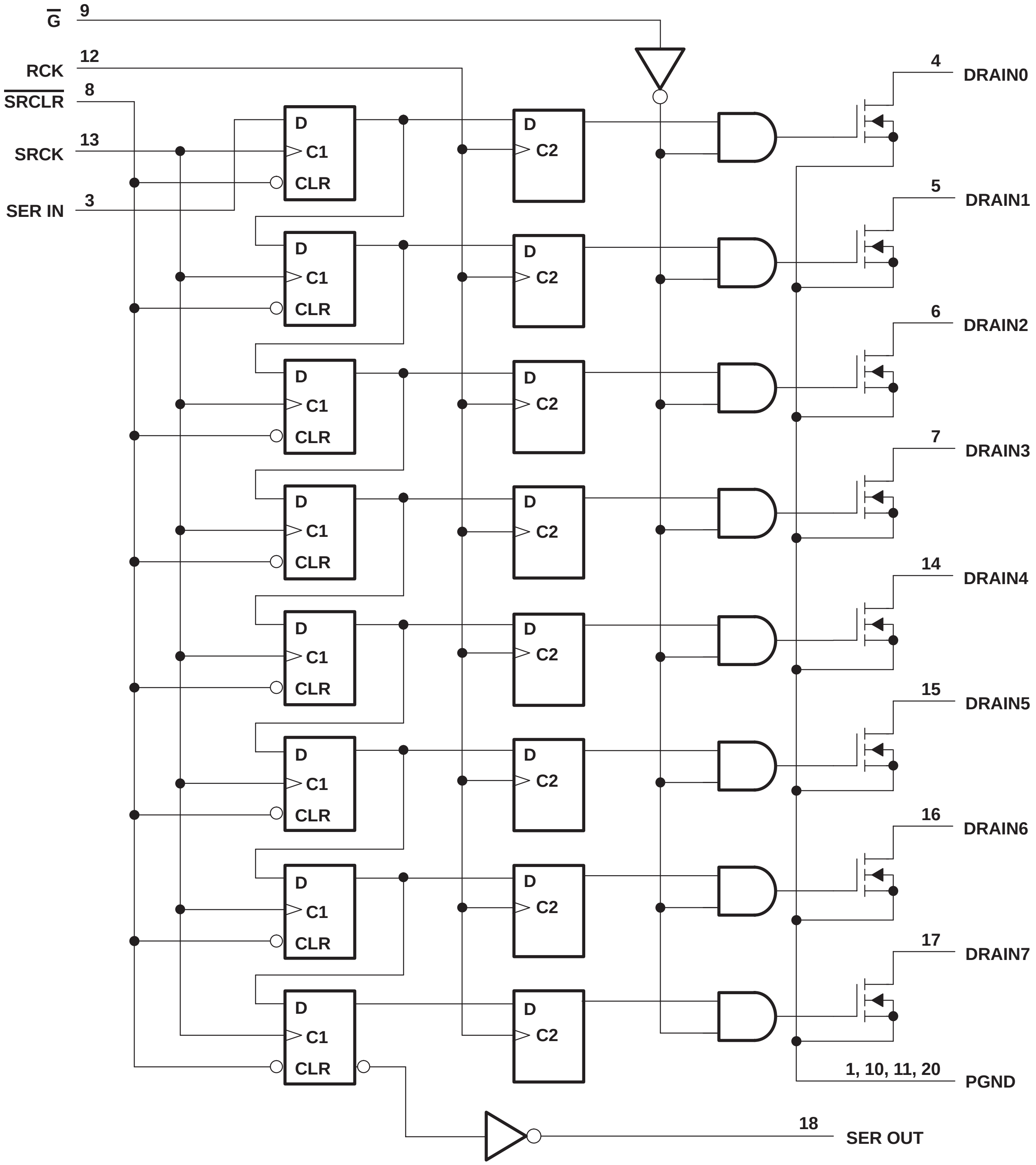
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Outputs are low-side, open-drain DMOS transistors with output ratings of 45 V and 250-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

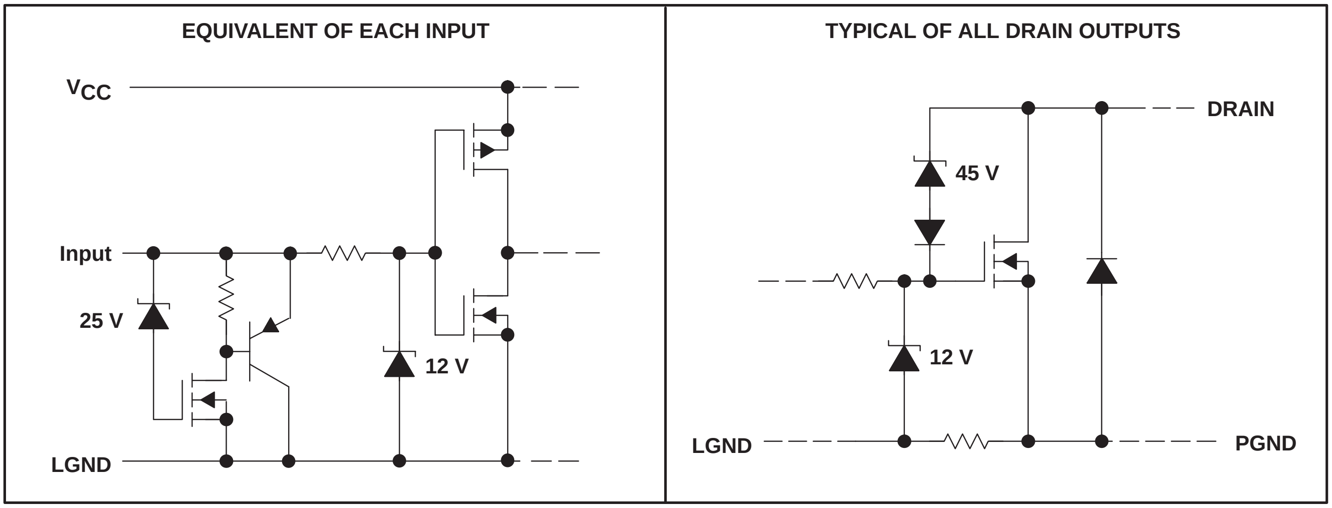
Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 19, logic ground (LGND), and pins 1, 10, 11, and 20, power grounds (PGND), must be externally made in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, $I_{Dn,}$ T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, $I_{Dn,}$ T_A = 25°C	250 mA
Peak drain current single output, $I_{DM,}T_A$ = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Note 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

---

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2 %
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	1.5	A
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	10		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20 mA, V_{CC} = 4.5 V		4.4	4.49		V
		I_{OH} = −4 mA, V_{CC} = 4.5 V		4.1	4.3		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 mA, V_{CC} = 4.5 V			0.002	0.1	V
		I_{OH} = 4 mA, V_{CC} = 4.5 V			0.2	0.4	
$V_{(hys)}$	Input hysteresis	V_{DS} = 15 V			1.3		V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CCL}	Logic supply current	I_O = 0, All inputs low			15	100	µA
$I_{CC(FRQ)}$	Logic supply current frequency	f_{SRCK} = 5 MHz, I_O = 0, C_L = 30 pF, See Figures 1, 2, and 6			0.6	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 9 and 10		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 250 mA, See Figures 1 and 2		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			150		ns
t_r	Rise time, drain output			750		ns
t_f	Fall time, drain output			425		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES:
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

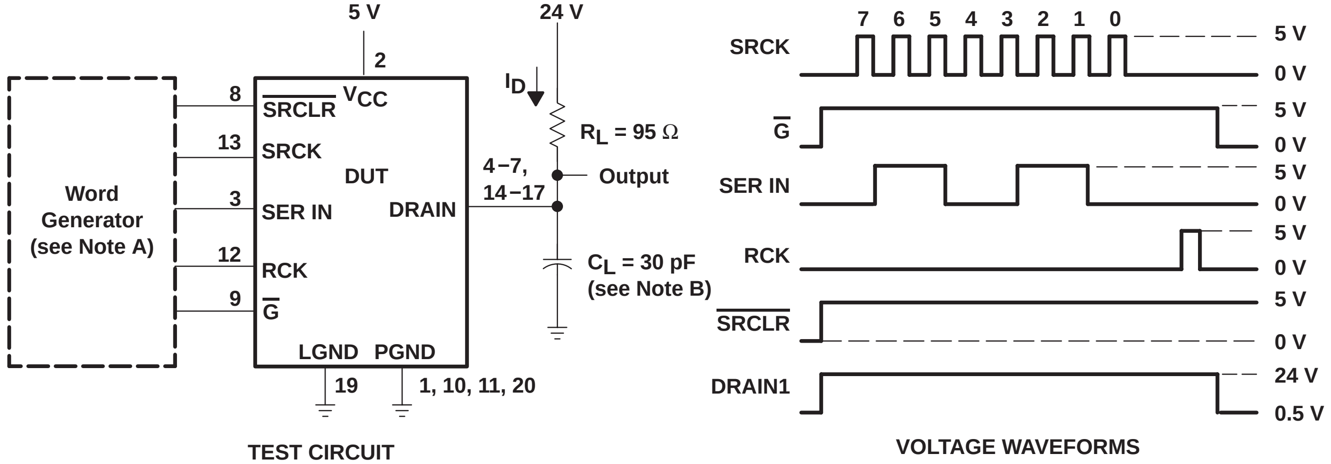


Figure 1. Resistive Load Operation

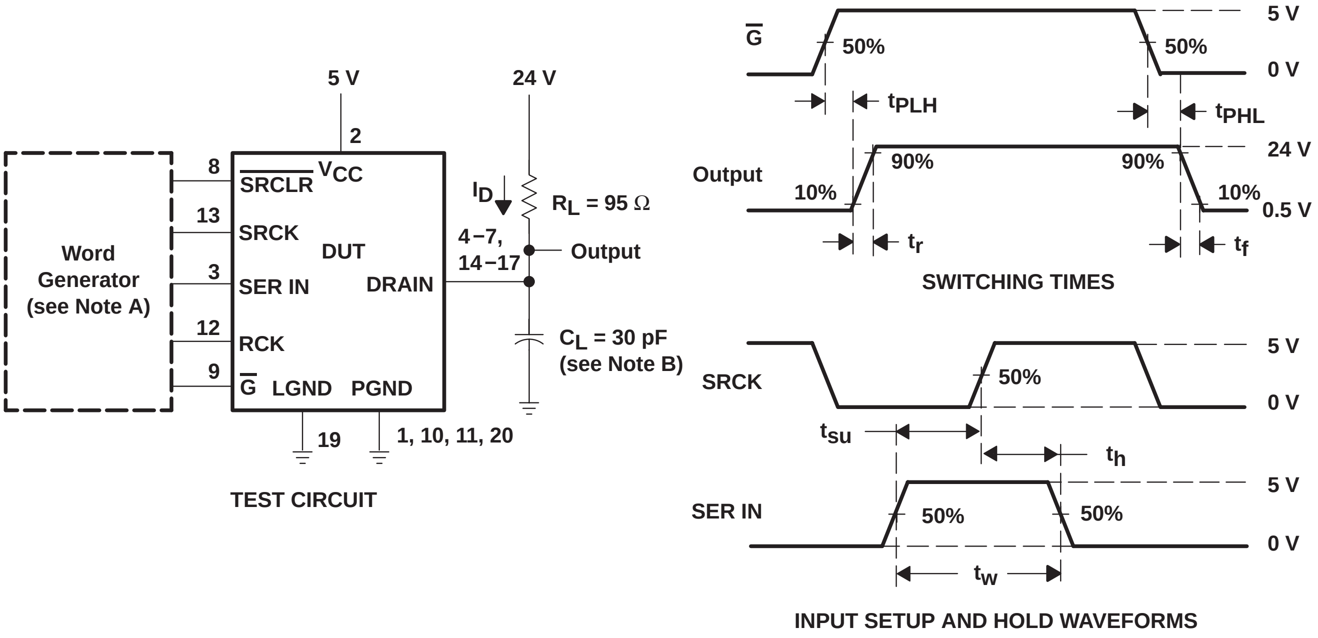
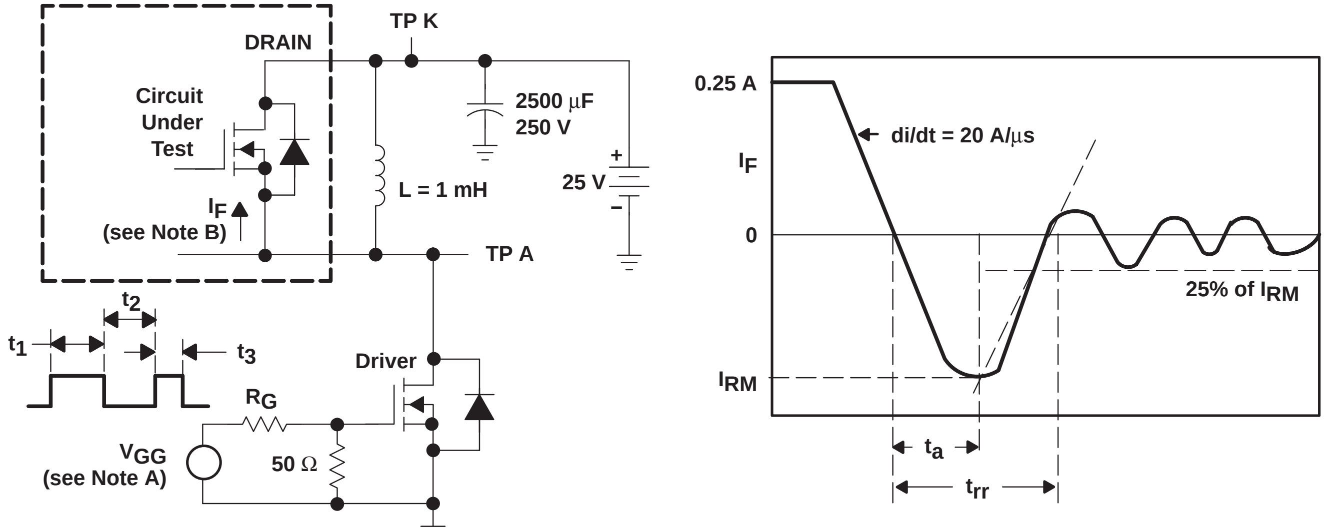


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24 V. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



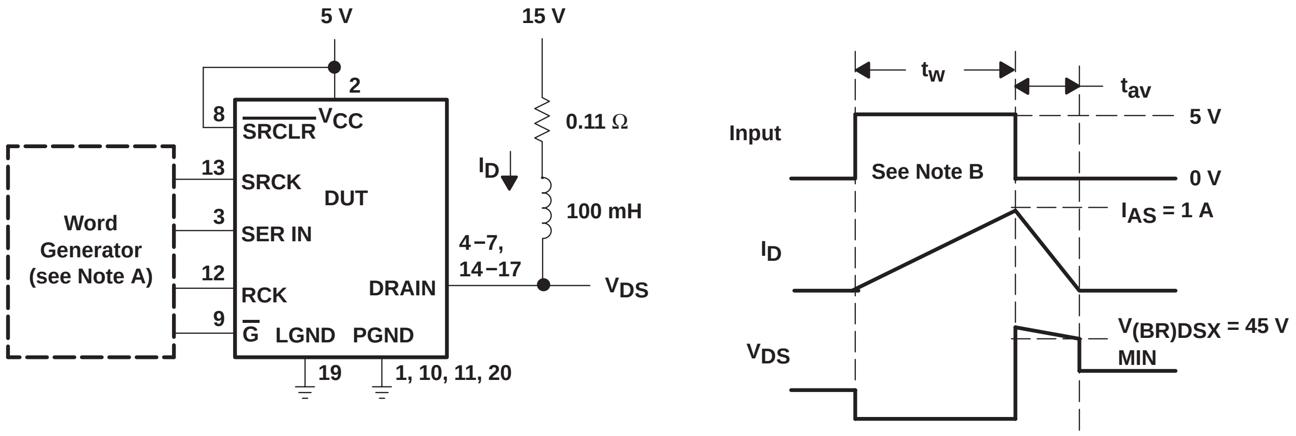
TEST CIRCUIT

CURRENT WAVEFORM

NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.

B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

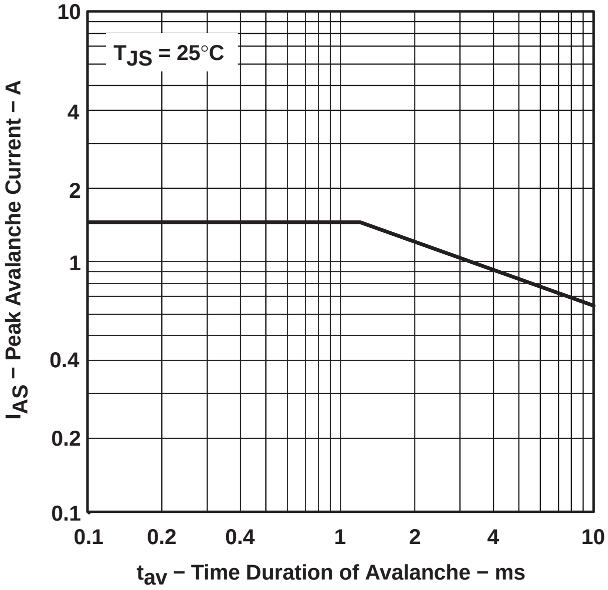


Figure 5

SUPPLY CURRENT vs FREQUENCY

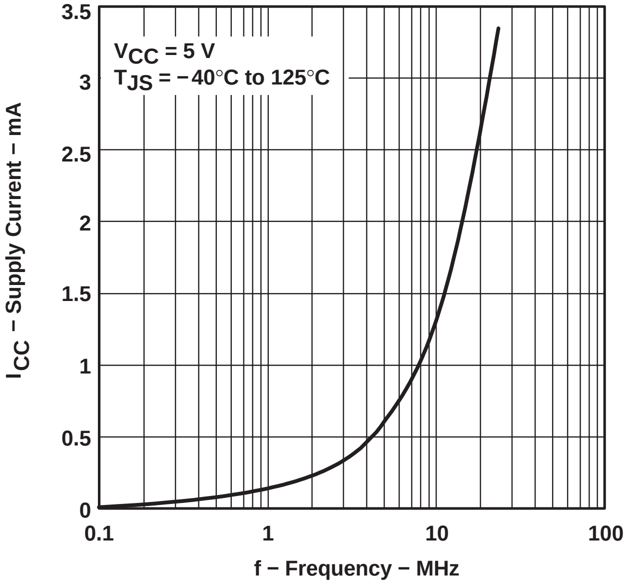


Figure 6

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

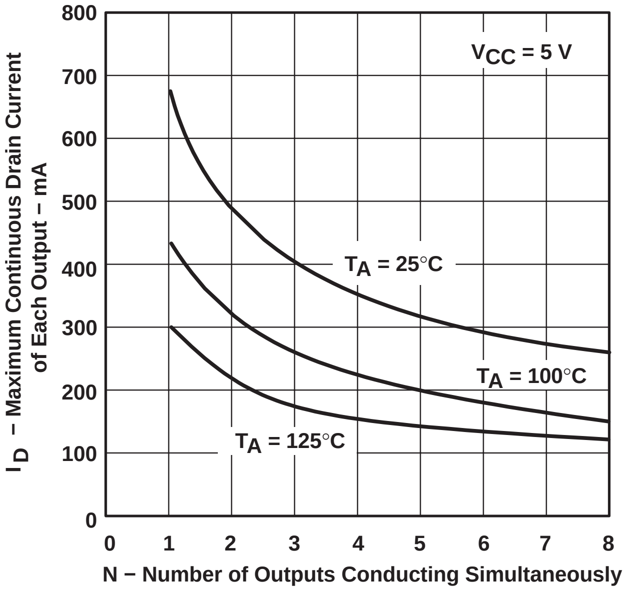


Figure 7

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

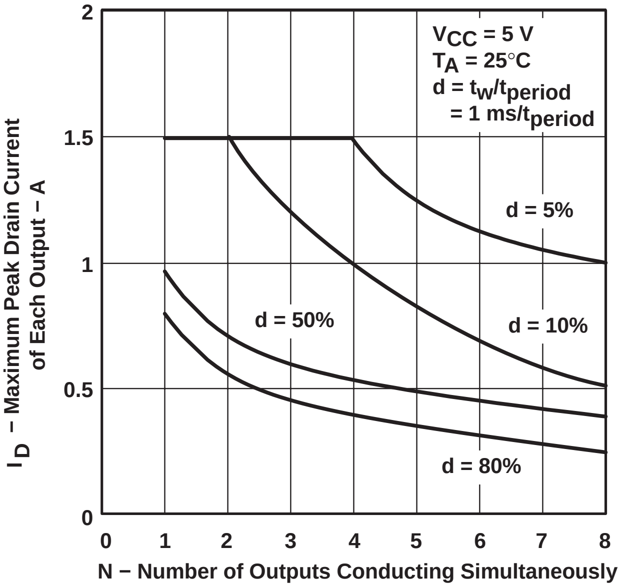


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

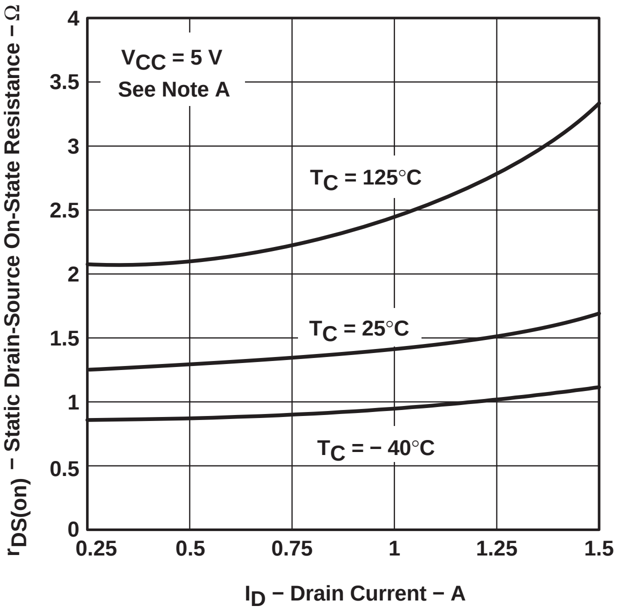


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

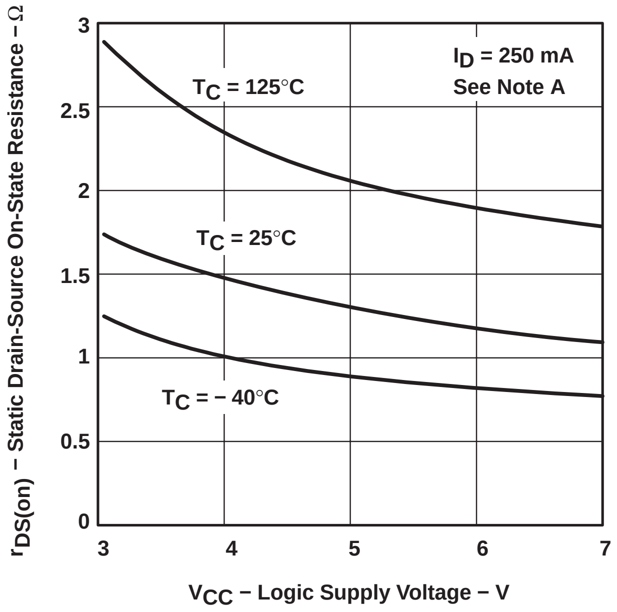


Figure 10

SWITCHING TIME vs FREE-AIR TEMPERATURE

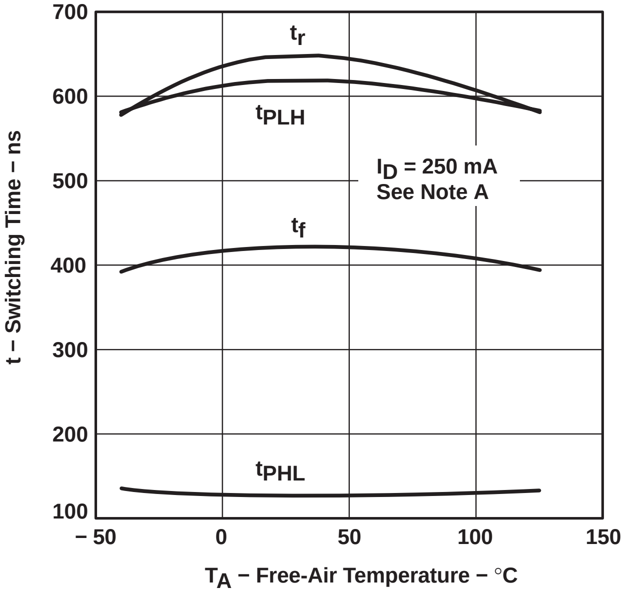


Figure 11

NOTE A: Technique should limit T_J − T_C to 10°C maximum.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
5/18/05	B	5	Figure 1	Changed $\overline{\text{SRCLR}}$ timing diagram
10/1/96	A		—	—
4/1992	*			Original reversion

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPIC6595DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6595	Samples
TPIC6595DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TPIC6595	Samples
TPIC6595DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6595	Samples
TPIC6595DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TPIC6595	Samples
TPIC6595N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TPIC6595N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

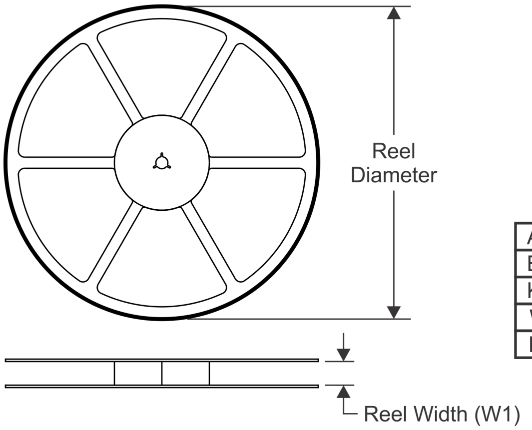
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

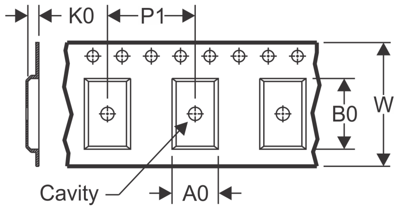
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

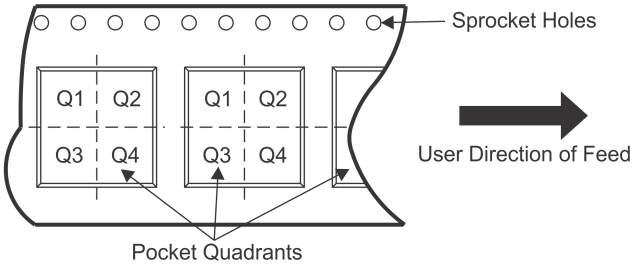


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

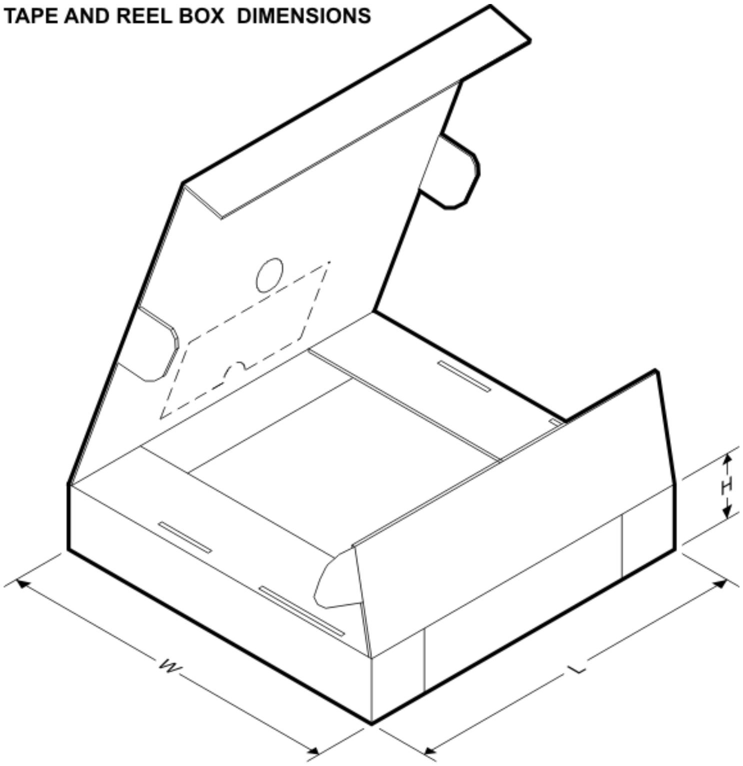
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6595DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TPIC6595DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

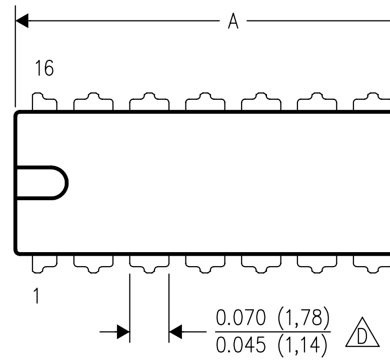


*All dimensions are nominal

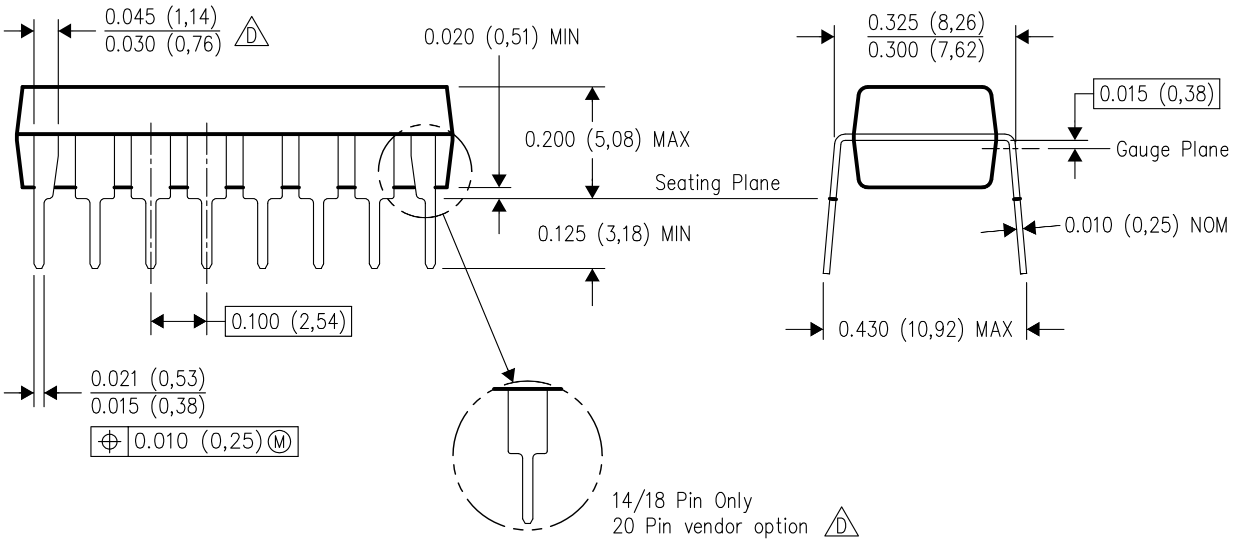
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6595DWR	SOIC	DW	20	2000	350.0	350.0	43.0
TPIC6595DWRG4	SOIC	DW	20	2000	350.0	350.0	43.0

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

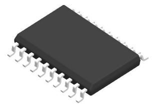


PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

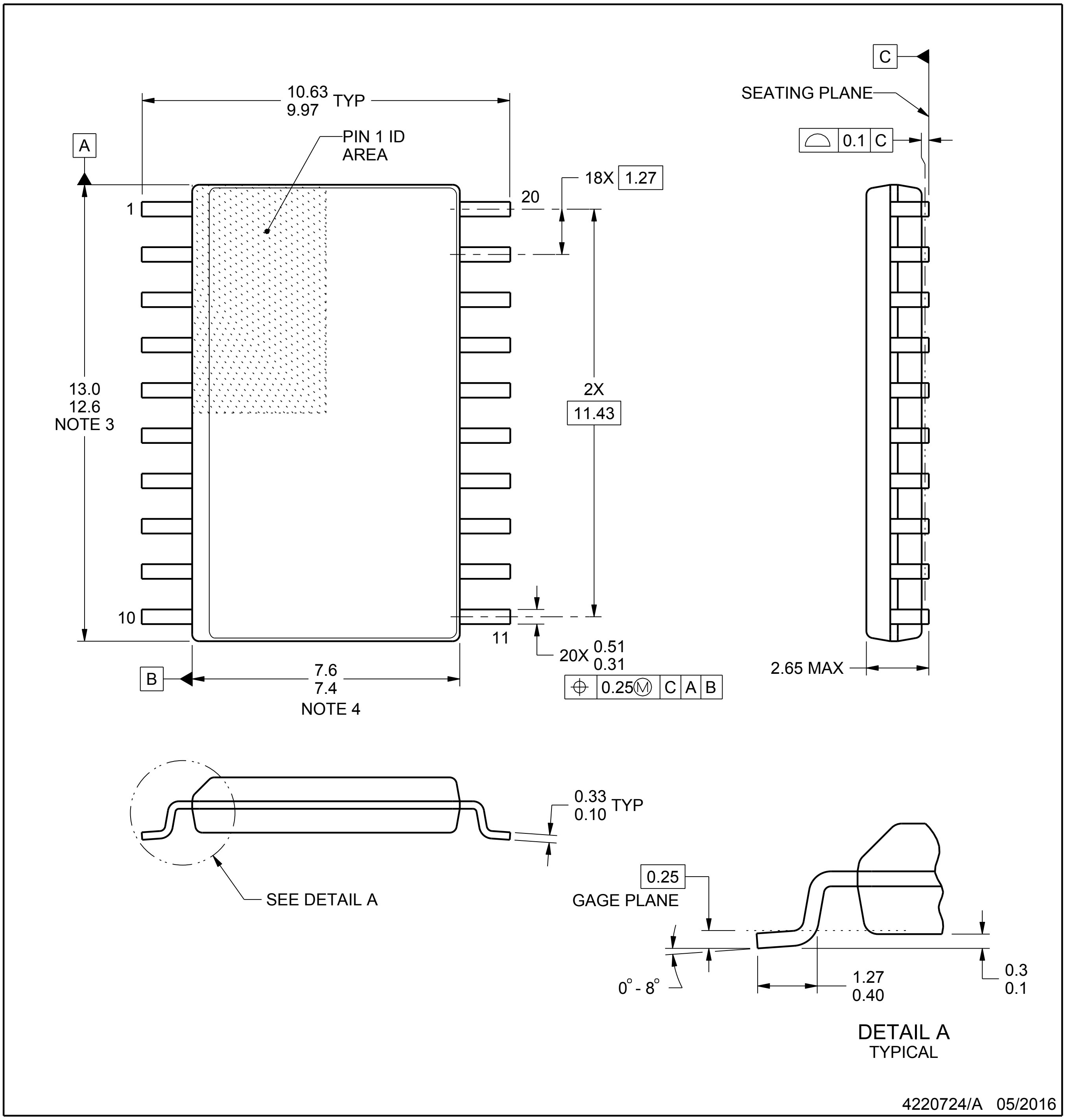


PACKAGE OUTLINE

DW0020A

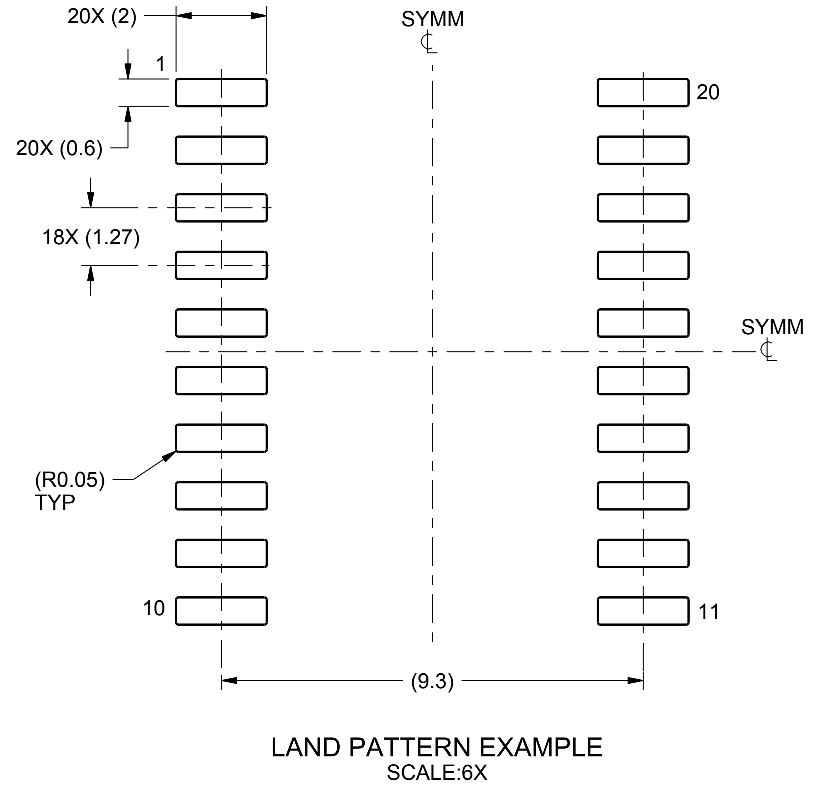
SOIC - 2.65 mm max height

SOIC

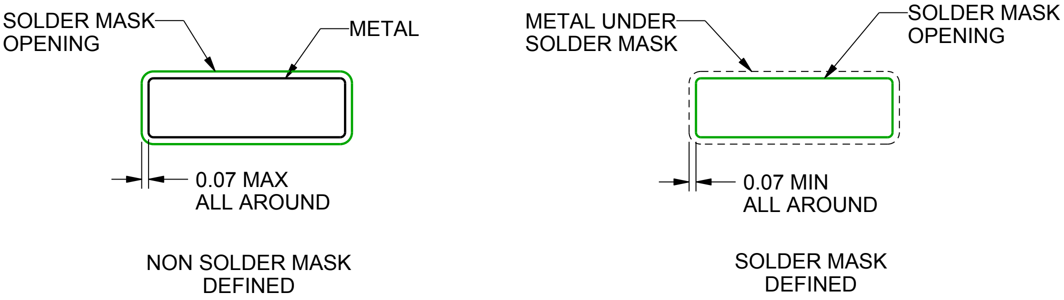


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

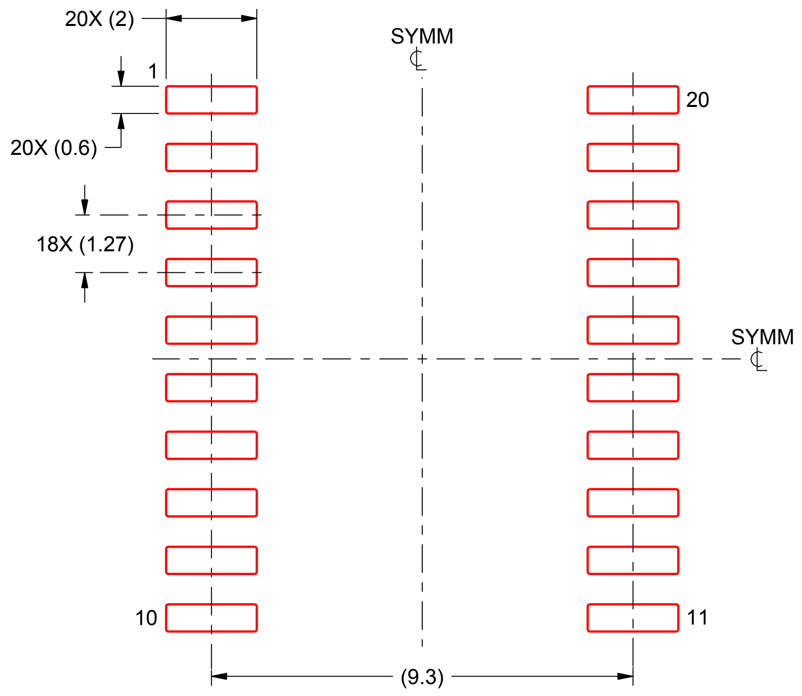


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated