

Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

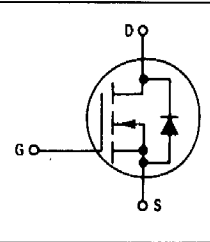
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTM2N85
MTM2N90
MTP2N85
MTP2N90

TMOS POWER FETs
2 AMPERES
 $r_{DS(on)} = 8 \text{ OHMS}$
850 and 900 VOLTS

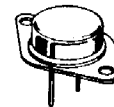


MAXIMUM RATINGS

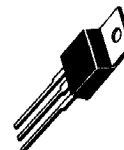
Rating	Symbol	MTM2N85	MTM2N90	Unit
		MTP2N85	MTP2N90	
Drain-Source Voltage	V_{DSS}	850	900	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	850	900	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50 \mu\text{s}$)	V_{GS} V_{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	2 7		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	- 65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient	$R_{\theta JA}$	30	
		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C



MTM2N85
MTM2N90
TO-204AA



MTP2N85
MTP2N90
TO-220AB

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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	MTM/MTP2N85 MTM/MTP2N90	V _{(BR)DSS}	850 900	— —	V _{dc}
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) (V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 0, T _J = 125°C)		I _{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)		I _{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)		I _{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) T _J = 100°C		V _{GS(th)}	2 1.5	4.5 4	V _{dc}
Static Drain-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 1 Adc)		r _{DS(on)}	—	8	Ohms
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 2 Adc) (I _D = 1 Adc, T _J = 100°C)		V _{DS(on)}	— —	20 16	V _{dc}
Forward Transconductance (V _{DS} = 15 V, I _D = 1 A)		g _{FS}	0.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz) See Figure 11	C _{iss}	—	1200	pF
Output Capacitance		C _{oss}	—	300	
Reverse Transfer Capacitance		C _{rss}	—	80	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V _{DD} = 125 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figures 9, 13 and 14	t _{d(on)}	—	50	ns
Rise Time		t _r	—	150	
Turn-Off Delay Time		t _{d(off)}	—	200	
Fall Time		t _f	—	100	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V) See Figure 12	Q _g	33 (Typ)	40	nC
Gate-Source Charge		Q _{gs}	20 (Typ)	—	
Gate-Drain Charge		Q _{gd}	13 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	(I _S = Rated I _D V _{GS} = 0)	V _{SD}	1 (Typ)	1.4	V _{dc}
Forward Turn-On Time		t _{on}	Limited by stray inductance		
Reverse Recovery Time		t _{rr}	420 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L _d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L _s	12.5 (Typ)	—	

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L _s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



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