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3N187

Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 300 MHz

Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance — g_{fs} = 12,000 μmho (typ.)
- High unneutralized RF power gain — G_{ps} = 18 dB(typ.) at 200 MHz
- Low VHF noise figure — 3.5 dB(typ.) at 200 MHz

Applications

- RF amplifier, mixer, and IF amplifier in military, and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's
- Wide dynamic range permits large-signal handling before overload
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

Maximum Ratings,

Absolute-Maximum Values, at T_A = 25°C

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No. 1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No. 2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE: Storage and Operating	-65 to +175	°C
* LEAD TEMPERATURE (During Soldering): At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265	°C

* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

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ELECTRICAL CHARACTERISTICS, at T_A = 25° C unless otherwise specified

	CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
*	Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		-0.5	-2	-4	V
*	Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		-0.5	-2	-4	V
*	Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V $V_{G2S} = V_{DS}$ = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V $V_{G2S} = V_{DS}$ = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V $V_{G1S} = V_{DS}$ = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V $V_{G1S} = V_{DS}$ = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V V_{G2S} = +4 V V_{G1S} = 0		5	15	30	mA
	Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 kHz		7000	12,000	18,000	μmho
*	Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz		4.0	6.0	8.5	pF
*	Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1)♦	C_{rss}			0.005	0.02	0.03	pF
*	Small-Signal, Short-Circuit Output Capacitanc	C_{oss}			–	2.0	–	pF
	Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 200 MHz		16	18	22	dB
	Maximum Available Power Gain	MAG			–	20	–	dB
	Maximum Usable Power Gain (unneutralized)	MUG			–	20▲	–	dB
	Noise Figure (see Fig. 1)	NF			–	3.5	4.5	dB
*	Magnitude of Forward Transadmittance	$\|Y_{fs}\|$			–	12,000	–	μmho
*	Phase Angle of Forward Transadmittance	θ			–	-35	–	Degrees
	Magnitude of Reverse Transadmittance	$\|Y_{rs}\|$			–	25	–	μmho
	Angle of Reverse Transadmittance	θ_{rs}			–	-25	–	Degrees
*	Input Resistance	r_{iss}			–	1.0	–	kΩ
*	Output Resistance	r_{oss}			–	2.8	–	kΩ
*	Gate-to-Source Forward Breakdown Voltage: Gate No. 1 Gate No. 2	$V_{(BR)G1SSF}$ $V_{(BR)G2SSF}$	$I_{G1SSF} = I_{G2SSF}$ = 100 μA		6.5	10	–	V
*	Gate-to-Source Reverse Breakdown Voltage: Gate No. 1 Gate No. 2	$V_{(BR)G1SSR}$ $V_{(BR)G2SSR}$	$I_{G1SSR} = I_{G2SSR}$ = -100 μA		-6.5	-10	–	V

▲Limited only by practical design considerations.

† Capacitance between Gate No. 1 and all other terminals

♦ Three-terminal measurement with Gate No. 2 and Source returned to ground terminal.

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OPERATING CONSIDERATIONS

The flexible leads of the 3N187 are usually soldered to th circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

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