+36V, +150mA, Ultralow-Noise, Positive LINEAR REGULATOR

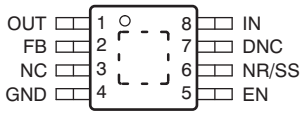
FEATURES

- **Input Voltage Range: +3V to +36V**
- **Noise:**
  - **12.7μV_{RMS} (20Hz to 20kHz)**
  - **15.4μV_{RMS} (10Hz to 100kHz)**
- **Power-Supply Ripple Rejection:**
  - **72dB (120Hz)**
  - **≥ 52dB (10Hz to 400kHz)**
- **Adjustable Output: +1.194V to +33V**
- **Output Current: 150mA**
- **Dropout Voltage: 260mV at 100mA**
- **Stable with Ceramic Capacitors ≥ 2.2μF**
- **CMOS Logic-Level-Compatible Enable Pin**
- **Built-In, Fixed, Current-Limit and Thermal Shutdown Protection**
- **Available in High Thermal Performance MSOP-8 PowerPAD™ Package**
- **Operating Tempature Range: –40°C to +125°C**

APPLICATIONS

- **Supply Rails for Op Amps, DACs, ADCs, and Other High-Precision Analog Circuitry**
- **Audio**
- **Post DC/DC Converter Regulation and Ripple Filtering**
- **Test and Measurement**
- **RX, TX, and PA Circuitry**
- **Industrial Instrumention**
- **Base Stations and Telecom Infrastrucure**

DGN PACKAGE
3mm × 5mm MSOP-8 PowerPAD
(TOP VIEW)



DESCRIPTION

The TPS7A49xx series of devices are positive, high-voltage (+36V), ultralow noise (15.4μV_{RMS}, 72dB PSRR) linear regulators capable of sourcing a load of 150mA.

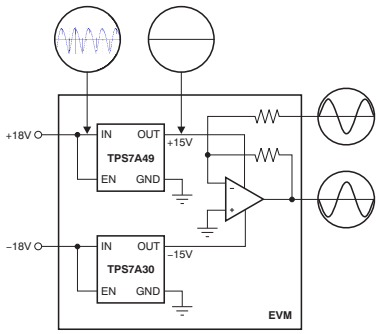
These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A49xx family is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes it an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A49xx family of linear regulators is suitable for post dc/dc converter regulation. By filtering out the output voltage ripple inherent to dc/dc switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

For applications where both positive and negative high-performance rails are required, consider TI's TPS7A30xx family of negative high-voltage, ultralow-noise linear regulators as well.

Typical Application



Post DC/DC Converter Regulation for High-Performace Analog Circuitry

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TPS7A49**xx** ***yyy*** **z**	**XX** is nominal output voltage (01 = Adjustable).(2) **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) For fixed -1.2V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN pin to GND pin	–0.3	+36	V
	OUT pin to GND pin	–0.3	+33	V
	OUT pin to IN pin	–36	+0.3	V
	FB pin to GND pin	–0.3	+2	V
	FB pin to IN pin	–36	+0.3	V
	EN pin to IN pin	–36	0.3	
	EN pin to GND pin	–0.3	+36	V
	NR/SS pin to IN pin	–36	+0.3	V
	NR/SS pin to GND pin	–0.3	+2	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge rating	Human body model (HBM)		1500	V
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS7A49xx DGN 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	55.09	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	8.47	
θ_{JB}	Junction-to-board thermal resistance	—	
ψ_{JT}	Junction-to-top characterization parameter	0.36	
ψ_{JB}	Junction-to-board characterization parameter	14.6	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	DERATING FACTOR ABOVE T_A = +25°C	$T_A \le$ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
High-K(1)	DGN	55.9°C/W	8.47°C/W	16.6mW/°C	1.83W	1.08W	0.833W

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch multilayer board with 2-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

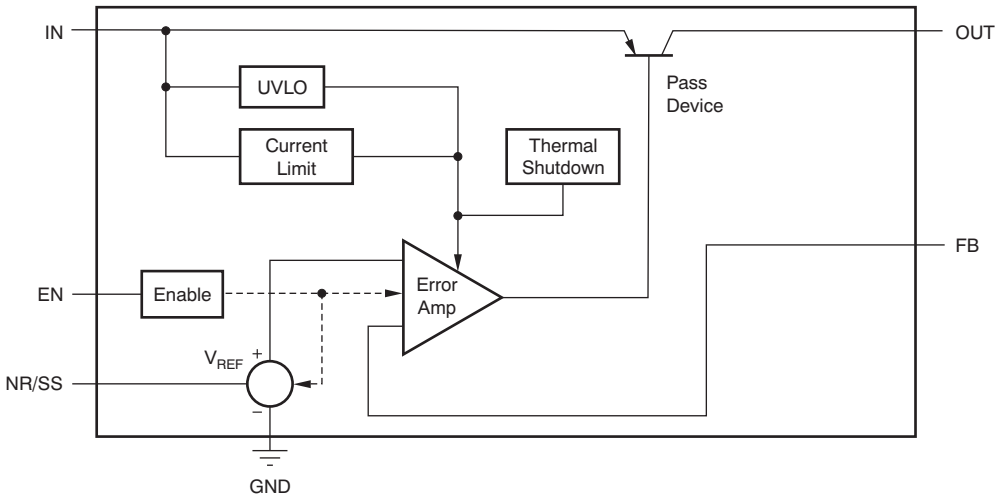
At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or V_{IN} = 3.0V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, $C_{NR/SS}$ = 0nF, and the FB pin tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS7A49xx			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage range		3.0		35	V
V_{REF}	Internal reference	T_J = +25°C, $V_{NR/SS}$ = V_{REF}	1.176	1.194	1.212	V
V_{OUT}	Output voltage range(1)	V_{IN} ≥ $V_{OUT(NOM)}$ + 1.0V	V_{REF}		33.0	V
	Nominal accuracy	T_J = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V	–1.5		+1.5	%V_{OUT}
	Overall accuracy	$V_{OUT(NOM)}$ + 1.0V ≤ V_{IN} ≤ 35V 1mA ≤ I_{OUT} ≤ 150mA	–2.5		+2.5	%V_{OUT}
$\frac{\Delta V_{OUT}(\Delta V_{IN})}{V_{OUT(NOM)}}$	Line regulation	T_J = +25°C, $V_{OUT(NOM)}$ + 1.0V ≤ V_{IN} ≤ 35V		0.11		%V_{OUT}
$\frac{\Delta V_{OUT}(\Delta I_{OUT})}{V_{OUT(NOM)}}$	Load regulation	T_J = +25°C, 1mA ≤ I_{OUT} ≤ 150mA		0.04		%V_{OUT}
V_{DO}	Dropout voltage	V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 100mA		260		mV
		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 150mA		333	600	mV
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$	220	309	500	mA
I_{GND}	Ground current	I_{OUT} = 0mA		61	100	µA
		I_{OUT} = 100mA		800		µA
I_{SHDN}	Shutdown supply current	V_{EN} = +0.4V		0.8	3.0	µA
I_{FB}	Feedback current(2)			3	100	nA
I_{EN}	Enable current	V_{EN} = V_{IN} = $V_{OUT(NOM)}$ + 1.0V		0.02	1.0	µA
		V_{EN} = V_{IN} = +35V		0.2	1.0	µA
V_{EN_HI}	Enable high-level voltage		+2.1		V_{IN}	V
V_{EN_LO}	Enable low- level voltage		0		+0.4	V
V_{NOISE}	Output noise voltage	V_{IN} = +3V, $V_{OUT(NOM)}$ = V_{REF}, C_{OUT} = 10µF, $C_{NR/SS}$ = 10nF, BW = 10Hz to 100kHz		15.4		μV_{RMS}
		V_{IN} = +6.2V, $V_{OUT(NOM)}$ = +5V, C_{OUT} = 10µF, $C_{NR/SS}$ = C_{BYP}(3) = 10nF, BW = 10Hz to 100kHz		21.15		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = +6.2V, $V_{OUT(NOM)}$ = +5V, C_{OUT} = 10µF, $C_{NR/SS}$ = C_{BYP}(3) = 10nF, f = 120Hz		72		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+170		°C
		Reset, temperature decreasing		+150		°C
T_J	Operating junction temperature range		–40		+125	°C

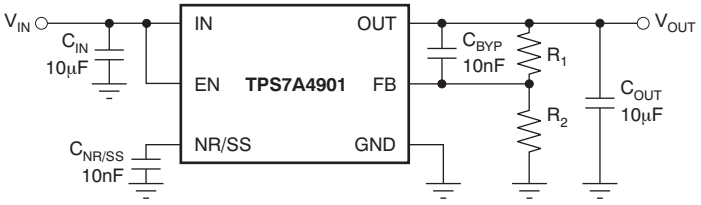
(1) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than 5µA is required.
(2) I_{FB} > 0 flows out of the device.
(3) C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



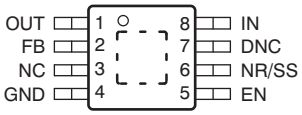
Where: $\frac{V_{OUT}}{R_1 + R_2} \geq 5\mu A$, and

$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$

Maximize PSRR Performance and Minimize RMS Noise

PIN CONFIGURATION

DGN PACKAGE
MSOP-8
(TOP VIEW)



PIN DESCRIPTIONS

TPS7A49xx		DESCRIPTION
NAME	NO.	
OUT	1	Regulator output. A capacitor ≥ 2.2μF must be tied from this pin to ground to assure stability.
FB	2	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
NC	3	Not internally connected. This pin may either be left open or tied to GND.
GND	4	Ground
EN	5	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$, the regulator is enabled. If $V_{EN\_LO} \geq V_{EN}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $V_{EN} \leq V_{IN}$.
NR/SS	6	Noise reduction pin. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This capacitor allows RMS noise to be reduced to very low levels and also controls the soft-start function.
DNC	7	**DO NOT CONNECT.** Do not route this pin to any electrical net, not even GND or IN.
IN	8	Input supply
PowerPAD		Must either be left open or tied to ground. Solder to printed circuit board (PCB) plane to enhance thermal performance.

TYPICAL CHARACTERISTICS

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or V_{IN} = 3.0V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, $C_{NR/SS}$ = 0nF, and the FB pin tied to OUT, unless otherwise noted.

FEEDBACK VOLTAGE vs INPUT VOLTAGE

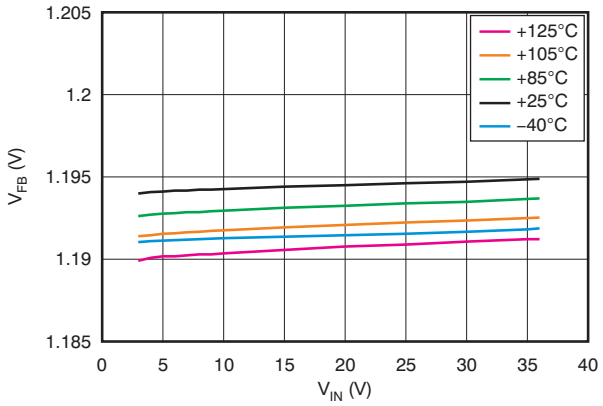


Figure 1.

FEEDBACK CURRENT vs TEMPERATURE

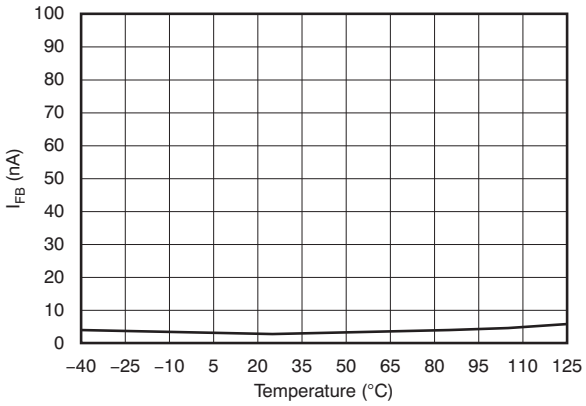


Figure 2.

GROUND CURRENT vs INPUT VOLTAGE

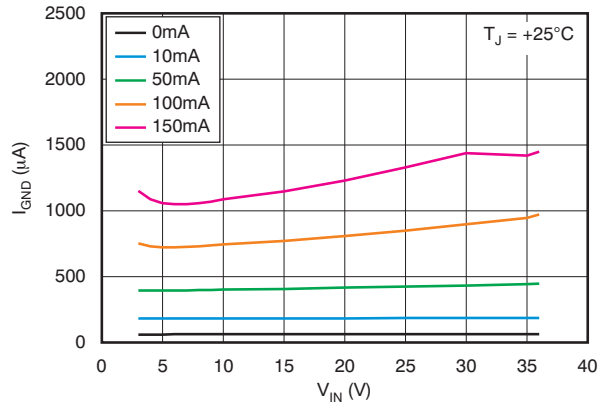


Figure 3.

GROUND CURRENT vs INPUT VOLTAGE

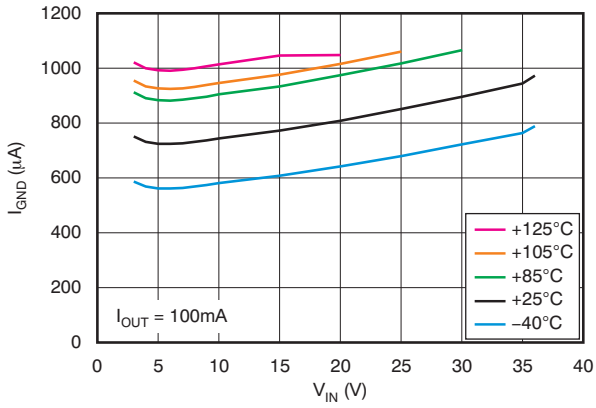


Figure 4.

GROUND CURRENT vs OUTPUT CURRENT

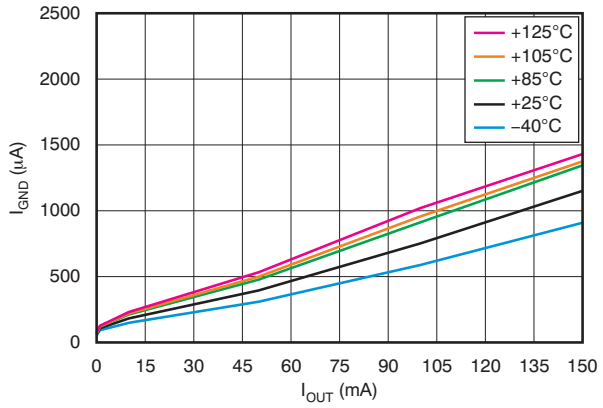


Figure 5.

ENABLE CURRENT vs ENABLE VOLTAGE

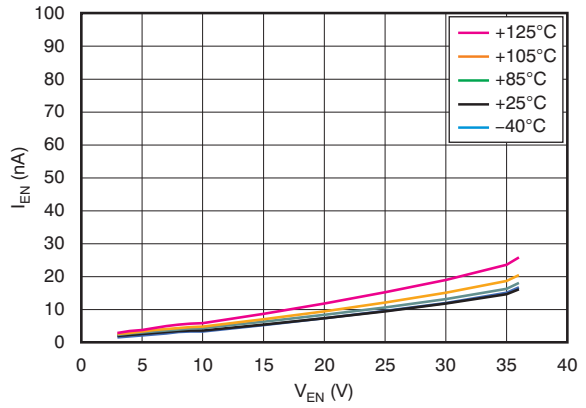


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or V_{IN} = 3.0V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, $C_{NR/SS}$ = 0nF, and the FB pin tied to OUT, unless otherwise noted.

QUIESCENT CURRENT vs INPUT VOLTAGE

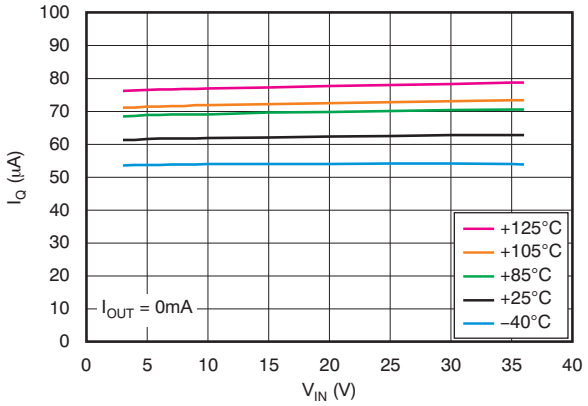


Figure 7.

SHUTDOWN CURRENT vs INPUT VOLTAGE

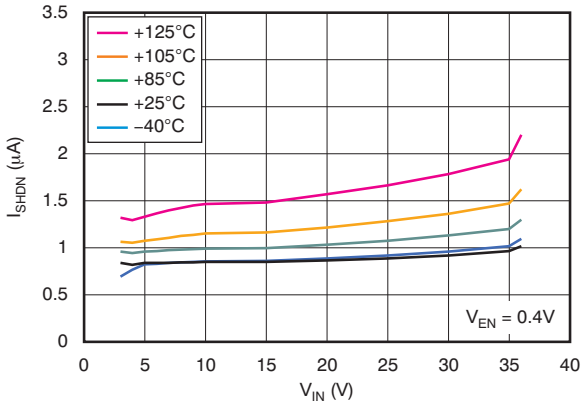


Figure 8.

DROPOUT VOLTAGE vs OUTPUT CURRENT

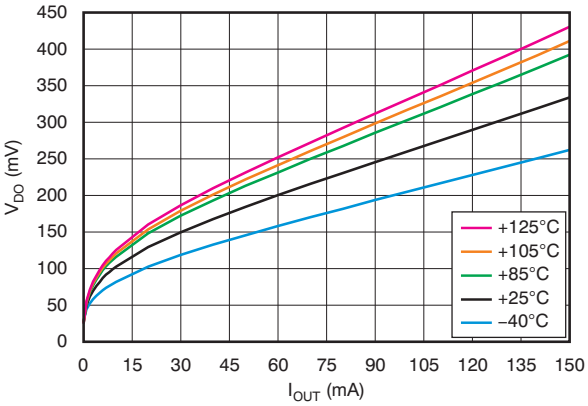


Figure 9.

DROPOUT VOLTAGE vs TEMPERATURE

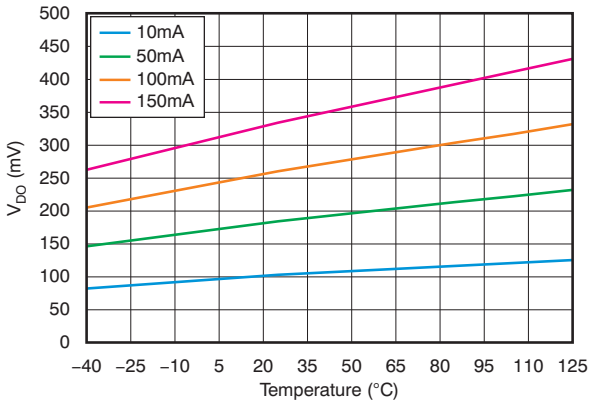


Figure 10.

CURRENT LIMIT vs INPUT VOLTAGE

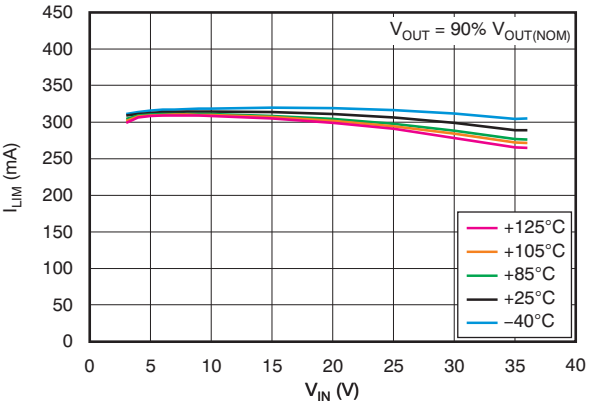


Figure 11.

CURRENT LIMIT vs TEMPERATURE

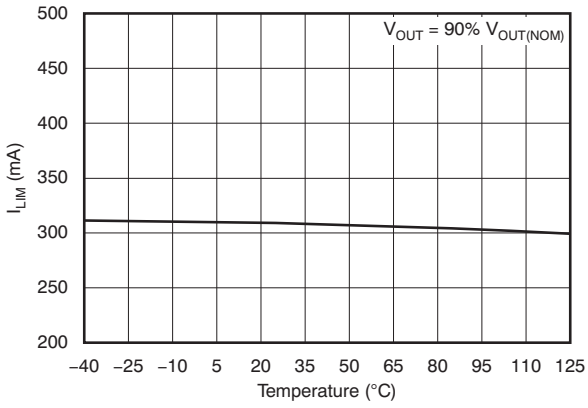


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or V_{IN} = 3.0V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, $C_{NR/SS}$ = 0nF, and the FB pin tied to OUT, unless otherwise noted.

ENABLE THRESHOLD VOLTAGE vs TEMPERATURE

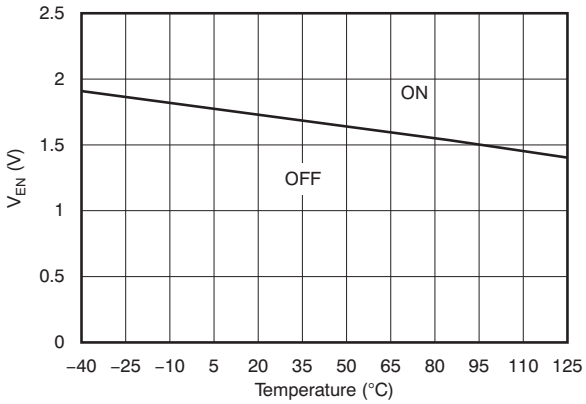


Figure 13.

POWER-SUPPLY REJECTION RATIO vs C_{OUT}

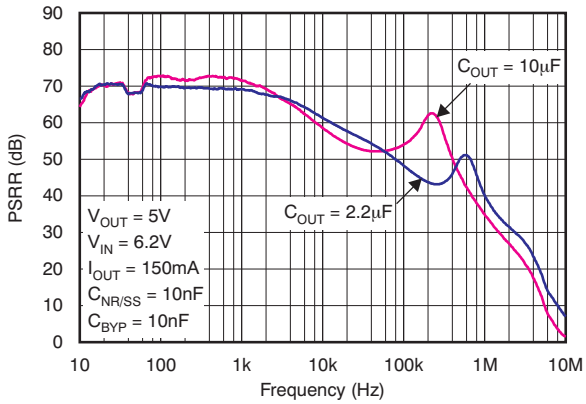


Figure 14.

LINE REGULATION

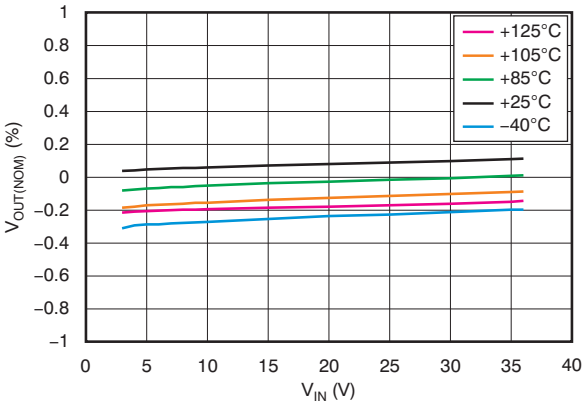


Figure 15.

POWER-SUPPLY REJECTION RATIO vs $C_{NR/SS}$

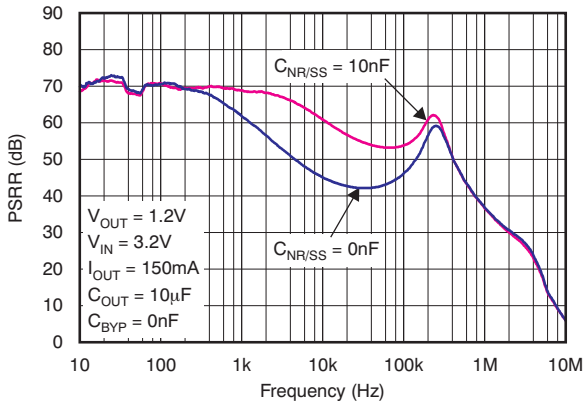


Figure 16.

LOAD REGULATION

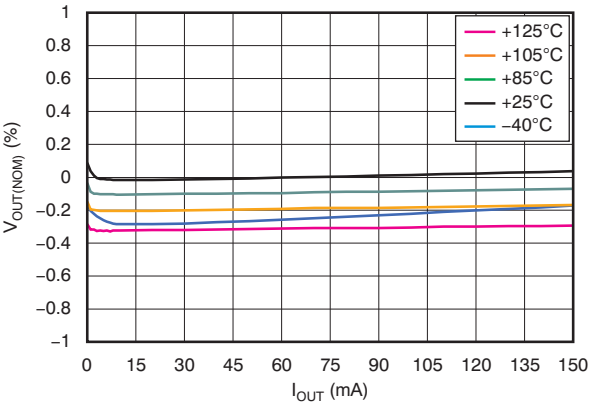


Figure 17.

POWER-SUPPLY REJECTION RATIO vs C_{BYP}

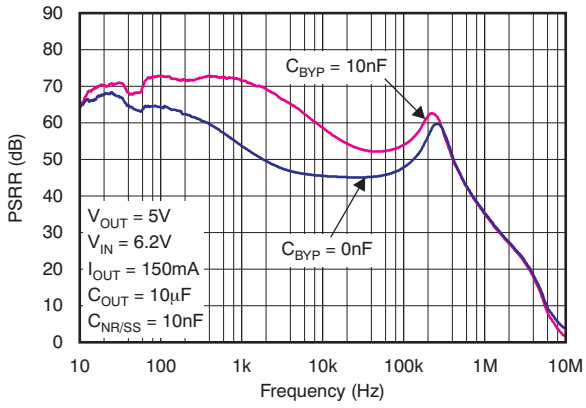
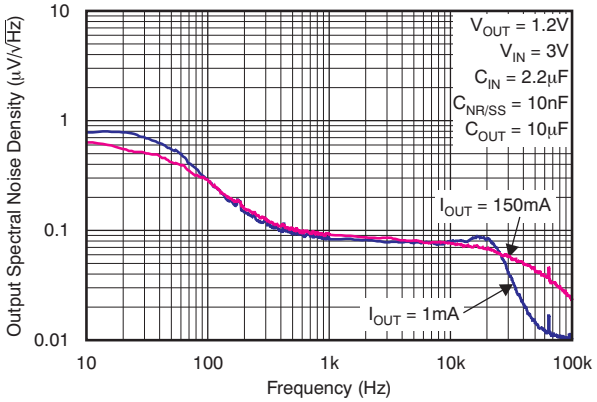


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or V_{IN} = 3.0V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, $C_{NR/SS}$ = 0nF, and the FB pin tied to OUT, unless otherwise noted.

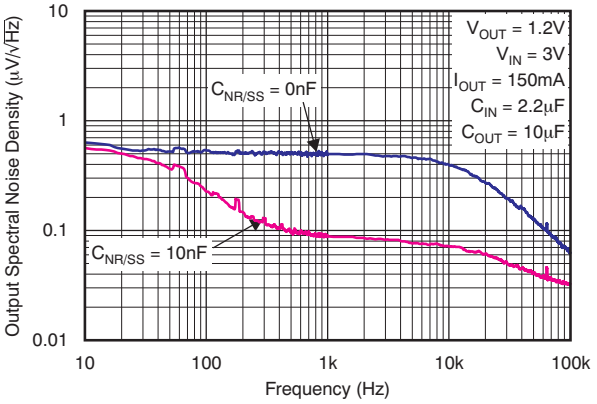
OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT CURRENT



I_{OUT}	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
1mA	15.44	14.14
150mA	17.27	16.46

Figure 19.

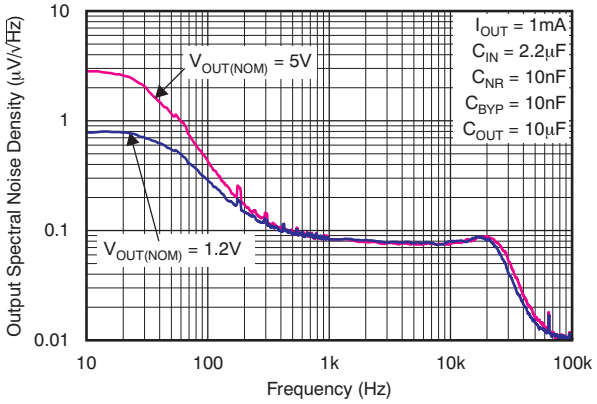
OUTPUT SPECTRAL NOISE DENSITY vs $C_{NR/SS}$



$C_{NR/SS}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
0nF	69.04	67.87
10nF	16.58	15.86

Figure 20.

OUTPUT SPECTRAL NOISE DENSITY vs $V_{OUT(NOM)}$



$V_{OUT(NOM)}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
5V	21.15	14.74
1.2V	15.44	14.14

Figure 21.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or V_{IN} = 3.0V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1mA, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, $C_{NR/SS}$ = 0nF, and the FB pin tied to OUT, unless otherwise noted.

CAPACITOR-PROGRAMMABLE SOFT-START

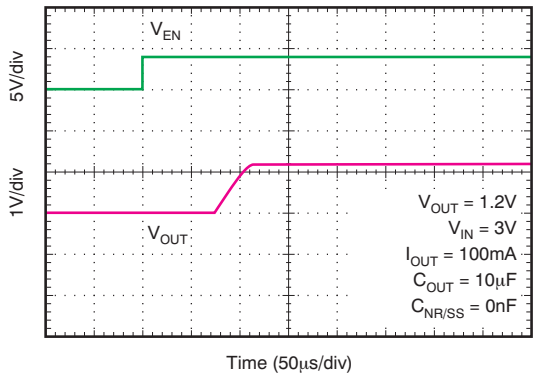


Figure 22.

CAPACITOR-PROGRAMMABLE SOFT-START

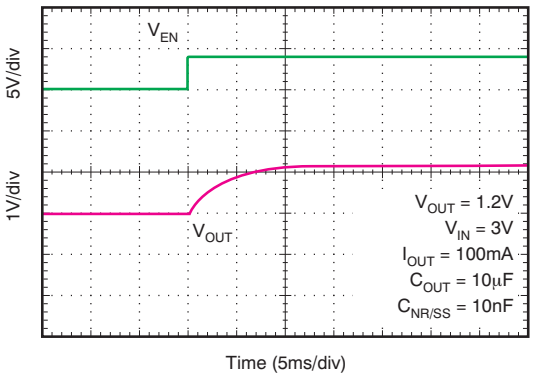


Figure 23.

LINE TRANSIENT RESPONSE

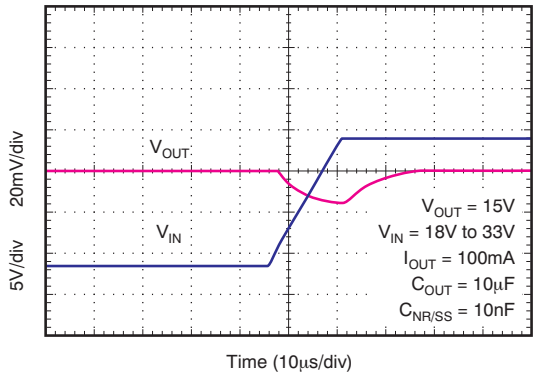


Figure 24.

LINE TRANSIENT RESPONSE

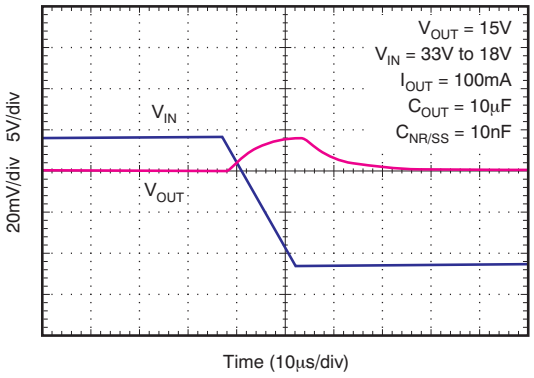


Figure 25.

LOAD TRANSIENT RESPONSE

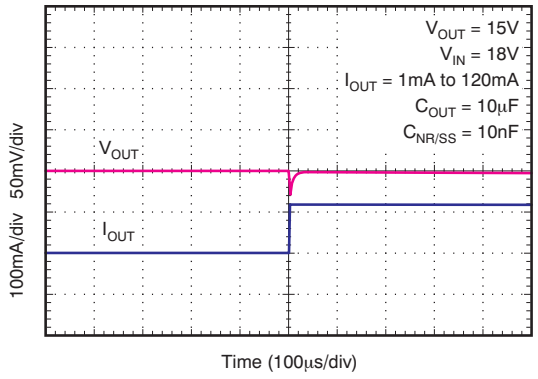


Figure 26.

LOAD TRANSIENT RESPONSE

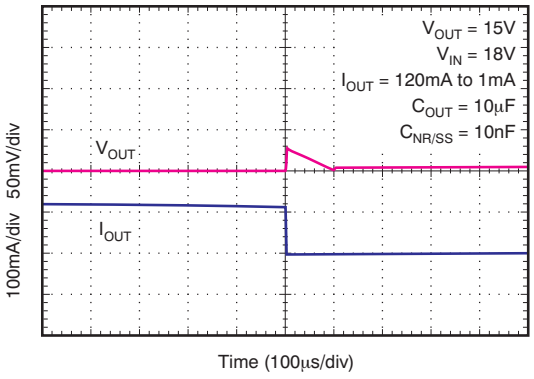


Figure 27.

THEORY OF OPERATION

GENERAL DESCRIPTION

The TPS7A49xx belongs to a family of new generation linear regulators that use an innovative bipolar process to achieve ultralow-noise and very high PSRR levels at a wide input voltage range. These features, combined with a high thermal performance MSOP-8 with PowerPAD package make this device ideal for high-performance analog applications.

ADJUSTABLE OPERATION

The TPS7A4901 has an output voltage range of +1.194 to +33V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 28.

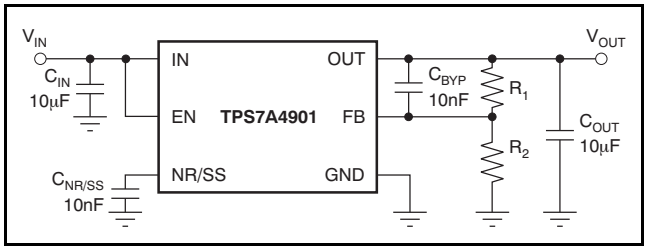


Figure 28. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 1. To ensure stability under no load conditions, this resistive network must provide a current equal to or greater than 5μA.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \quad \text{where} \quad \frac{V_{OUT}}{R_1 + R_2} \geq 5\mu A \tag{1}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

ENABLE PIN OPERATION

The TPS7A49xx provides an enable feature (EN) that turns on the regulator when V_{EN} > 2.1V.

CAPACITOR RECOMMENDATIONS

Low ESR capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high ESR capacitors may degrade PSRR. To ensure stability, maximum ESR must be less than 200mΩ.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TPS7A49xx family of positive, high-voltage linear regulators achieve stability with a minimum input and output capacitance of 2.2μF; however, it is highly recommended to use a 10μF capacitor to maximize ac performance.

NOISE REDUCTION AND BYPASS CAPACITOR REQUIREMENTS

Although noise reduction and bypass capacitors ($C_{NR/SS}$ and C_{BYP}, respectively) are not needed to achieve stability, it is highly recommended to use 0.01μF capacitors to minimize noise and maximize ac performance.

MAXIMUM AC PERFORMANCE

In order to maximize noise and PSRR performance, it is recommended to include 10μF or higher input and output capacitors, and 0.01μF noise reduction and bypass capacitors, as shown in Figure 28. The solution shown delivers minimum noise levels of 15.4μV_{RMS} and power-supply rejection levels above 52dB from 10Hz to 400kHz; see Figure 18 and Figure 19.

OUTPUT NOISE

The TPS7A49xx provides low output noise when a noise reduction capacitor ($C_{NR/SS}$) is used.

The noise reduction capacitor serves as a filter for the internal reference. By using a 0.01μF noise reduction capacitor, the output noise is reduced by almost 75% (from 69μV_{RMS} to 17μV_{RMS}); see Figure 20.

TPS7A49xx low output voltage noise makes it an ideal solution for powering noise-sensitive circuitry.

POWER-SUPPLY REJECTION

The 0.01μF noise reduction capacitor greatly improves TPS7A49xx power-supply rejection, achieving up to 15dB of additional power-supply rejection for frequencies between 110Hz and 200KHz.

Additionally, ac performance can be maximized by adding a 0.01μF bypass capacitor (C_{BYP}) from the FB pin to the OUT pin. This capacitor greatly improves power-supply rejection at lower frequencies, for the band from 10Hz to 200kHz; see Figure 18.

The very high power-supply rejection of the TPS7A49xx makes it a good choice for powering high-performance analog circuitry, such as operational amplifiers, ADCs, DACS, and audio amplifiers.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

APPLICATION INFORMATION

POWER FOR PRECISION ANALOG

One of the primary TPS7A49xx applications is to provide ultralow-noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision.

The TPS7A49xx family of positive high-voltage linear regulators in conjunction with its negative counterpart (the TPS7A30xx family of negative high-voltage linear regulators), provide ultralow-noise, positive and negative voltage rails for high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range, maximizing system accuracy.

POST DC/DC CONVERTER FILTERING

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC/DC converters are the preferred solution to step up or down a voltage rail when current consumption is not negligible. They offer high efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the dc output signal.

This high-frequency component, if not filtered properly, degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A49xx offers a wide-bandwidth, very-high power-supply rejection ratio. This specification makes it ideal for post dc/dc converter filtering, as shown in Figure 29. It is highly recommended to use the maximum performance schematic shown in Figure 28. Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR, shown in Figure 18.

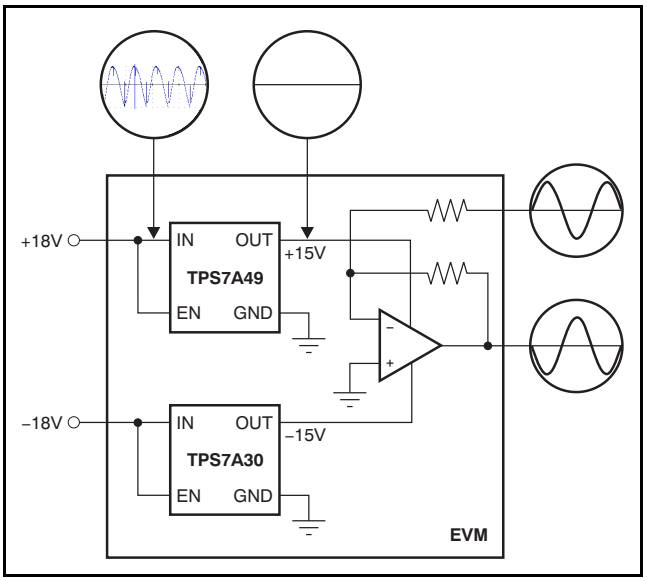


Figure 29. Post DC/DC Converter Regulation to High-Performance Analog Circuitry

AUDIO APPLICATIONS

Audio applications are extremely sensitive to any distortion and noise in the audio band from 20Hz to 20kHz. This stringent requirement demands clean voltage rails to power critical high-performance audio systems.

The very-high power-supply rejection ratio (> 55dB) and low noise at the audio band of the TPS7A49xx maximize performance for audio applications; see Figure 18.

LAYOUT

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS7A49xx are available at the end of this product datasheet and at www.ti.com.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, C_{BYP}) must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product datasheet, use the same layout pattern used for TPS7A49 evaluation board, available at www.ti.com.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of +125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A49xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A49xx into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data or JEDEC low- and high-K boards are given in the *Dissipation Ratings Table*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT})\ I_{OUT} \quad (2)$$

SUGGESTED LAYOUT AND SCHEMATIC

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with a X5R or X7R dielectric.

The GND pin should be tied directly to the PowerPAD under the IC. The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC.

It may be possible to obtain acceptable performance with alternate PCB layouts; however, the layout shown in Figure 30 and the schematic shown in Figure 31 have been shown to produce good results and are meant as a guideline.

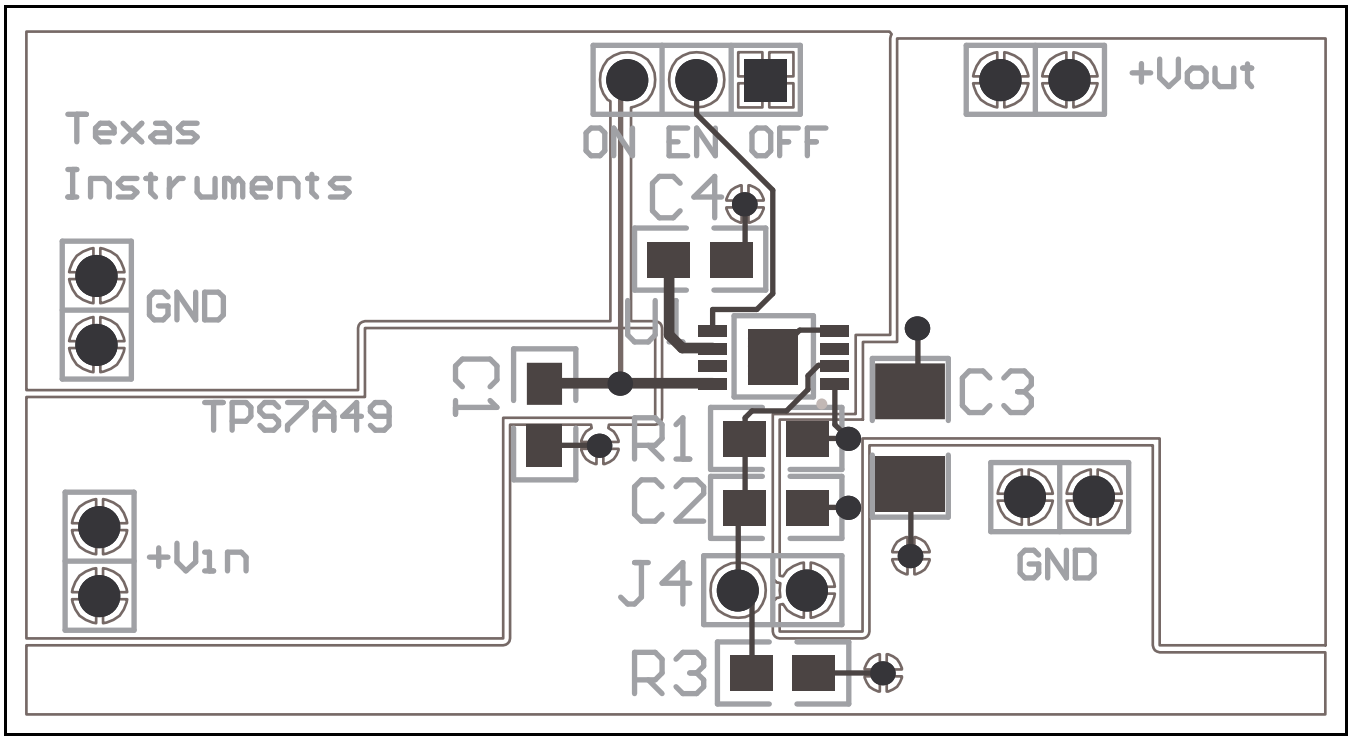


Figure 30. PCB Layout Example

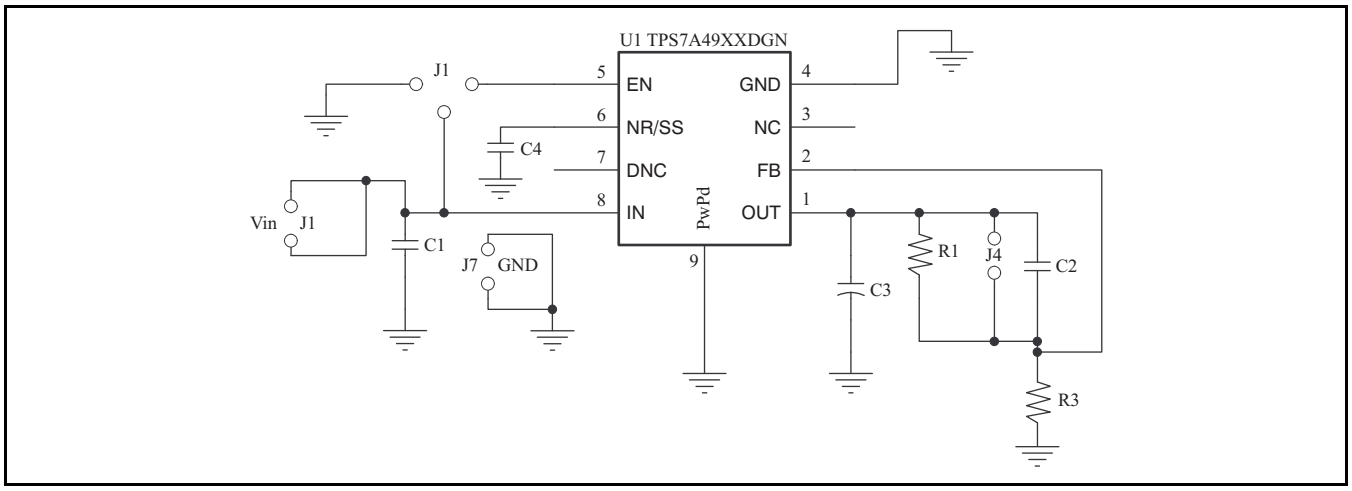


Figure 31. Schematic for PCB Layout Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2010) to Revision B **Page**

- Changed HBM max value from 500V to 1500V 2

Changes from Original (August 2010) to Revision A **Page**

- Revised *Features* list 1
- Changed *Description* text (paragraph 1) to remove description of maximum load 1
- Revised *shutdown supply current, feedback current,* and *enable current* specifications; rounded typical performance values 3
- Revised *Functional Block Diagram* for clarification 4
- Changed description of NC pin (pin 3) in *Pin Descriptions* table 5
- Updated Figure 1 to show correct device performance 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4901DGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples
TPS7A4901DGNT	ACTIVE	HVSSOP	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples
TPS7A4901DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples
TPS7A4901DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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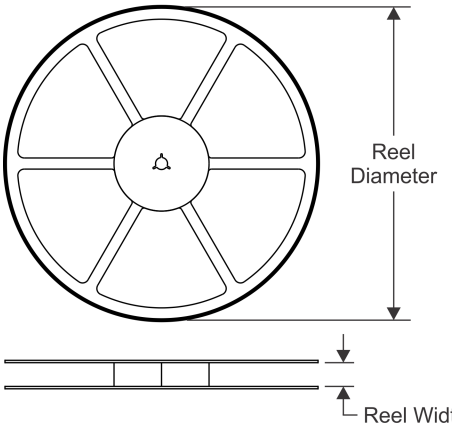
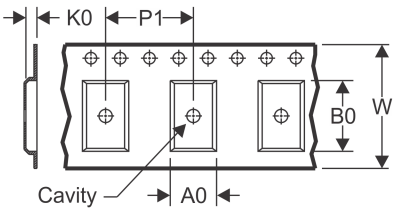
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

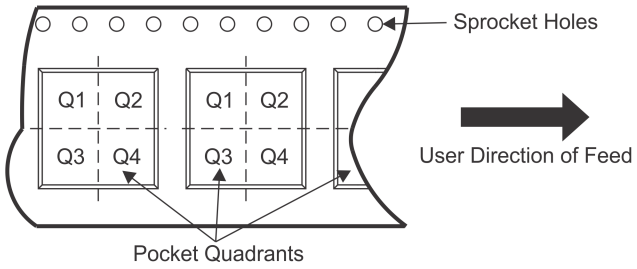


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

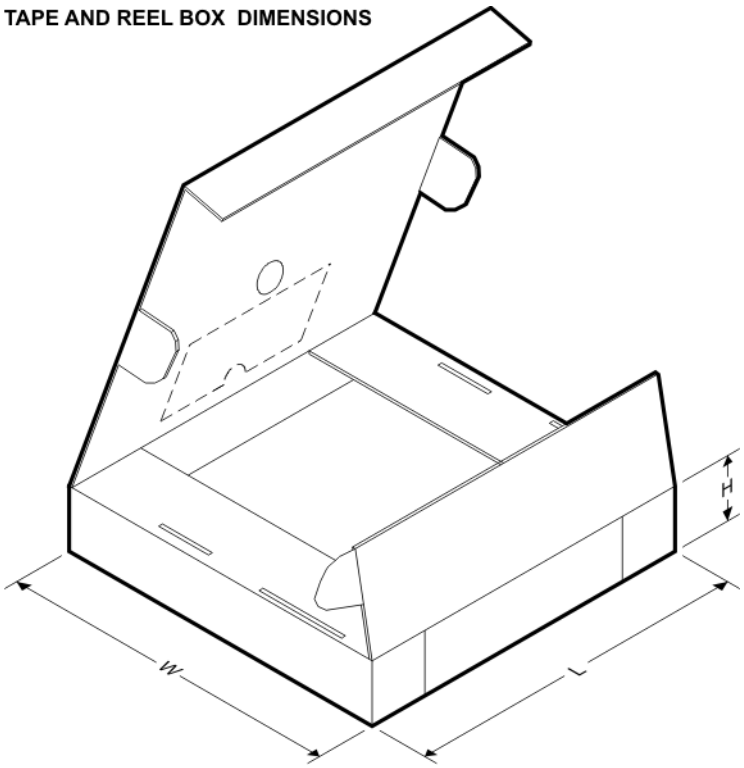
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4901DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A4901DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A4901DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A4901DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4901DGNR	HVSSOP	DGN	8	2500	367.0	367.0	35.0
TPS7A4901DGNT	HVSSOP	DGN	8	250	210.0	185.0	35.0
TPS7A4901DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS7A4901DRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

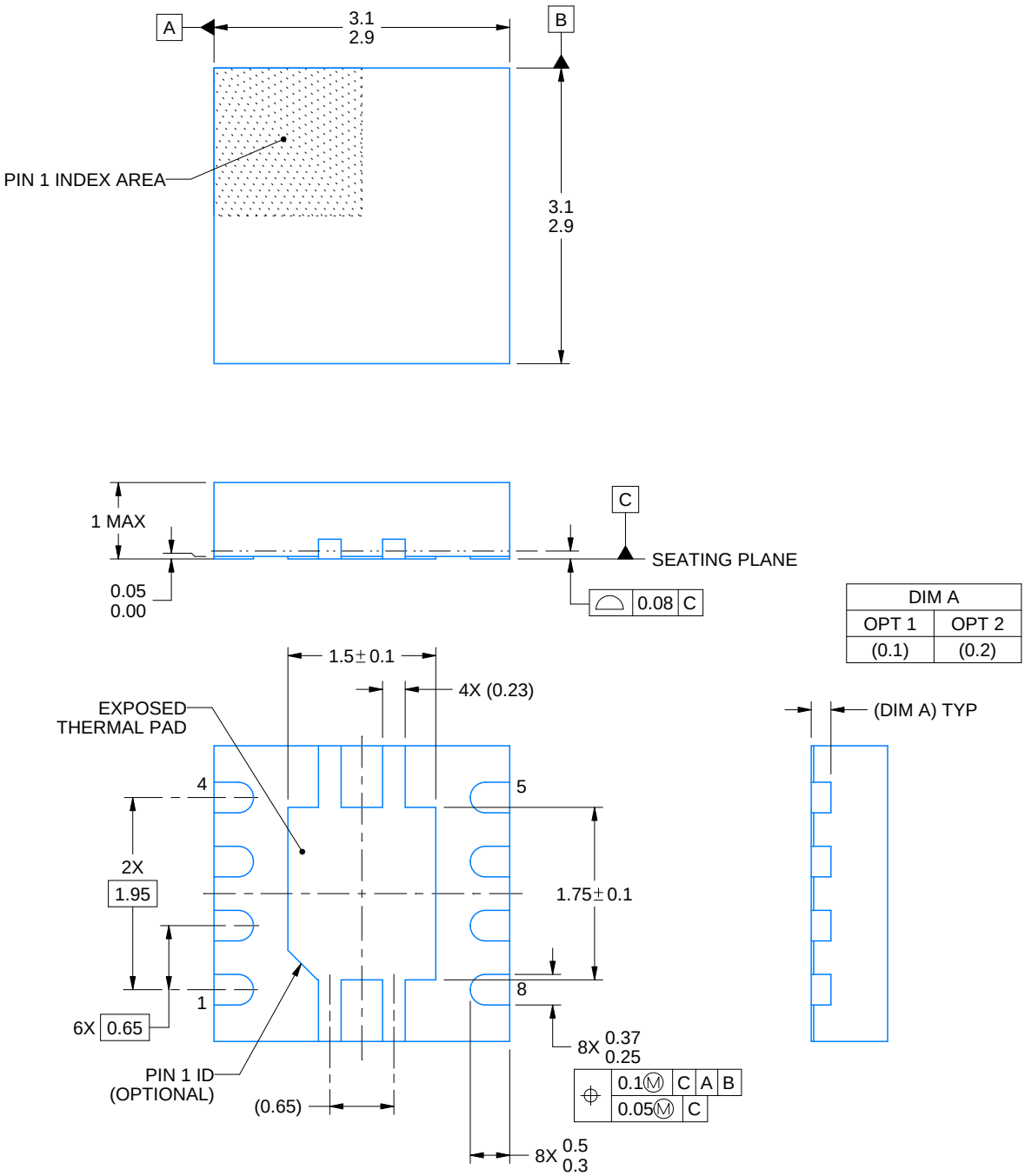
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

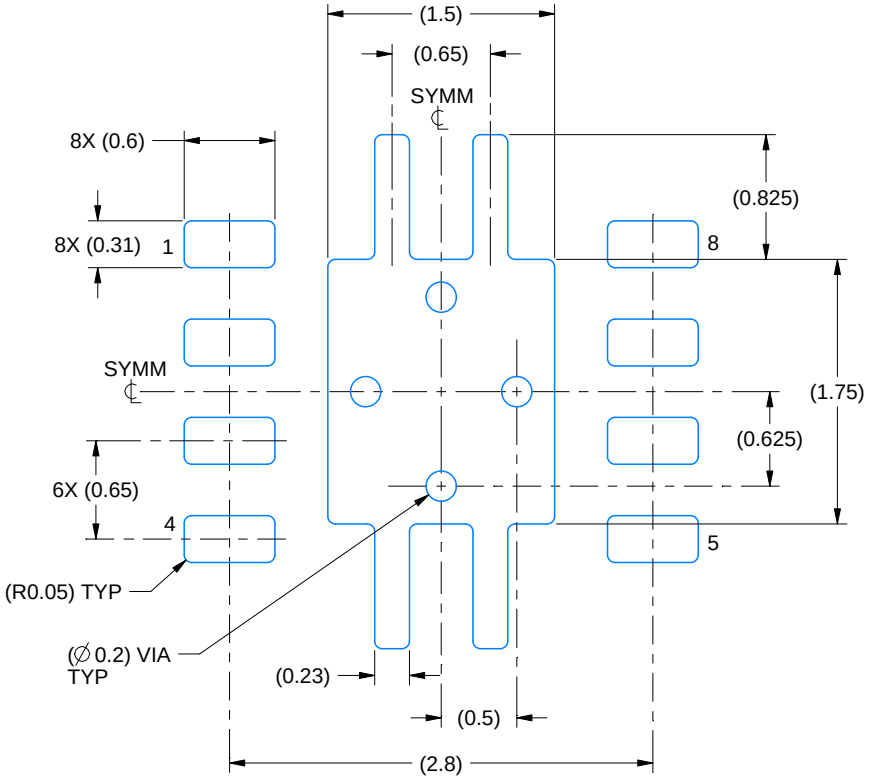
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

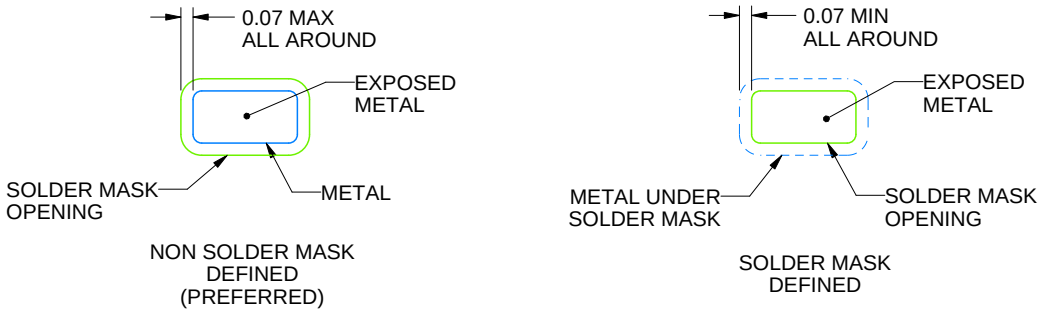
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

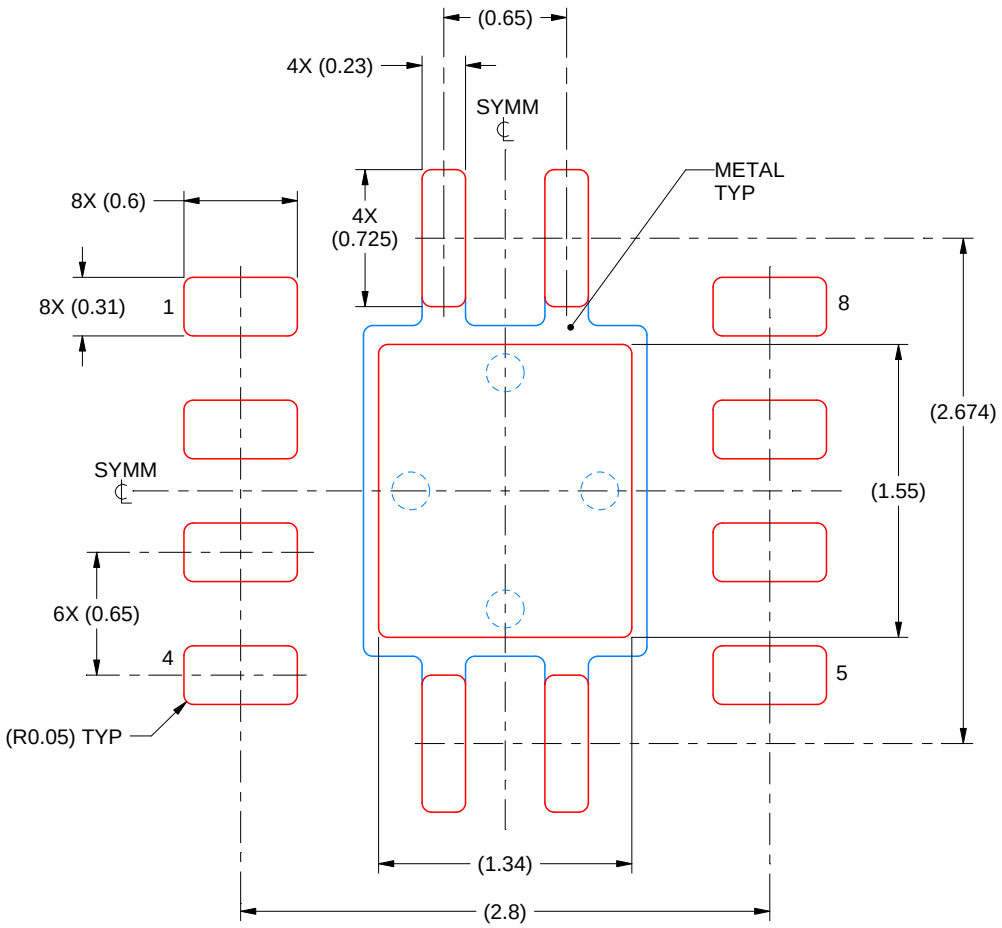


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

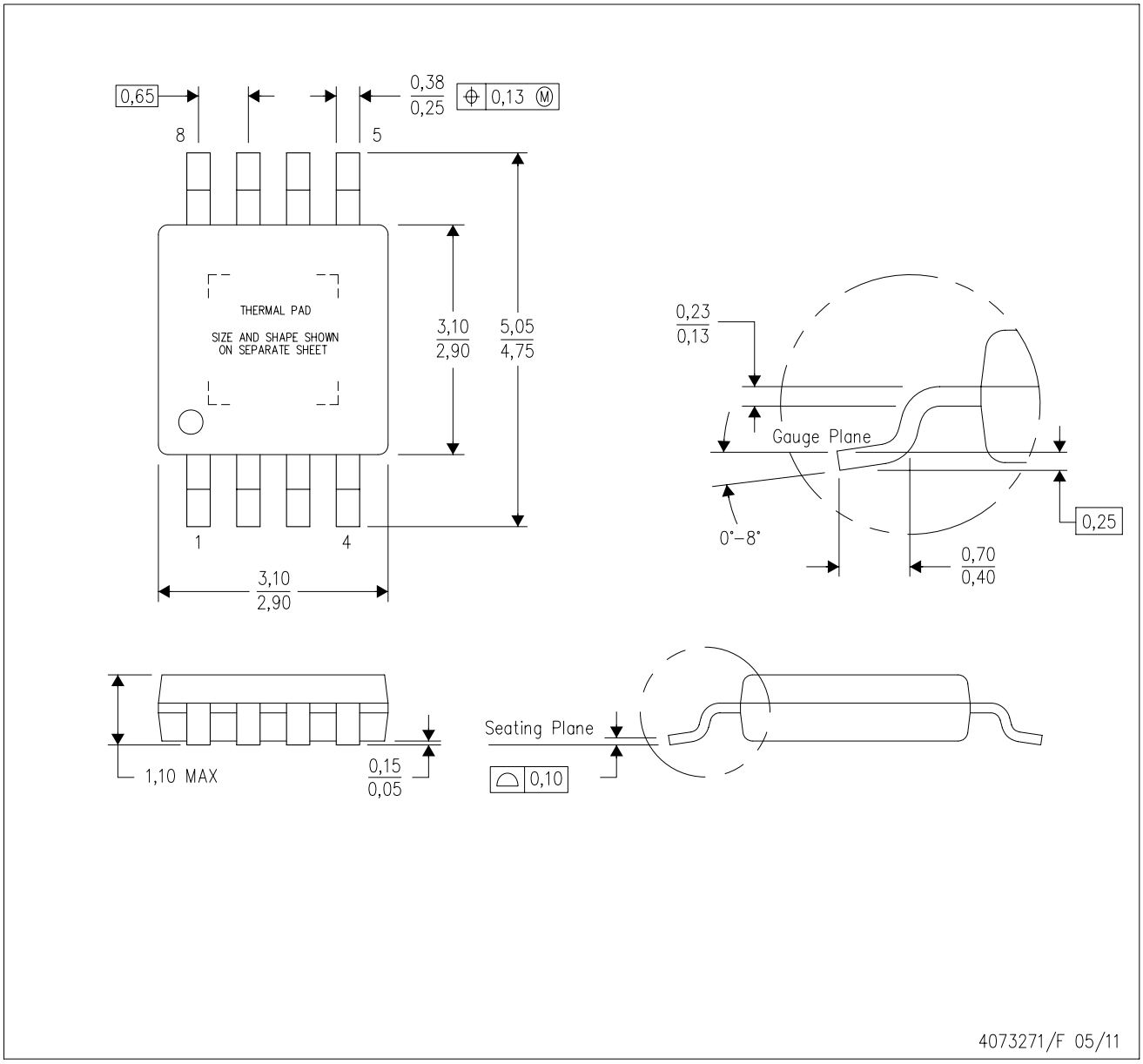
EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

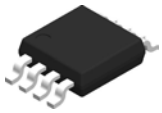


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

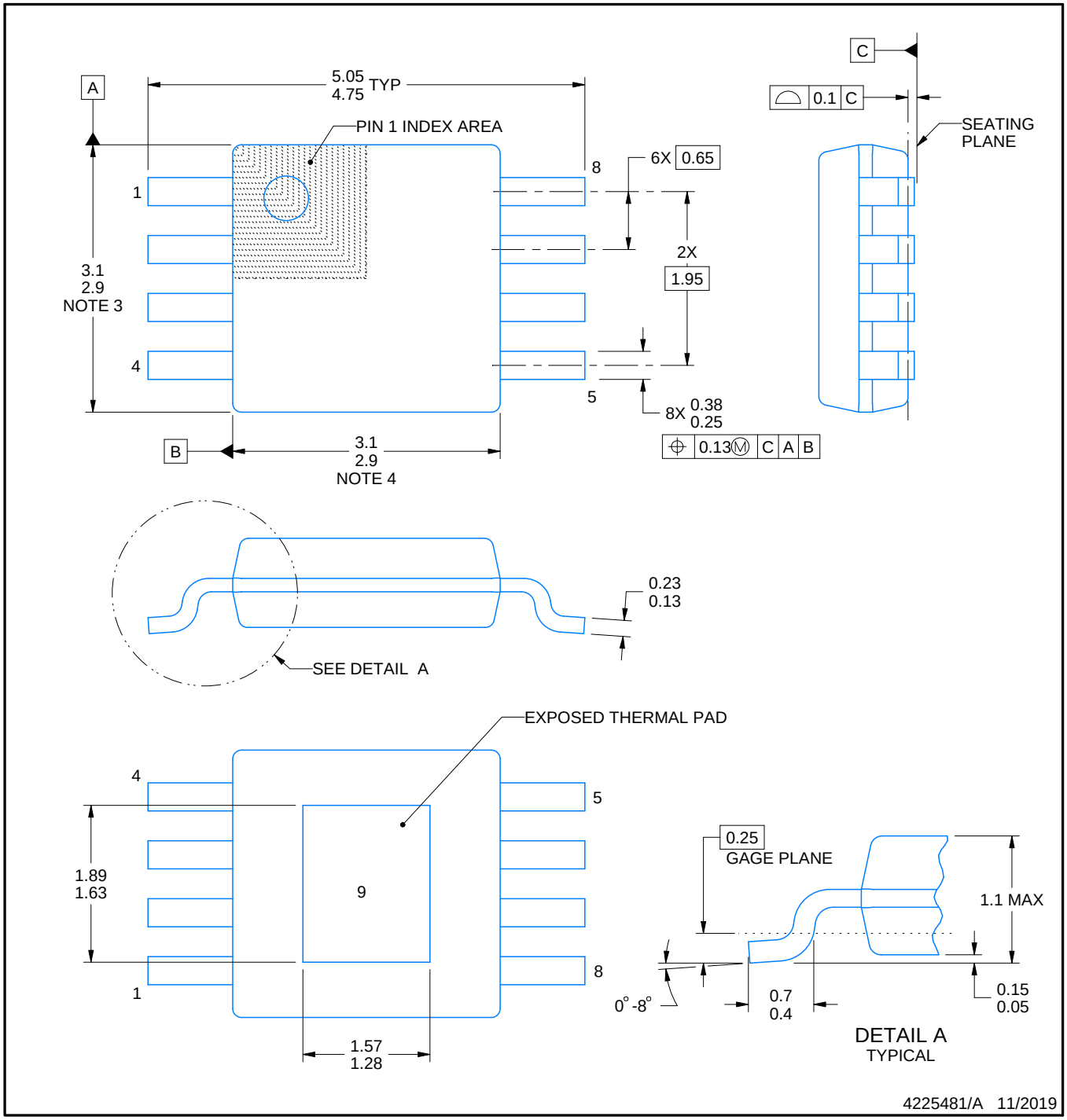
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

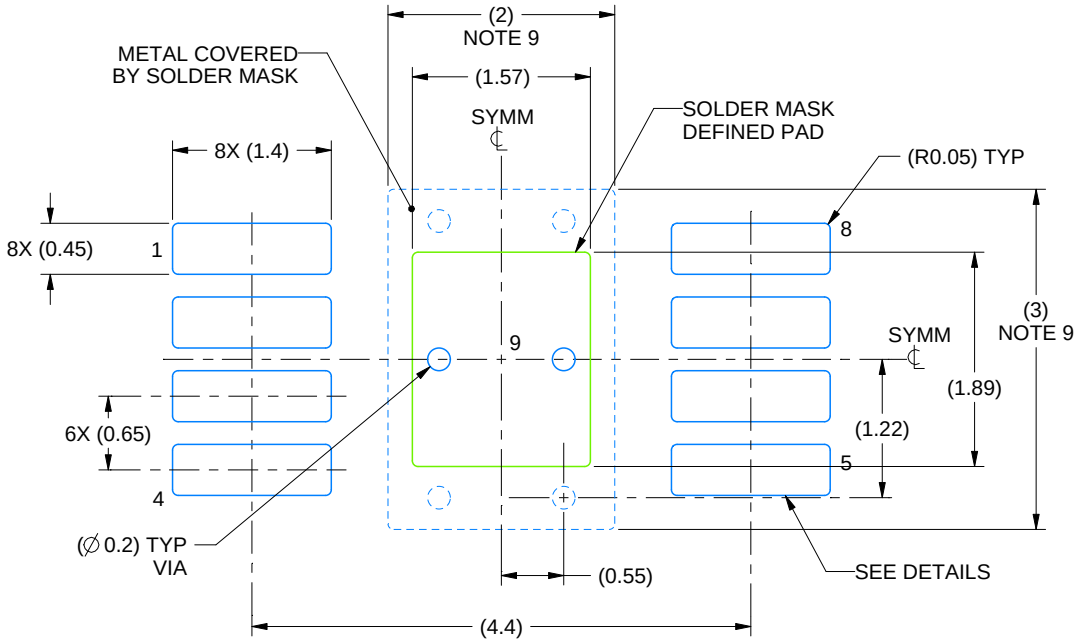
SMALL OUTLINE PACKAGE



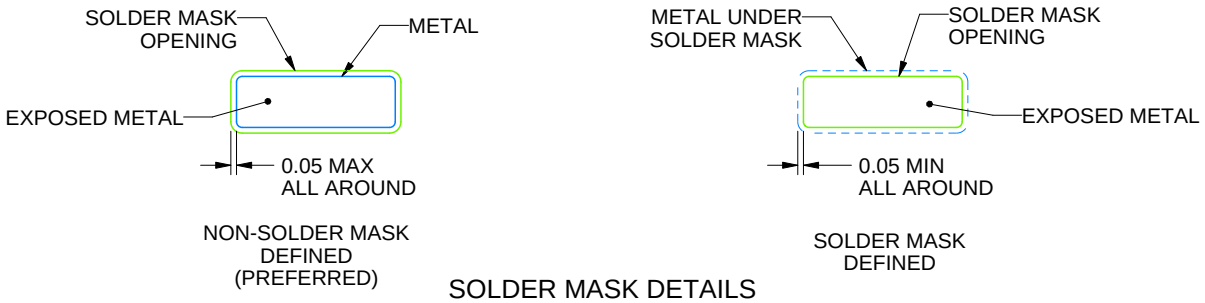
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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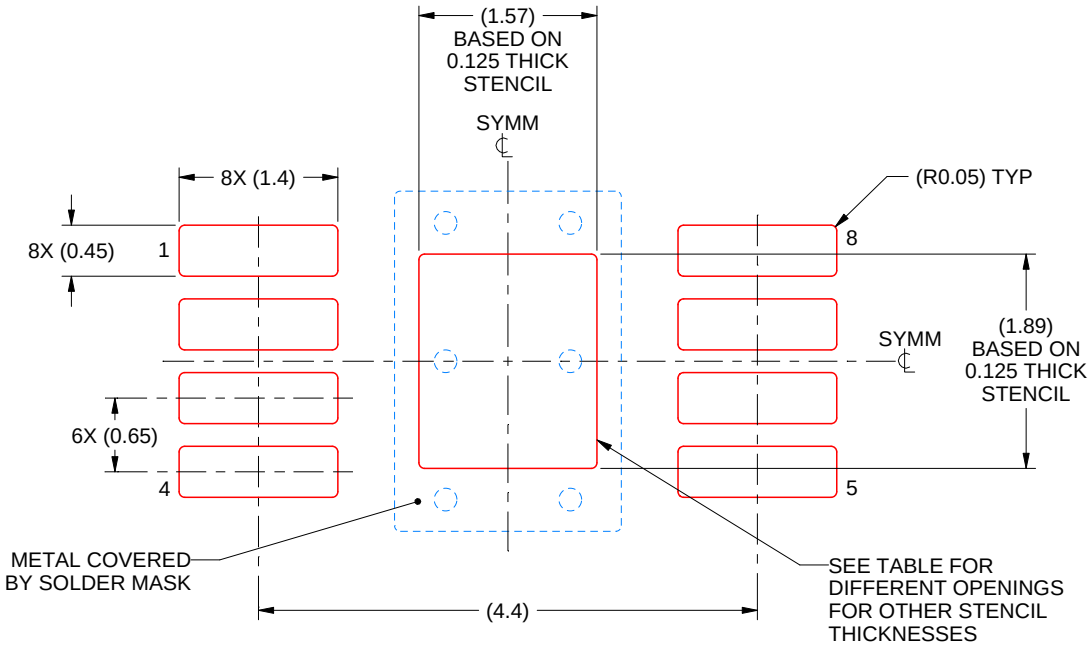
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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