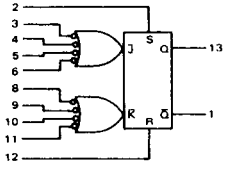
85-MHz AC-COUPLED
J-$\bar{K}$ FLIP-FLOPS

MC1013
MC1213

Designed for use at clock frequencies to 70 MHz minimum (85 MHz typical). Logic performing inputs ($\bar{J}$ and $\bar{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 125 mW typical

R-S TRUTH TABLE

Pin No.	R	S	Q^{n+1}
	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\bar{J}$-$\bar{K}$ inputs are static.
N.D. = Not defined

$\bar{J}_D$ $\bar{K}_D$ TRUTH TABLE

Pin No.	$\bar{J}_D$	$\bar{K}_D$	Q^{n+1}
	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

All other $\bar{J}$-$\bar{K}$ inputs and the R-S inputs are at a "0" level

CLOCKED $\bar{J}$ $\bar{K}$ TRUTH TABLE

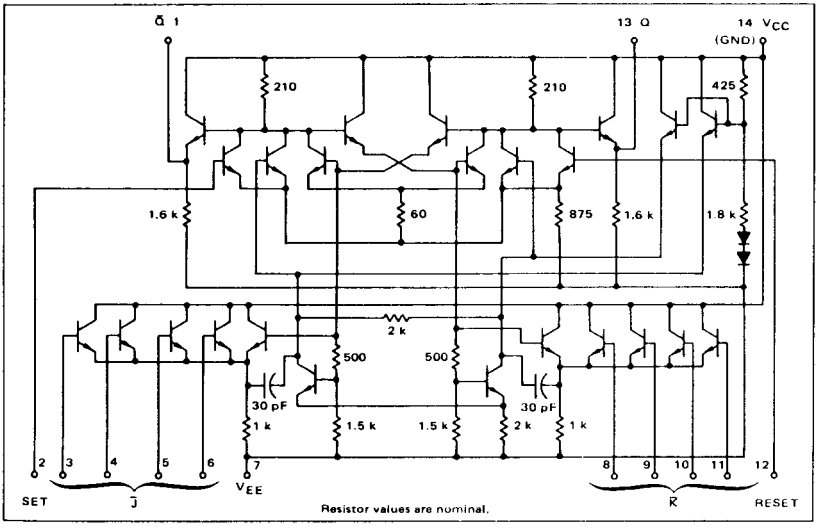
Pin No.	$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^n
	*	*	**	13
	ϕ	ϕ	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All other $\bar{J}$ $\bar{K}$ inputs and the R-S inputs are at a "0" level.
ϕ = Either state will result in the desired output.

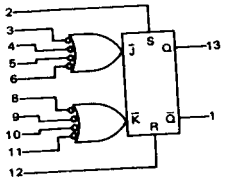
*Any $\bar{J}$ or $\bar{K}$ input, not used for $\bar{C}_D$.
**$\bar{C}_D$ obtained by connecting one $\bar{J}$ and one $\bar{K}$ input together.

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1213 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1013 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	29	-	-	mAdc	-	-	-	29	-	-	mAdc
Input Current	I_{in}	2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		3	-	-	-		-	-		-	-	-		-	-	
		4	-	-	-		-	-		-	-	-		-	-	
		5	-	-	-		-	-		-	-	-		-	-	
		6	-	-	-		-	-		-	-	-		-	-	
		8	-	-	-		-	-		-	-	-		-	-	
		9	-	-	-		-	-		-	-	-		-	-	
		10	-	-	-		-	-		-	-	-		-	-	
		11	-	-	-		-	-		-	-	-		-	-	
		12	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
Input Leakage Current	I_R	Inputs*	-	-	-		-	-		-	-	-		-	-	
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	13	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q̄" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q̄" Logical "0" Output Voltage‡	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q" or "Q̄" Latch Voltage	V_L	2	-1.34	-1.16	-1.21	-1.09	-1.07	-0.93	Vdc	-1.25	-1.11	-1.21	-1.09	-1.14	-1.02	Vdc
		12	-1.34	-1.16	-1.21	-1.09	-1.07	-0.93	Vdc	-1.25	-1.11	-1.21	-1.09	-1.14	-1.02	Vdc
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	-	-	70	-	-	-	MHz	-	-	70	-	-	-	MHz
Sensitivity (No Toggle)	-	1	←		See Figure 1			→		←		See Figure 1			→	
		13	←		See Figure 1			→		←		See Figure 1			→	
Sensitivity (Toggle)	-	1, 13	←		See Figure 2			→		←		See Figure 2			→	
Switching Times ④			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{6+1+}	1	6.0	8.5	6.0	8.5	8.0	10.5	ns	6.0	8.5	6.0	8.5	6.5	9.0	ns
	t_{6+1-}	1					7.5									
	t_{8+13+}	13					8.0									
	t_{8+13-}	13					7.5									
Rise Time	t_{1+}	1	4.0	7.5	4.0	7.5	5.5	9.5		4.0	7.5	4.0	7.5	5.0	8.0	
	t_{13+}	13	4.0		4.0		5.5	9.5		4.0		4.0			8.0	
Fall Time	t_{1-}	1	5.0		5.0		7.5	10		5.0		5.0			8.5	
	t_{13-}	13	5.0		5.0		7.5	10		5.0		5.0			8.5	

* Individually test each input using the pin connections shown.

‡ V_{OH} limits apply from no load (0 mA) to full load (−2.5 mA).

① $V_{in(set)}$: V_{OH} then $V_{OL(max)}$.

② $V_{in(reset)}$: V_{OH} then $V_{OL(max)}$.

③ Input voltage is adjusted to obtain $dV_{-}/dV_{in} = *$.

④ AC fan-out = 3

	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc		
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L		
MC1213	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	2.5		
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	2.5		
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	2.5		
MC1013	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	2.5		
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	2.5		
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	2.5		

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	dV_{in}	V_{cc} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
Input Current	I_{in}	2	-	-	2	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
		3	-	-	3	2, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	
		4	-	-	4	2, 3, 5, 6, 7, 8, 9, 10, 11, 12	-	-	
		5	-	-	5	2, 3, 4, 6, 7, 8, 9, 10, 11, 12	-	-	
		6	-	-	6	2, 3, 4, 5, 7, 8, 9, 10, 11, 12	-	-	
		8	-	-	8	2, 3, 4, 5, 6, 7, 9, 10, 11, 12	-	-	
		9	-	-	9	2, 3, 4, 5, 6, 7, 8, 10, 11, 12	-	-	
		10	-	-	10	2, 3, 4, 5, 6, 7, 8, 9, 11, 12	-	-	
		11	-	-	11	2, 3, 4, 5, 6, 7, 8, 9, 10, 12	-	-	
		12	-	-	12	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	
Input Leakage Current	I_R	Inputs*	-	-		2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-	-	2①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	13	-	14
"Q" Logical "0" Output Voltage	V_{OL}	13	-	-	12②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	14
"Q̄" Logical "1" Output Voltage‡	V_{OH}‡	1	-	-	12②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1	-	14
"Q̄" Logical "0" Output Voltage	V_{OL}	1	-	-	2①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" or "Q̄" Latch Voltage	V_L	2	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	2③	14
		12	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	12③	14
Input Toggle Frequency (See Figures 3 & 4)	f_{TOG}	13	Pulse In 6, 8	Pulse Out 13	-	V_{EE} = −4.0 Vdc 2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	(+1.2V) 14
Sensitivity (No Toggle)	-	1	6, 8	1	-	↓	↓	↓	↓
		13	6, 8	13	-				
Sensitivity (Toggle)	-	1, 13	6, 8	1, 13	-				
Switching Times ④									
Propagation Delay	t_{6+1+}	1	6	1	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
	t_{6+1-}	1	6	1	-	↓	↓	↓	↓
	t_{8+13+}	13	8	13	-				
	t_{8+13-}	13	8	13	-				
Rise Time	t_{1+}	1	6	1	-				
	t_{13+}	13	8	13	-				
Fall Time	t_{1-}	1	6	1	-				
	t_{13-}	13	8	13	-	↓	↓	↓	↓

14/C/

FIGURE 1 - SENSITIVITY (NO TOGGLE)

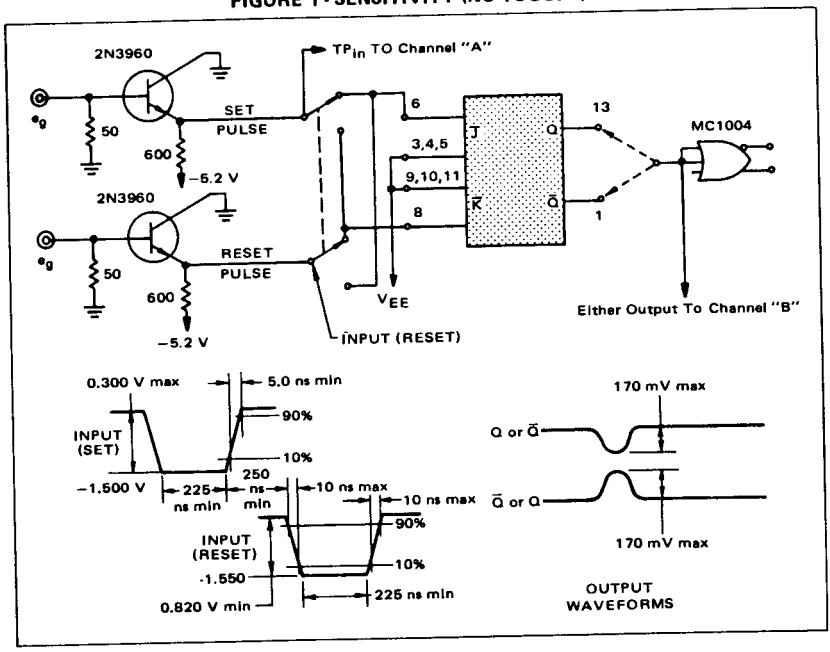
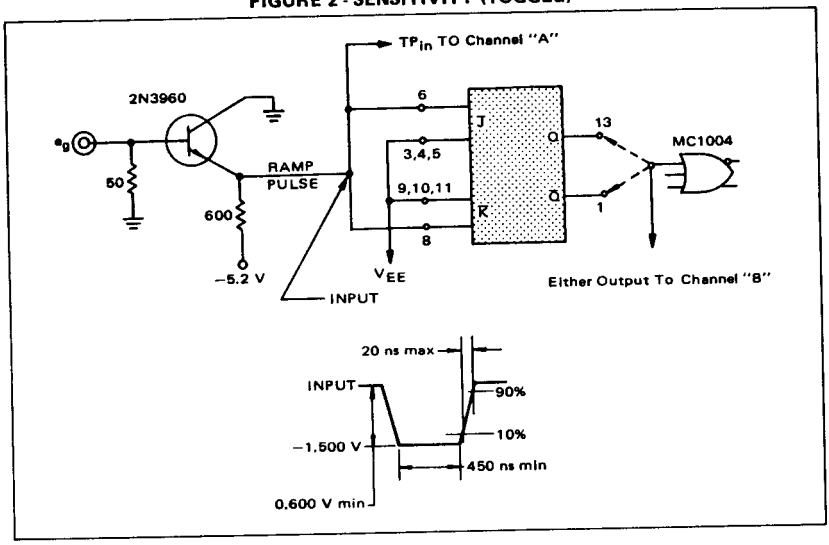
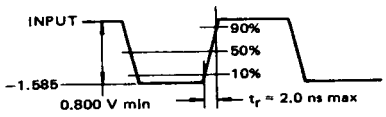


FIGURE 2 - SENSITIVITY (TOGGLE)



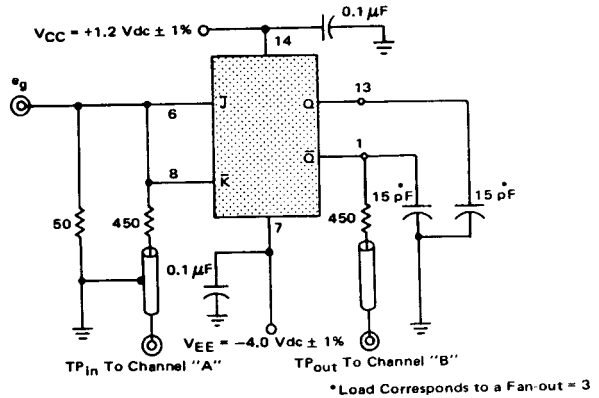
145

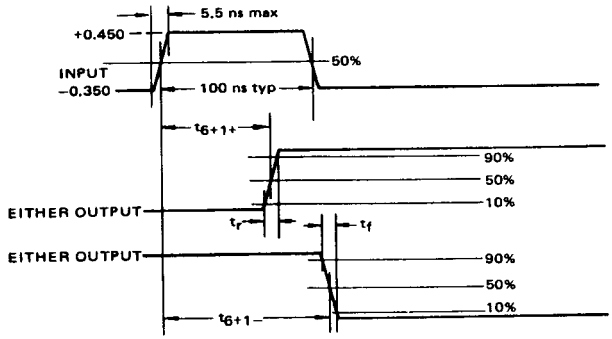


Input Frequency = 70 MHz @ 50% Duty Cycle
Output Frequency = 1/2 Input Frequency

FIGURE 3 - INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C





APPLICATIONS INFORMATION

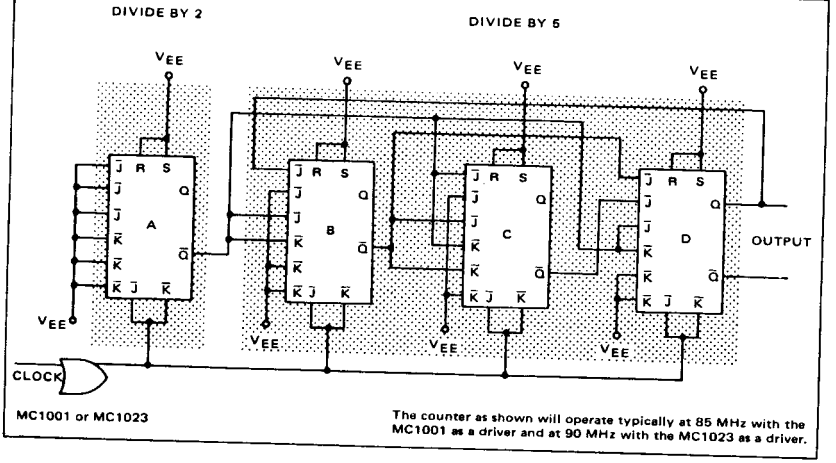
The MC1013/MC1213 $\overline{J}$-$\overline{K}$ flip-flop is used in both counter and shift register applications. Typically the flip-flop will shift and toggle at 85 MHz. Flip-flop operation is illustrated by the curves shown on page 2-125. For a complete characterization of the device, refer to Application Note AN-280. Circuit operation is essentially the same as the MC314/MC364 flip-flop which is explained in Application Note AN-244. Due to the four $\overline{J}$ and four $\overline{K}$ inputs, many clocked and ripple through counters may be built without additional logic. Figure 5 is a table illustrating the $\overline{J}$ and $\overline{K}$ input equations for clocked counters, divide by 3 through 10. Figure 6 is a clocked BCD counter utilizing the logic equations shown in the table.

FIGURE 5 - INPUT EQUATIONS FOR CLOCKED COUNTERS

Divide By:	$\overline{J}_A$	$\overline{K}_A$	$\overline{J}_B$	$\overline{K}_B$	$\overline{J}_C$	$\overline{K}_C$	$\overline{J}_D$	$\overline{K}_D$
3	B	0	$\overline{A}$	0	..	..	..	..
4	0	0	$\overline{A}$	$\overline{A}$	..	..	..	..
5	C	0	$\overline{A}$	$\overline{A}$	$\overline{A+B}$	0	..	..
6	0	0	$\overline{A+C}$	$\overline{A}$	$\overline{A+B}$	$\overline{A}$	..	..
7	BC	0	$\overline{A}$	$\overline{A+C}$	$\overline{A+B}$	$\overline{B}$	..	..
8	0	0	$\overline{A}$	$\overline{A}$	$\overline{A+B}$	$\overline{A+B}$	..	..
9	D	0	$\overline{A}$	$\overline{A}$	$\overline{A+B}$	$\overline{A+B}$	$\overline{A+B+C}$	0
10	0	0	$\overline{A+D}$	$\overline{A}$	$\overline{A+B}$	$\overline{A+B}$	$\overline{A+B+C}$	$\overline{A}$

0 (logic zero) ≤ -1.6 V (pin usually tied to V_{EE}).
All but $\div 7$ may be obtained without additional gating.
All $\overline{J}$ inputs and all $\overline{K}$ inputs are ORed together.

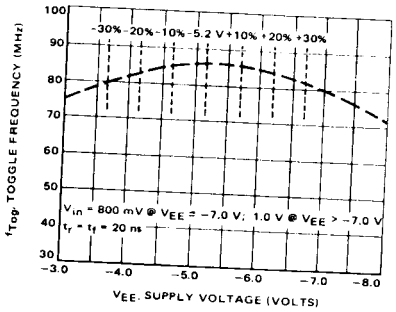
FIGURE 6 - CLOCKED BCD COUNTER USING MECL $\overline{J}$-$\overline{K}$ FLIP-FLOPS



The counter as shown will operate typically at 85 MHz with the MC1001 as a driver and at 90 MHz with the MC1023 as a driver.

147

FIGURE 7 - TYPICAL TOGGLE FREQUENCY versus V_{EE}



ALL UNUSED INPUTS RETURNED TO V_{EE}.
V_{EE} = −5.2 V, V_{in} = 800 mV, T_A = 25°C unless otherwise noted.
——— WORST CASE - - - - - TYPICAL

FIGURE 8 - TYPICAL AND WORST CASE TOGGLE FREQUENCY versus AMBIENT TEMPERATURE

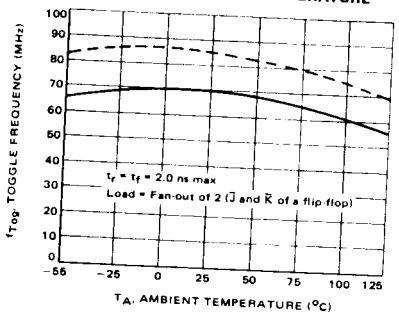


FIGURE 9 - AMPLITUDE versus RISE TIME TO INSURE TOGGLE

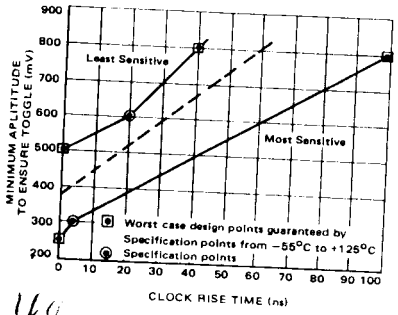


FIGURE 10 - TIME TO DOMINATE

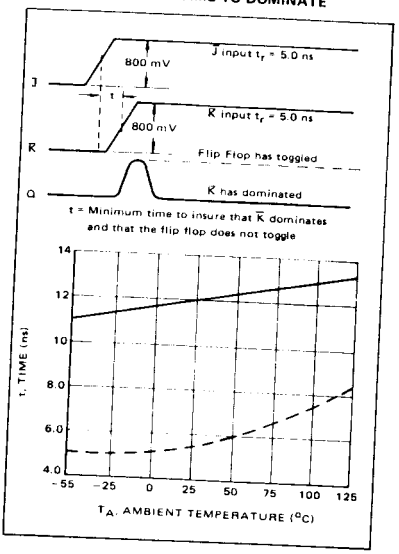


FIGURE 11 - PROPAGATION DELAY TIMES, RISE TIME, FALL TIME versus TEMPERATURE