April 1995
Edition 2.0

FUJITSU

DATA SHEET

MB1511 ASSP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

DESCRIPTION

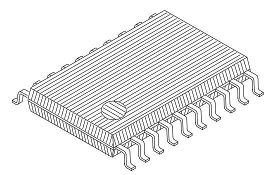
The Fujitsu MB1511 is a single chip serial input PLL frequency synthesizer designed for VHF tuner and cellular telephone applications.

It contains a 1.1 GHz dual modulus prescaler which enables pulse swallow function, and an analog switch to speed up lock up time.

It operates supply voltage of 3.0 V typ. and dissipates 7 mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

FEATURES

- Low power supply voltage: V_{CC} = 2.7 to 5.5 V
- High operating frequency: $f_{IN\ MAX}$ = 1.1 GHz ($P_{IN\ MIN}$ = –10dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC} = 7 mA typ.
- Serial input 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter: 0 to 127
  Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 8 to 16383
  1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2 types of phase detector output
  On-chip charge pump (Bipolar type)
  Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 20-pin Plastic Shrink Small Outline Package (Suffix: –PFV)



Plastic Package
(FPT-20P-M03)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Power Supply voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output voltage	V_{OUT}	–0.5 to V_{CC}+0.5	V
Open-drain voltage	V_{OOP}	–0.5 to 8.0	V
Output current	I_{OUT}	± 10	mA
Storage temperature	Tstg	–55 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of theis data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

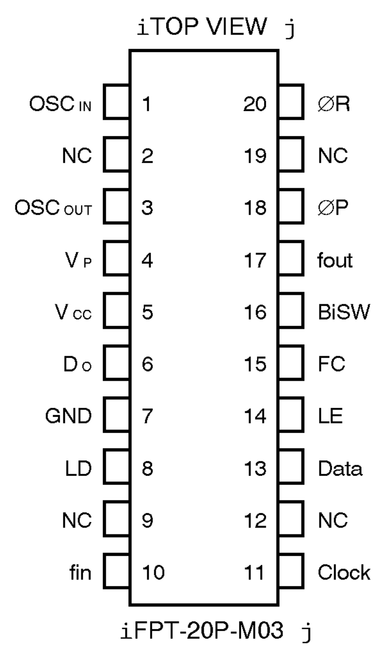
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max	
Power Supply voltage	V_{CC}	2.7	3.0	5.5	V
	V_P	V_{CC}	—	8.0	V
Input voltage	V_{IN}	GND	—	V_{CC}	V
Operating temperature	Ta	–40	—	+85	°C

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handing or transporting PC boards with devices.

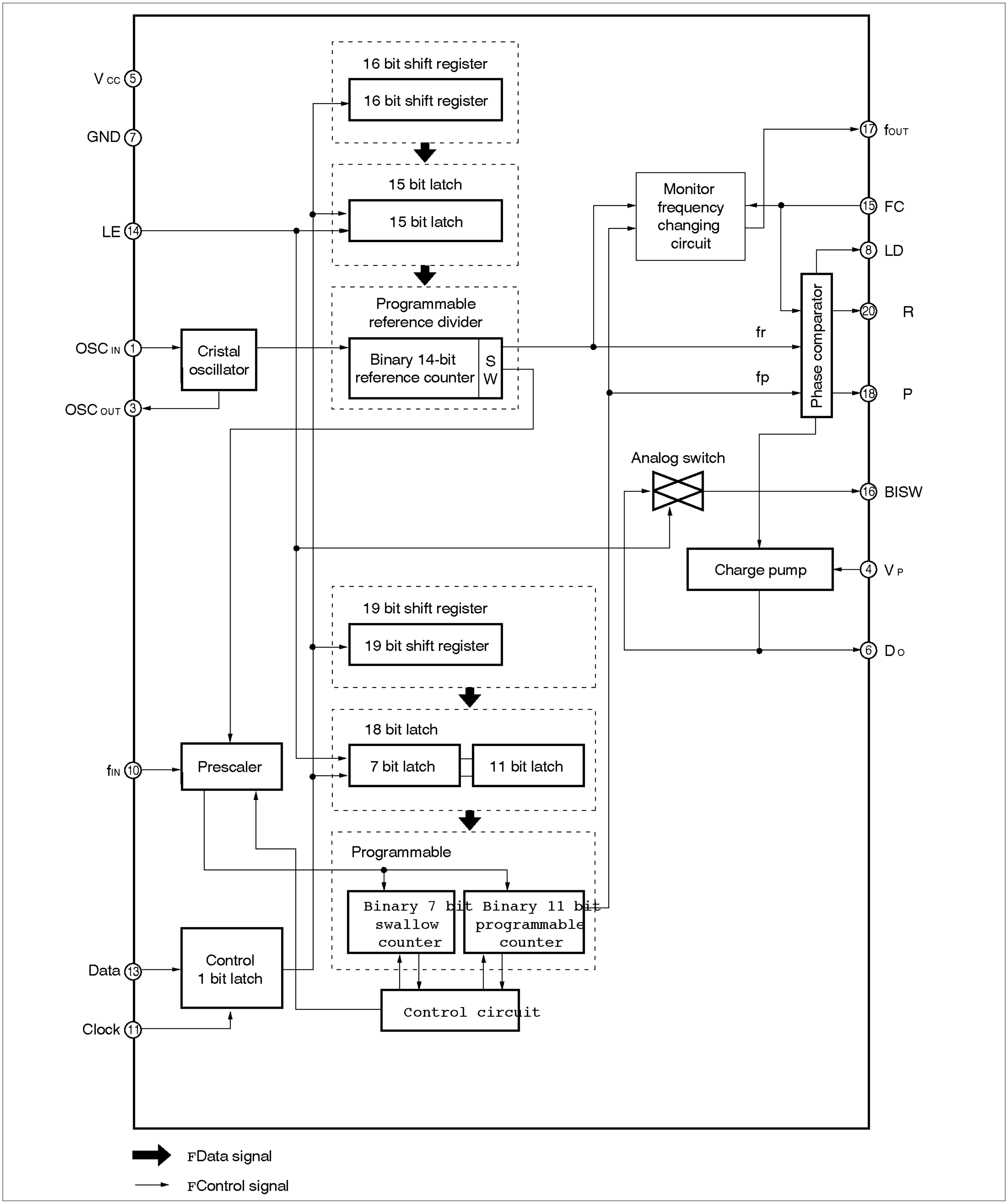
PIN ASSIGNMENT



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Oscillator input. Oscillator output. A crystal is placed between OSCIN and OSCOUT.
3	OSC_{OUT}	O	
4	V_P	—	Power supply input for charge pump and analog switch.
5	V_{CC}	—	Power supply voltage input.
6	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
7	GND	—	Ground.
8	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of fr and fp exists, this pin outputs low level.
10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
11	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
13	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
14	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output is connected to BISW pin because internal analog switch becomes ON state.
15	FC	I	Phase select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal controls fout pin (test pin) output level, fr or fp.
16	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump output.
17	f_{OUT}	O	Minitor pin of phase comparator input. fout pin outputs either programmable reference divider output (fr) or programmable divider output (fp) depending upon FC pin input level. FC = H: It is the same as fr output level. FC = L: It is the same as fp output level.
18	∅P	O	Output for external charge pump. The characteristics are reversed according to FC input.
20	∅R	O	∅P pin is N-channel open drain output.
2, 9 12, 19	NC	—	No connection.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTIONS

1. PULSE SWALLOW FUNCTION

The divide ratio is set using the following equation.

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R$

f_{VCO}	:	Output frequency of external voltage controlled oscillator (VCO)
M	:	Preset modulus of external dual modulus prescaler (64 or 128)
N	:	Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A	:	Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{OSC}	:	Output frequency of the external reference frequency oscillator
R	:	Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

2. SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.

Binary serial data is input to Data pin.

On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.

Control data “H” data is transferred into 15-bit latch.

Control data “L” data is transferred into 18-bit latch.

(1) PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.

Control bit
Divide ratio of prescaler setting bit
LSB
MSB

C	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	S 9	S 10	S 11	S 12	S 13	S 14	S W

Divide ratio of programmable reference counter setting bit

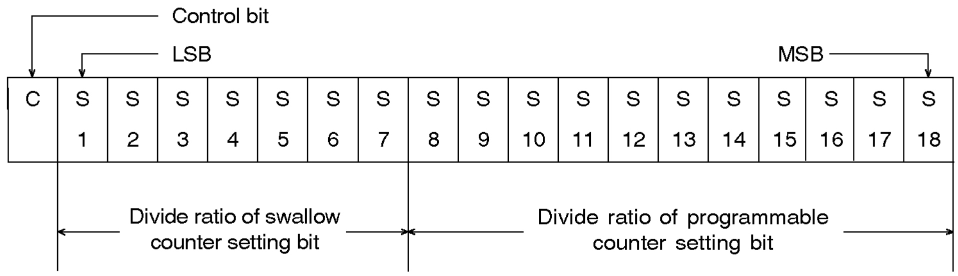
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW = H: 64/65
SW = L: 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

(2) PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown following page.



E7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	1	1	1	1	1	1	1

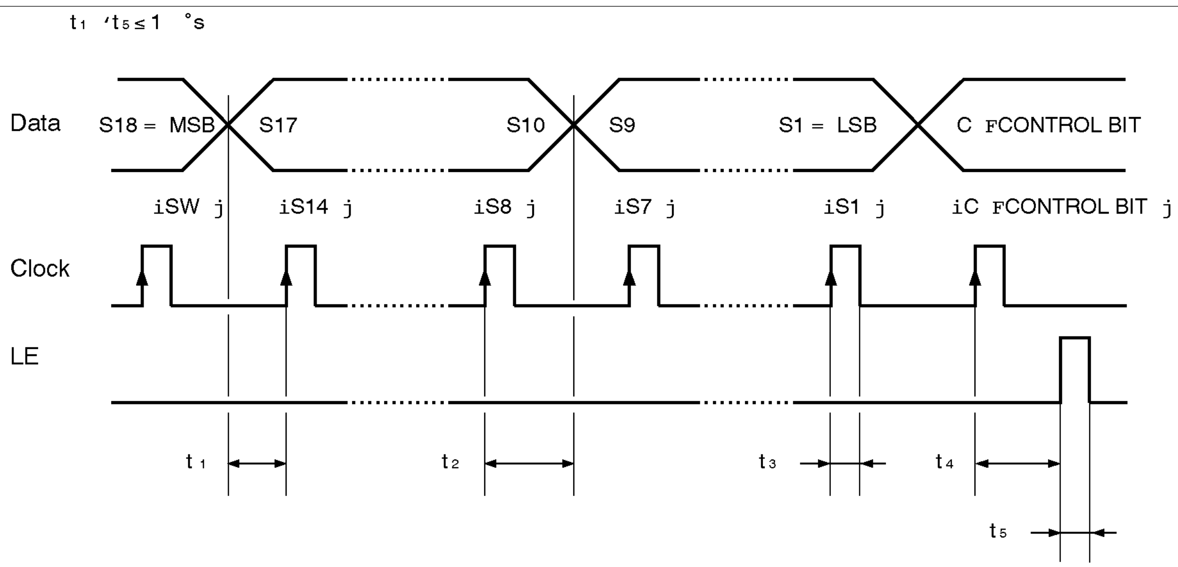
NOTE: Divide ratio: 0 to 127

E11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

3. SERIAL DATA INPUT TIMING



Notes: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

4. PHASE CHARACTERISTICS

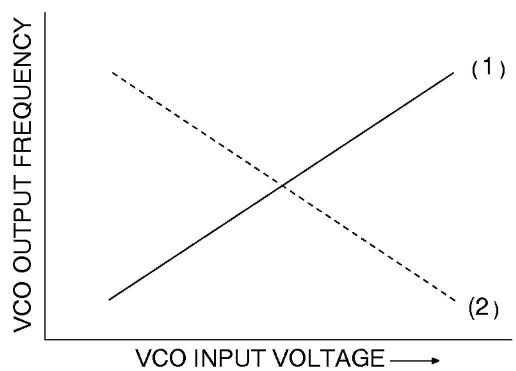
FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (∅R, ∅P) are reversed depending upon FC pin input level. Also, monitor pin (f_{OUT}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, ∅R, ∅P) and FC input level are shown below.

	FC: "H" or open				FC: "L"			
	D_O	∅R	∅P	f_{OUT}	D_O	∅R	∅P	f_{OUT}
fr > fp	H	L	L	(fr)	L	H	Z	(fp)
fr = fp	Z	L	Z	(fr)	Z	L	Z	(fp)
fr < fp	L	H	Z	(fr)	H	L	L	(fp)

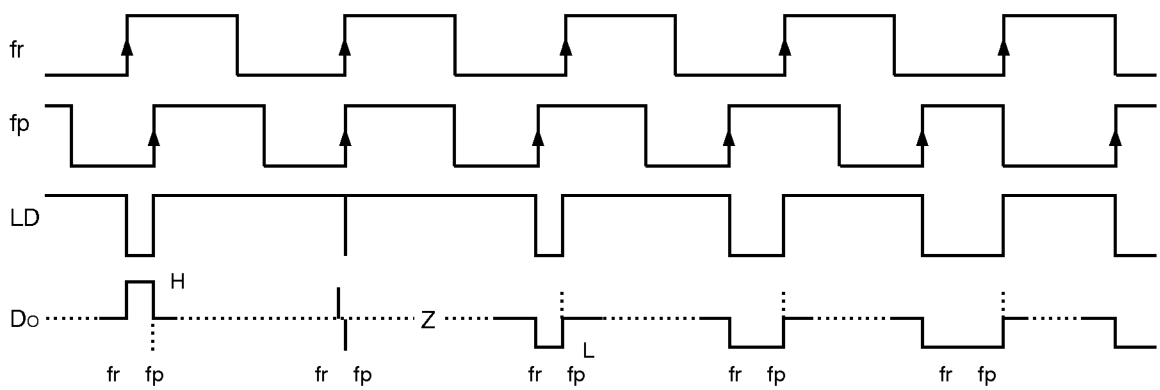
NOTE: Z = (High impedance)

Depending upon VCO characteristics, FC pin should be set accordingly:

When VCO characteristics are like (1),
FC should be set High or open circuit:
When VCO characteristics are like (2)
FC should be set Low.



Phase comparator output waveforms are shown below.



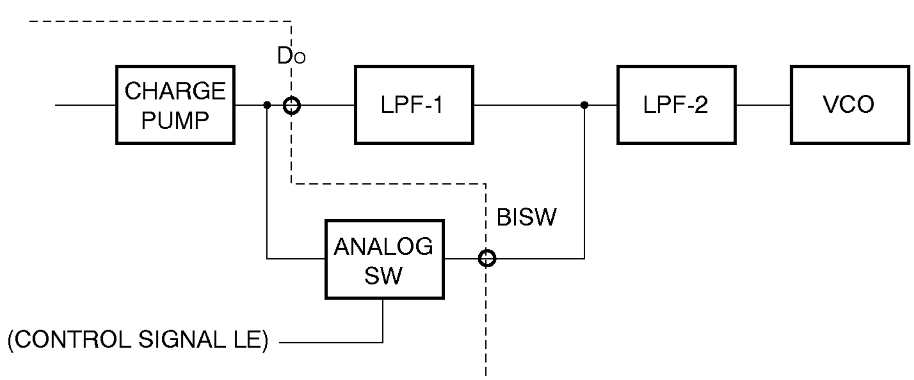
Notes: Phase difference detection range: -2π to +2π
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When fr>fp or fr<fp, spike might not appear depending upon charge rump characteristics.

5. ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (DO) is connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE	Analog Switch
H (Changing the divide ratio of internal prescaler)	ON
L (Normal operating mode)	OFF

When an analog switch is inserted between LP1 and LP2, faster lock up times is achieved to reduce LPF time constant during PLL channal switching.



ELECTRICAL CHARACTERISTICS

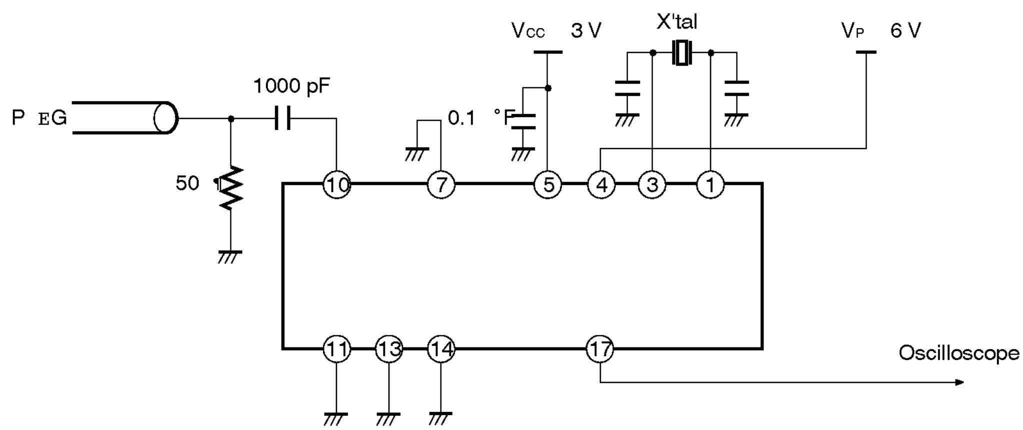
(VCC = 2.7 V to 5.5 V, Ta = -40°C to +85°C)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply current*1		I_{CC}	—	7.0	—	mA
Operating frequency	fin*2	f_{IN}	10	—	1100	MHz
	OSCIN	f_{OSC}	—	12	20	MHz
Input sensitivity	fin-1*3	Pfin1	–4	—	6	dBm
	fin-2*4	Pfin2	–10	—	6	dBm
	OSCIN	V_{OSC}	0.5	—	—	Vp-p
High-level input voltage	Except fin and OSC_{IN}	V_{IH}	VCC×0.7	—	—	V
Low-level input voltage		V_{IL}	—	—	VCC×0.3	V
High-level input current	Data clock	I_{IH}	—	1.0	—	µA
Low-level input current		I_{IL}	—	–1.0	—	µA
Input current	OSC_{IN}	I_{OSC}	—	+50	—	µA
	LE, FC	I_{LE}	—	-60	—	µA
High-level output current	Except DO and OSC_{OUT}	V_{OH}*5	2.2	—	—	V
Low-level output current		V_{OL}	—	—	0.4	V
N-channel open drain cutoff current	DO, ∅p*6	I_{OFF}	—	—	1.1	µA
Output current	Except DO and OSC_{OUT}	I_{OH}	–1.0	—	—	µA
		I_{OL}	1.0	—	—	µA
Analog switch on resistance		R_{ON}	—	50	—	Ω

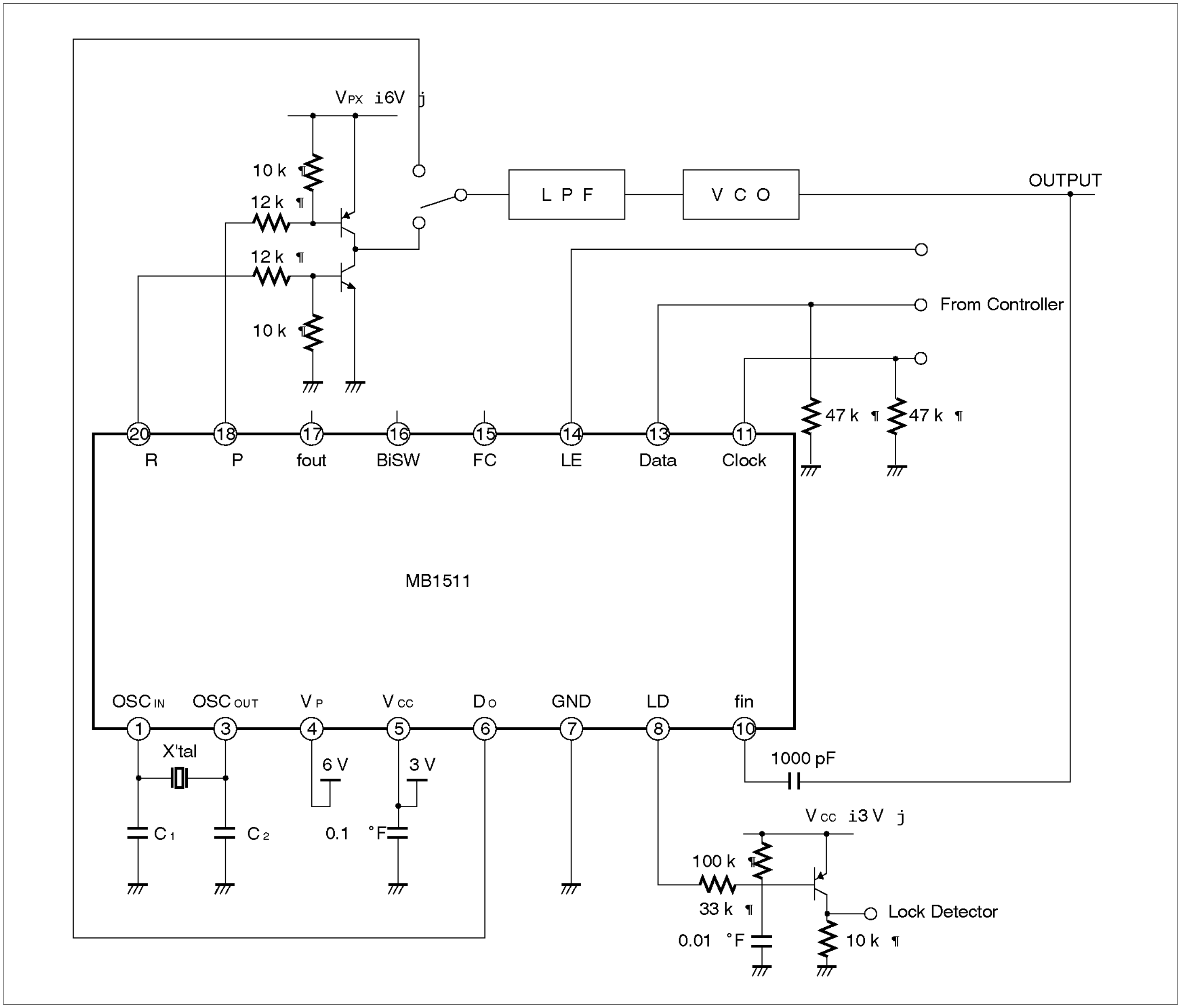
Notes:

1. fin =1.1 GHz, OSCIN=12 MHz, VCC=3V. Inputs are grounded and outputs are open.
2. AC coupling. Minimum operating frequency is measured when a capacitor 1000pF.
3. VCC=4.0 to 5.5V, 50Ω
4. VCC=2.7 to 4.0V, 50Ω
5. VCC=3V
6. VP=VCC to 8V, VOOP=GND to 8V

MEASUREMENT CIRCUIT

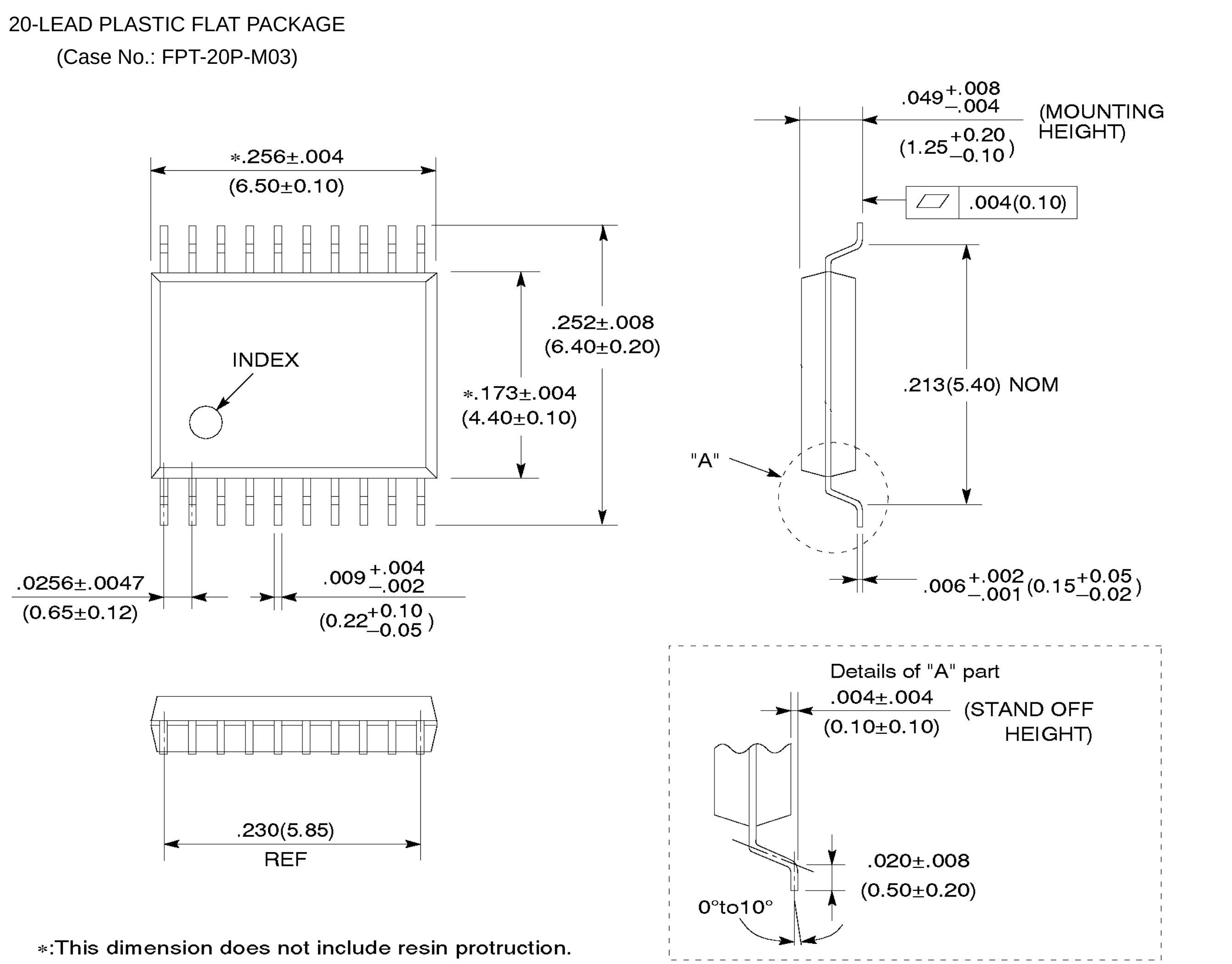


TYPICAL APPLICATION EXAMPLE



VPX, VP	:	8V max.
C1, C2	:	Depends on crystal oscillator
LE, FC	:	With internal pull up resistor
fP	:	Open drain output

PACKAGE DIMENSION



Dimensions in inches (millimeters)

NOTES

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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