

**Document Title**

**128K x8 bit Low Power CMOS Static RAM**

**Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	November 22, 1995	Design target
0.1	First revision - Separate read and write at Icc, Icc1 Icc = Icc1 → Read : 15mA, Write : 35mA	April 15, 1996	Preliminary
1.0	Finalized - Add 70ns speed bin for commercial product and 85ns speed bin for industrial.	September 5, 1996	Final
2.0	Revised - Improved operating current Add typical value. Icc Read : 15mA → 10mA(Remove write current) Icc2 : 90mA → 60mA - Speed bin change Remove 45ns from commercial part Remove 55ns and 100ns from industrial part.	November 5, 1997	Final

Datasheet.Live

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## 128K x8 bit Low Power CMOS Static RAM

### FEATURES

- Process Technology: TFT
- Organization: 128K x8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-DIP-600, 32-SOP-525, 32-TSOP1-0820F/R

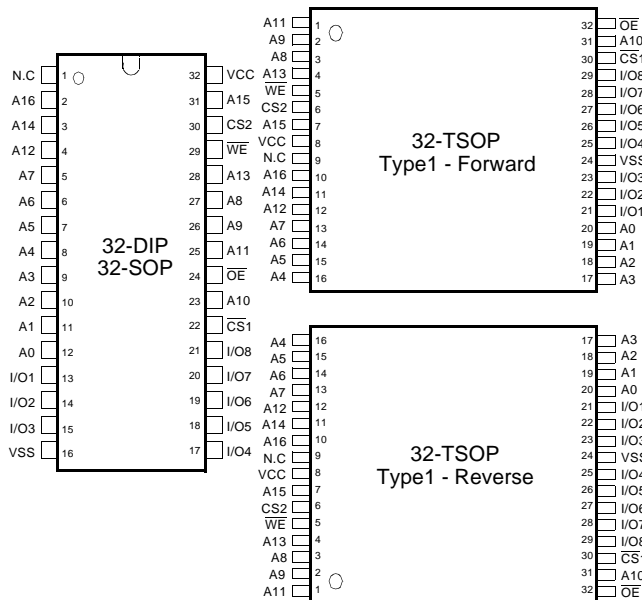
### GENERAL DESCRIPTION

The KM681000C families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

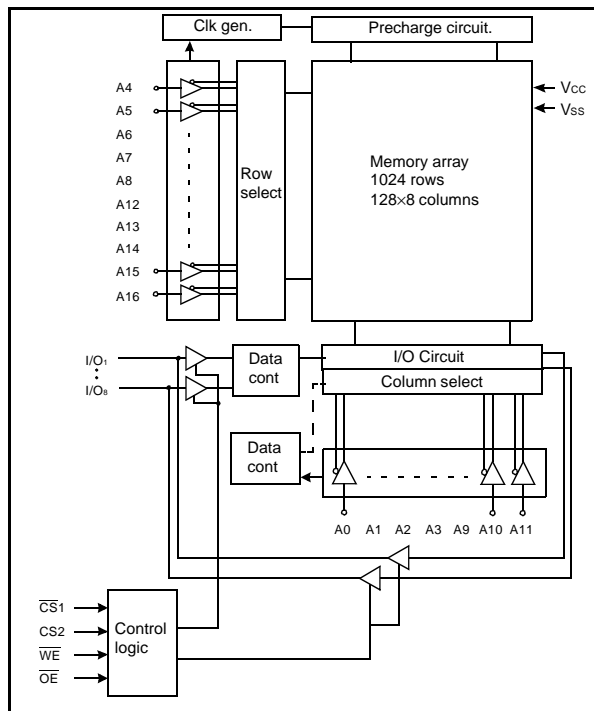
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> , Max)	
KM681000CL KM681000CL-L	Commercial(0~70°C)	4.5~5.5V	55/70ns	50µA 10µA	60mA	32-DIP, 32-SOP 32-TSOP1-F/R
KM681000CLI KM681000CLI-L	Industrial(-40~85°C)		70ns	50µA 15µA		32-SOP 32-TSOP1-F/R

### PIN DESCRIPTION



Name	Function	Name	Function
CS <sub>1</sub> , CS <sub>2</sub>	Chip Select Inputs	I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Inputs/Out-
OE	Output Enable	Vcc	Power
WE	Write Enable	Vss	Ground
A <sub>0</sub> ~A <sub>16</sub>	Address Inputs	N.C	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM681000CLP-5	32-DIP, 55ns, L-pwr	KM681000CLGI-7	32-SOP, 70ns, L-pwr
KM681000CLP-7	32-DIP, 70ns, L-pwr	KM681000CLGI-7L	32-SOP, 70ns, LL-pwr
KM681000CLP-5L	32-DIP, 55ns, LL-pwr	KM681000CLTI-7L	32-TSOP1-F, 70ns, LL-pwr
KM681000CLP-7L	32-DIP, 70ns, LL-pwr		
KM681000CLG-5	32-SOP, 55ns, L-pwr	KM681000CLRI-7L	32-TSOP1-R, 70ns, LL-pwr
KM681000CLG-7	32-SOP, 70ns, L-pwr		
KM681000CLG-5L	32-SOP, 55ns, LL-pwr		
KM681000CLG-7L	32-SOP, 70ns, LL-pwr		
KM681000CLT-5L	32-TSOP1-F, 55ns, LL-pwr		
KM681000CLT-7L	32-TSOP1-F, 70ns, LL-pwr		
KM681000CLR-5L	32-TSOP1-R, 55ns, LL-pwr		
KM681000CLR-7L	32-TSOP1-R, 70ns, LL-pwr		

## FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	$CS_2$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disable	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care(Must be in high or low status.)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.5 to 7.0	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	KM681000CL
		-40 to 85	°C	KM681000CLI
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.5 <sup>3)</sup>	-	0.8	V

Note

1. Commercial Product : T<sub>A</sub>=0 to 70°C and Industrial Product : T<sub>A</sub>=-40 to 85°C, otherwise specified.
2. Overshoot : V<sub>CC</sub>+3.0V for ≤30ns pulse width.
3. Undershoot : -3.0V for ≤30ns pulse width.
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	8	pF

1. Capacitance is sampled not, 100% tested.

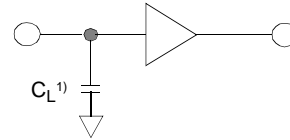
## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , Read	-	5	10	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1 \leq 0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	Read	-	2	5	mA
			Write	-	20	35	
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	45	60	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> , Other input=V <sub>IL</sub> or V <sub>IH</sub>	-	-	3	mA	
Standby Current (CMOS)	KM681000CL	$\overline{CS}_1 \geq V_{CC}-0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V or CS <sub>2</sub> ≤0.2V Other input =0~V <sub>CC</sub>	Low Power	-	1	50	μA
	KM681000CL-L			-	0.3	10	
	KM681000CLI			-	1	50	
	KM681000CLI-L			-	0.3	15	

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.8 to 2.4V  
 Input rising and falling time : 5ns  
 Input and output reference voltage : 1.5V  
 Output load (See right) :  $C_L = 100\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	55	-	70	-	ns
	Address access time	t <sub>AA</sub>	-	55	-	70	ns
	Chip select to output	t <sub>CO1</sub> , t <sub>CO2</sub>	-	55	-	70	ns
	Output enable to valid output	t <sub>OE</sub>	-	25	-	35	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	20	0	25	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	20	0	25	ns
	Output hold from address change	t <sub>OH</sub>	10	-	10	-	ns
Write	Write cycle time	t <sub>WC</sub>	55	-	70	-	ns
	Chip select to end of write	t <sub>CW</sub>	45	-	60	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	45	-	60	-	ns
	Write pulse width	t <sub>WP</sub>	40	-	50	-	ns
	Write recovery time	t <sub>WR1</sub> , t <sub>WR2</sub>	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	20	0	25	ns
	Data to write time overlap	t <sub>DW</sub>	25	-	30	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	ns
End write to output low-Z	t <sub>OW</sub>	5	-	5	-	ns	

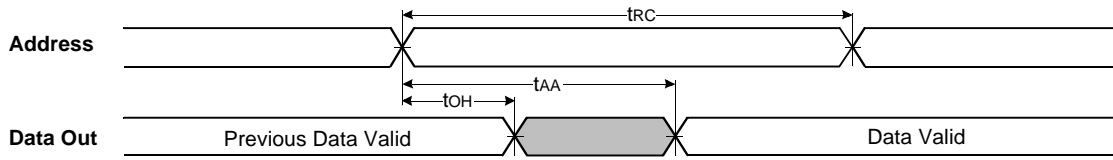
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS}_1 \geq V_{CC} - 0.2V$ , $CS_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$	2.0	-	5.5	V	
Data retention current	I <sub>DR</sub>	$V_{CC} = 3.0V$ , $\overline{CS}_1 \geq V_{CC} - 0.2V$ , $CS_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$	KM681000CL	-	1	20	$\mu A$
			KM681000CL-L	-	1	10	
			KM681000CLI	-	-	25	
			KM681000CLI-L	-	-	10	
Data retention set-up	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms	
Recovery time	t <sub>RDR</sub>		5	-	-		

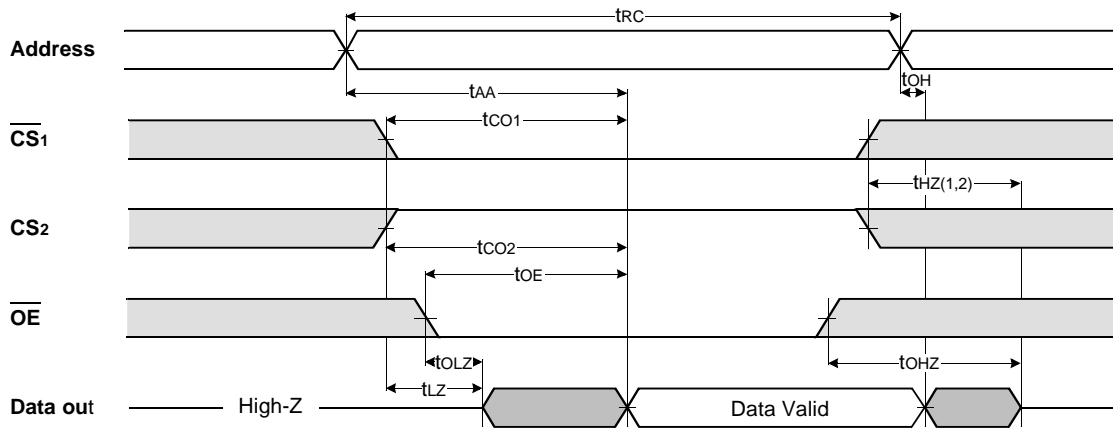
1.  $\overline{CS}_1 \geq V_{CC} - 0.2V$ ,  $CS_2 \geq V_{CC} - 0.2V$  or  $CS_2 \leq 0.2V$

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



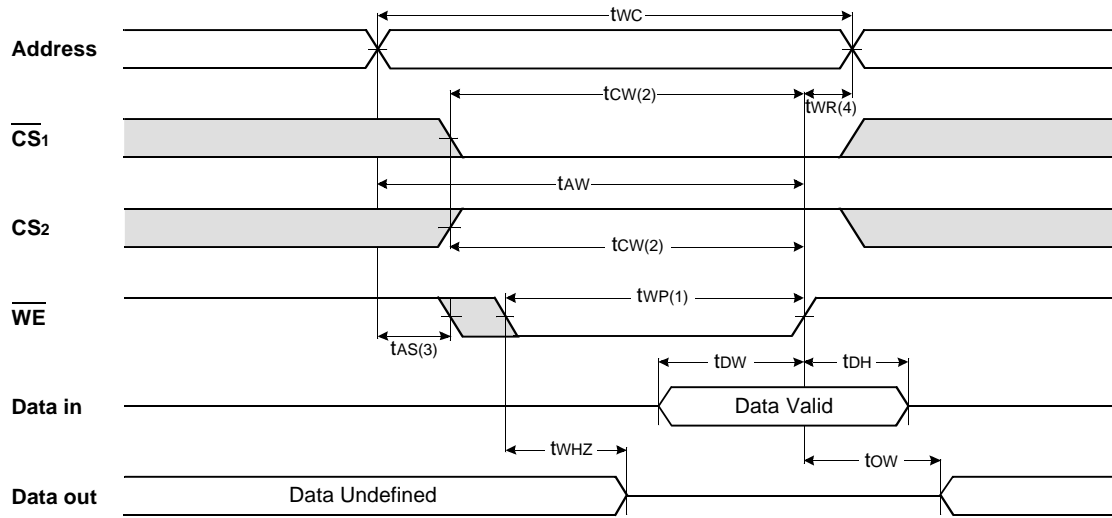
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



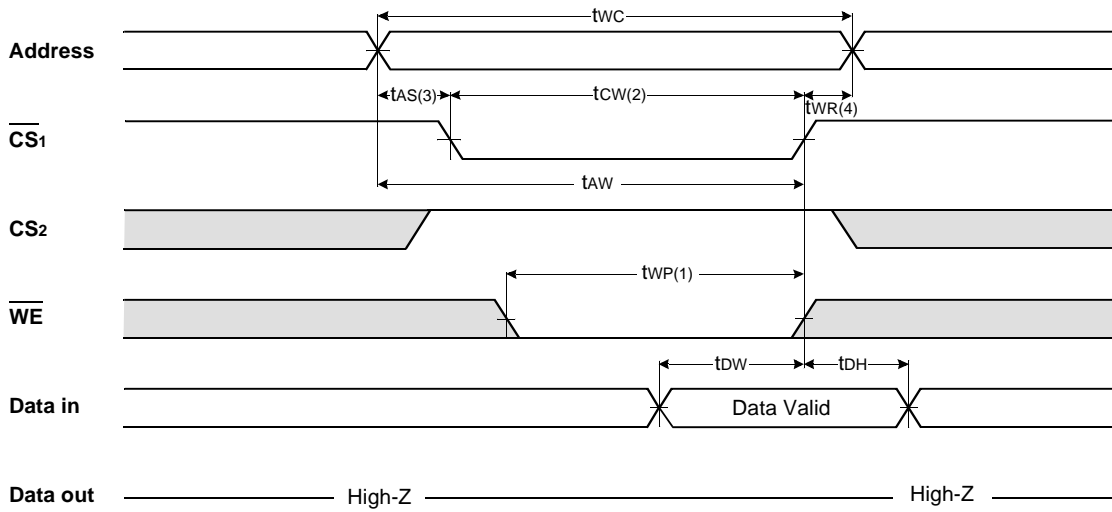
NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

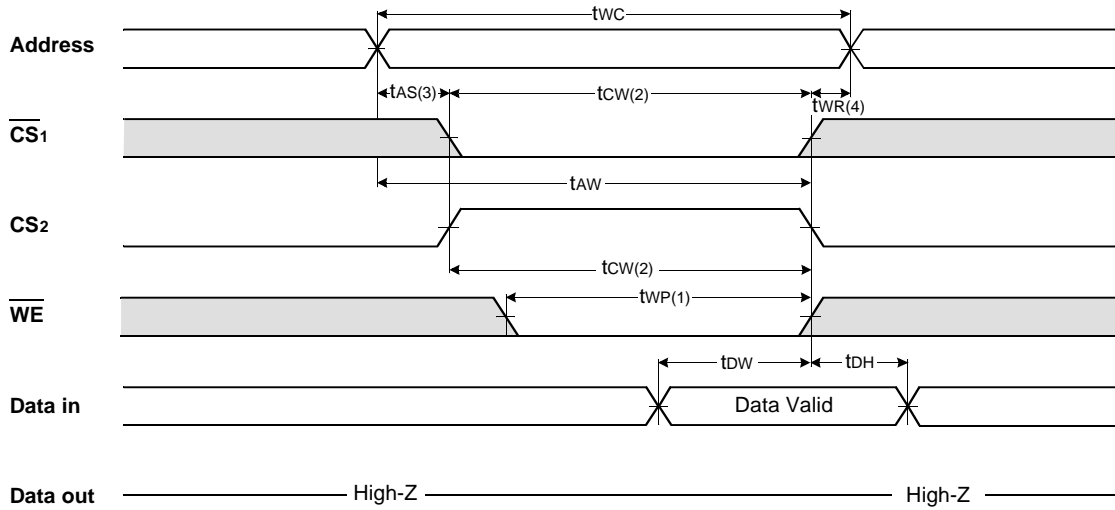
TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

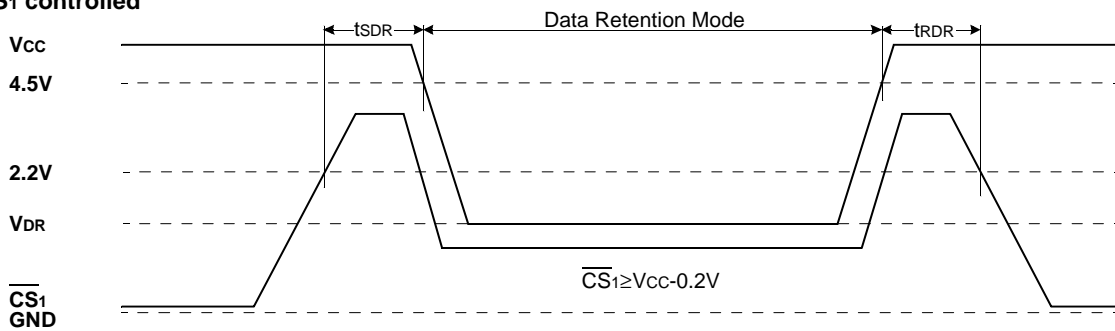


### NOTES (WRITE CYCLE)

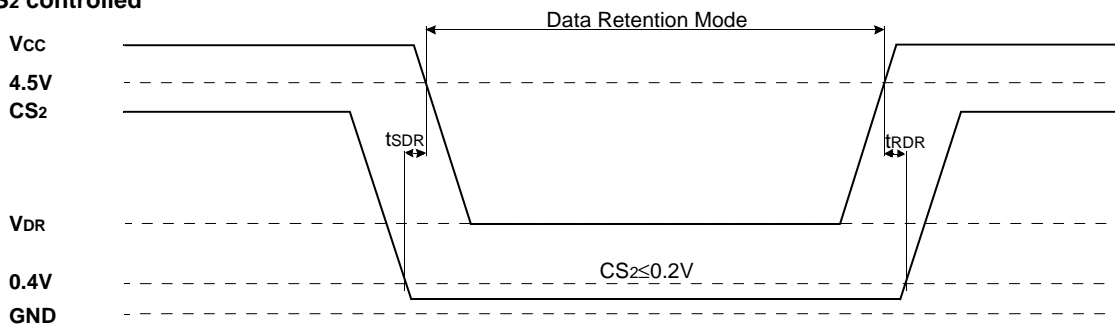
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  going low,  $CS_2$  going high and  $\overline{WE}$  going low : A write ends at the earliest transition among  $\overline{CS}_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR(1)}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR(2)}$  applied in case a write ends as  $CS_2$  going to low.

## DATA RETENTION WAVE FORM

### $\overline{CS}_1$ controlled



### CS<sub>2</sub> controlled

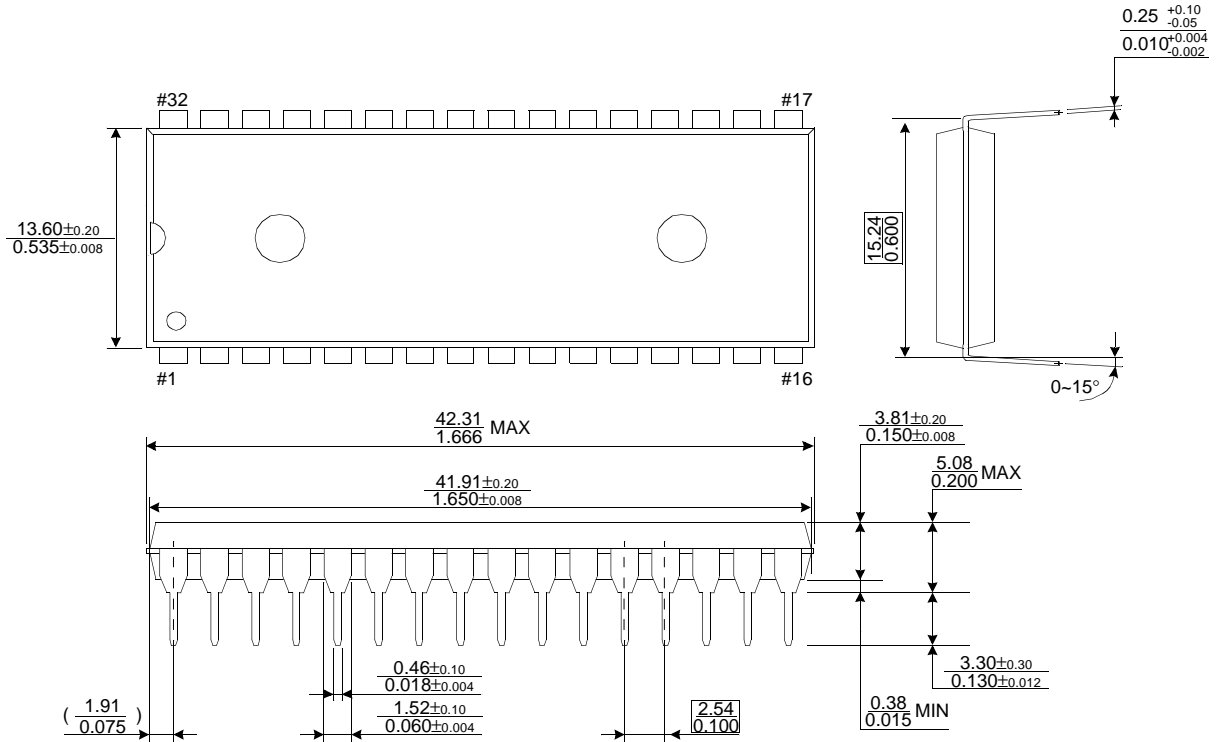




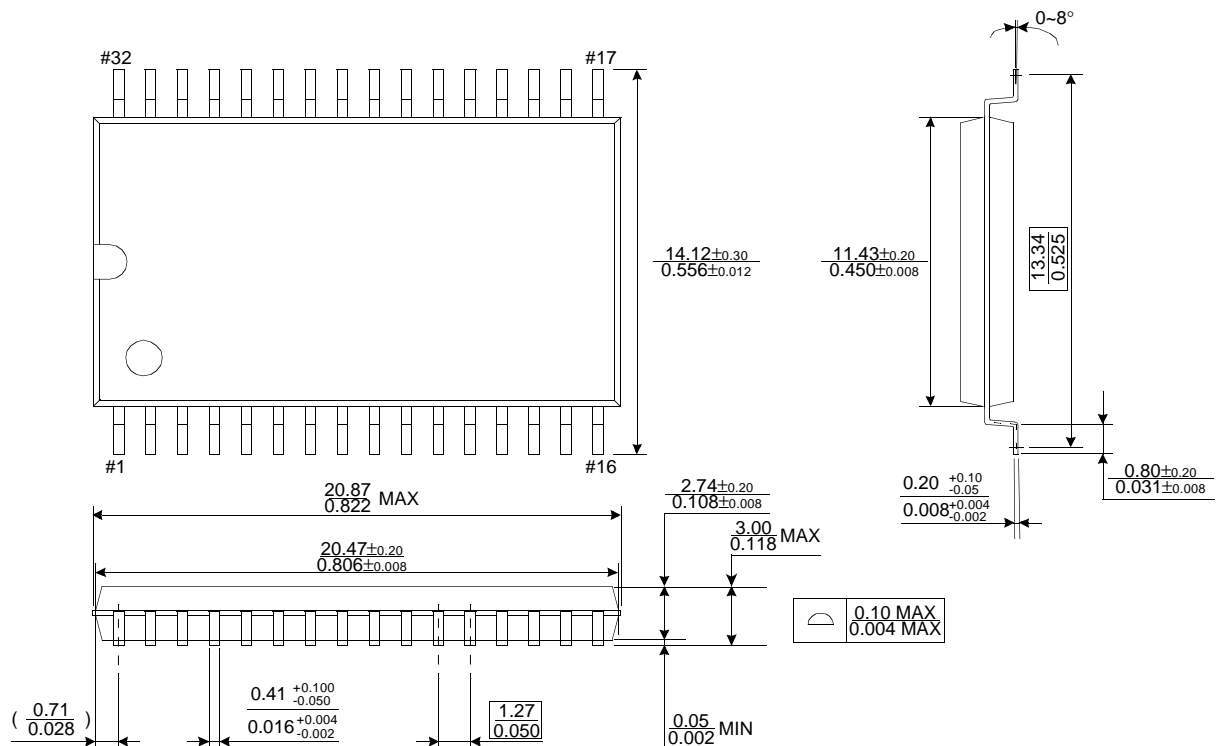
## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 32 DUAL INLINE PACKAGE (600mil)



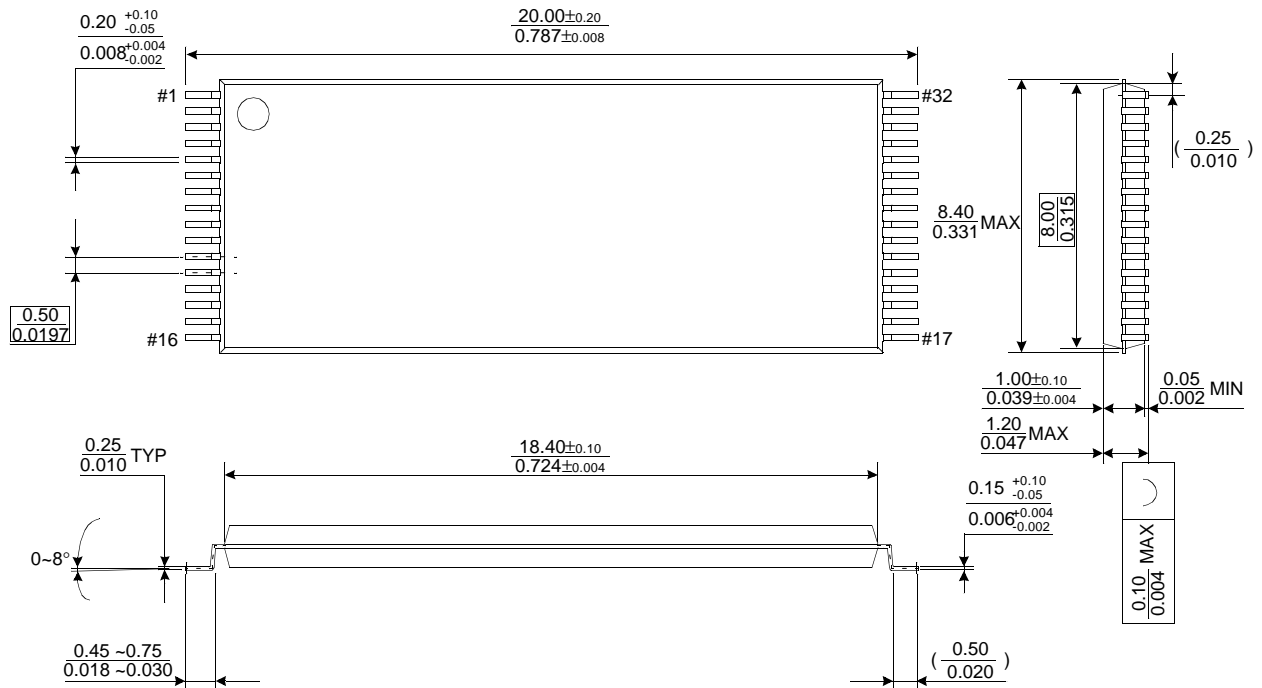
### 32 PLASTIC SMALL OUTLINE PACKAGE (525mil)



## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 32 THIN SMALL OUTLINE PACKAGE TYPE1 (0820F)



### 32 THIN SMALL OUTLINE PACKAGE TYPE1 (0820R)

