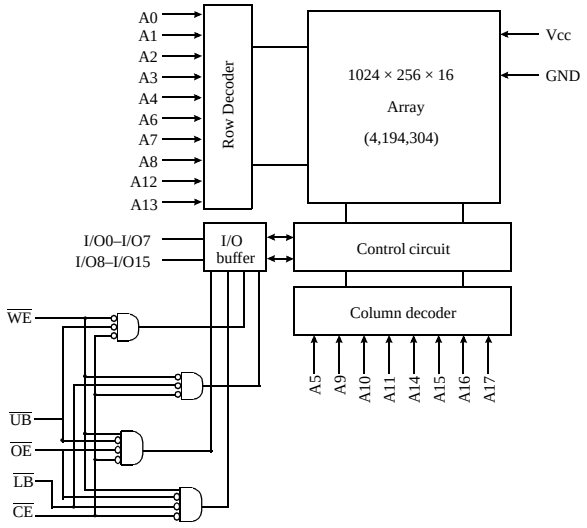
5V/3.3V 256K×16 CMOS SRAM

Features

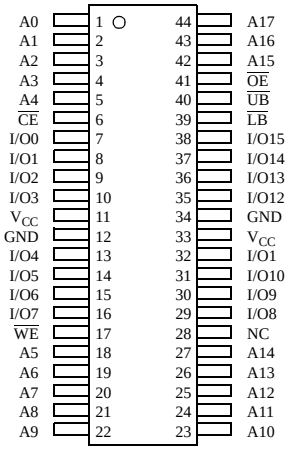
- Organization: 262,144 words × 16 bits
- Available in 3.3V (AS7C34098) and 5V (AS7C34098) versions
- High speed
  - 10/12/15/20/25 ns address access time
  - 4/4/5/5/6/7 ns output enable access time
- Low power consumption
  - Active: 990 mW max (20 ns cycle, 5V)
  - Standby:55 mW max, CMOS inputs
  - Very low DC component in active power
- Equal access and cycle times
- Individual byte read/write controls
- 2.0V data retention
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL- and CMOS-compatible, three-state I/
- 44-pin JEDEC standard packages
  - 400 mil SOJ
  - 400 mil TSOP II
- Center power and ground pins for low noise
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- Industrial temperature range available (-40 to +85 °C)
- Downward pin-compatible
  - 32K×16 (AS7C3513)
  - 64K×16 (AS7C31026)
  - 128K×16 (AS7C3128K16)

Logic block diagram



Pin arrangement

SOJ, TSOP II



Selection guide

	7C34098-10	7C4098-12 7C34098-12	7C4098-15 7C34098-15	7C4098-20 7C34098-20	7C4098-25 7C34098-25	Unit
Maximum address access time	10	12	15	20	25	ns
Maximum output enable access time	4	5	5	6	7	ns
Maximum operating current	AS7C4098	–	220	180	170	mA
	AS7C34098	200	170	120	110	mA
Maximum CMOS standby current		10	10	10	10	mA

Shaded areas indicate preliminary information.

Functional description

The AS7C4098 and AS7C34098 are high performance CMOS 4,194,304-bit Static Random Access Memories (SRAM) organized as 262,144 words × 16 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20/25 ns with output enable access times (t_{OE}) of 4/5/5/6/7 ns are ideal for high performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is High the device enters standby mode. The standard AS7C4098 is guaranteed not to exceed 55 mW power consumption in CMOS standby mode. Both devices offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0-I/O15 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) High. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

These devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0–I/O7, and $\overline{UB}$ controls the higher bits, I/O8–I/O15.

All chip inputs and outputs are TTL- and CMOS-compatible, and operation is from either a single 5V (AS7C4098) or 3.3V (AS7C34098) supply. Both devices are available in the JEDEC standard 400-mil, 44-pin SOJ and TSOP II packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any input pin relative to GND (7C4098)	V_t	–0.5	+7.0	V
Voltage on any input pin relative to GND (7C34098)	V_t	–0.5	+5.5	V
Voltage on any I/O pin	V_t	–0.5	V_{CC} + 0.5	V
Power dissipation	P_D	–	1.5	W
Storage temperature	T_{stg}	–55	+150	°C
DC output current	I_{out}	–	+/–20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specificati on is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Supply current	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	I_{SB}, I_{SB1}	High Z	High Z	Standby
L	H	H	X	X	I_{CC}	High Z	High Z	Output disable
L	X	X	H	H				
L	H	L	L	H	I_{CC}	D_{OUT}	High Z	Read
			H	L		High Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	I_{CC}	D_{IN}	High Z	Write
			H	L		High Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

Key: X = don't care, L = Low, H = High

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage	AS7C4098	V_{CC}	4.5	5.0	5.5	V
	AS7C34098	V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
Input voltage	AS7C4098	V_{IH}	2.2	–	V_{CC} + 0.5	V
	AS7C34098	V_{IH}	2.0	–	V_{CC} + 0.5	V
		V_{IL}	–0.5†	–	0.8	V
Ambient operating temperature	Commercial	T_A	0	–	70	°C
	Industrial	T_A	-40	–	85	°C

† V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics

				-10		-12		-15		-20		-25		
Parameter	Symbol	Test conditions		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = GND to V_{CC}		–	1	–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}		–		–	5	–	5	–	5	–	5	µA
Operating power supply current	I_{CC}	Min cycle, 100% duty $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA	–	AS7C4098		–	200	–	180	–	150	–	125	mA
			–	AS7C34098		–	110	–	90	–	80	–	70	mA
Standby power supply current	I_{SB}	$\overline{CE}$ = $V_{IH, f=MAX}$				–	60	–	60	–	60	–	60	mA
	I_{SB1}	$\overline{CE}$ ≥ V_{CC}–0.2V V_{IN} ≥ V_{CC}–0.2V or V_{IN} ≤ 0.2V, f=0				–	10	–	10	–	10	–	10	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min				–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min				2.4	–	2.4	–	2.4	–	2.4	–	V

Shaded areas indicate preliminary information.

Capacitance

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$	V_{IN} = 0V	6	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	8	pF

Key to switching waveforms

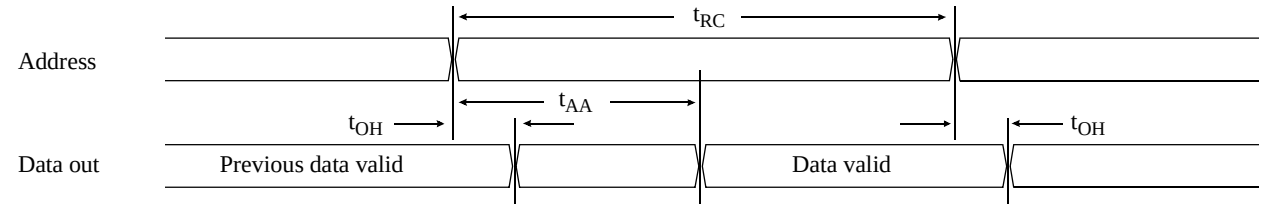
Rising input Falling input Undefined output/don't care

Read cycle [3,9]

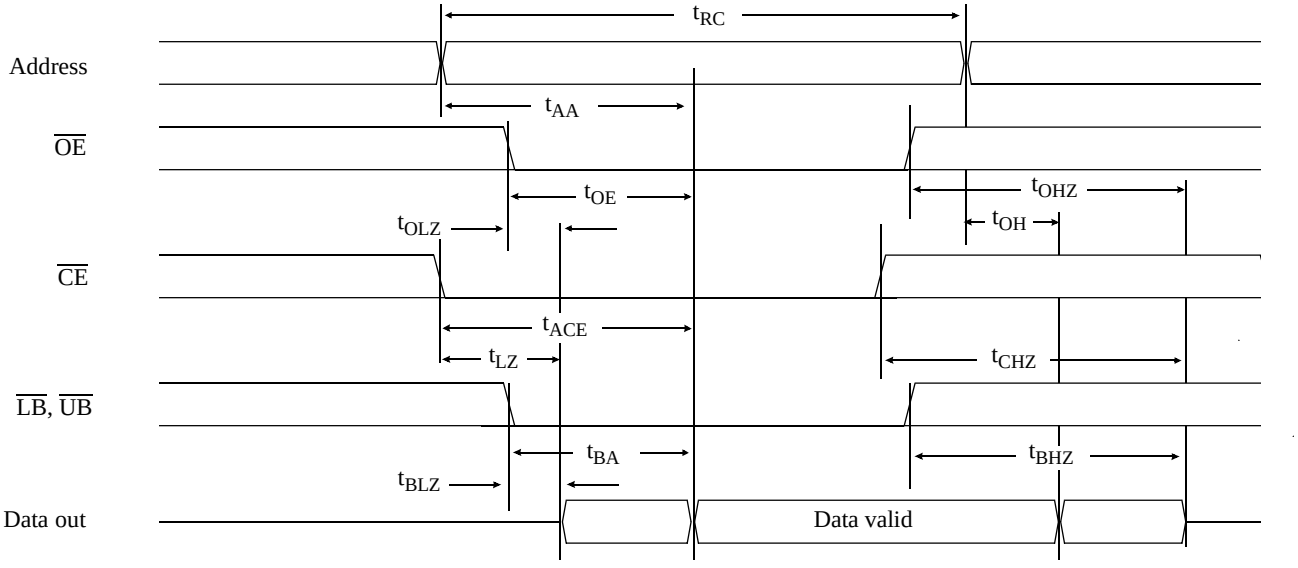
		-10		-12		-15		-20		-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	25	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	–	25	ns	
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	–	20	–	25	ns	
Output enable ($\overline{OE}$) access time	t_{OE}	–	4	–	5	–	5	–	6	–	7	ns	
Output hold from address change	t_{OH}	3	–	4	–	4	–	4	–	5	–	ns	5
$\overline{CE}$ Low to output in Low Z	t_{CLZ}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{CE}$ High to output in High Z	t_{CHZ}	–	4	–	5	–	6	–	7	–	8	ns	4, 5
$\overline{OE}$ Low to output in Low Z	t_{OLZ}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ High to output in High Z	t_{OHZ}	–	4	–	5	–	6	–	7	–	8	ns	4, 5
$\overline{LB}$, $\overline{UB}$ access time	t_{BA}	–	4	-	5	-	6	-	7	-	8	ns	
$\overline{LB}$, $\overline{UB}$ Low to output in Low Z	t_{BLZ}	0	–	0	-	0	-	0	-	0	-	ns	
$\overline{LB}$, $\overline{UB}$ High to output in High Z	t_{BHZ}	–	4	-	5	-	6	-	7	-	8	ns	
Power up time	t_{PU}	0	–	0	–	0	–	0	–	0	–	ns	5
Power down time	t_{PD}	–	10	–	12	–	15	–	20	–	25	ns	5

Shaded areas indicate preliminary information.

Read waveform 1 [6,7,9]



Read waveform 2 [6,8,9]

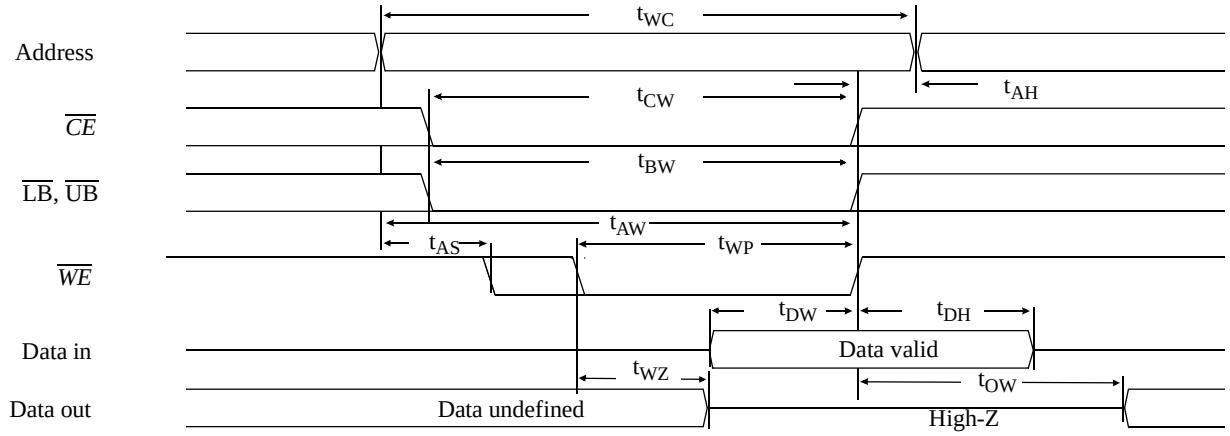


Write cycle [11]

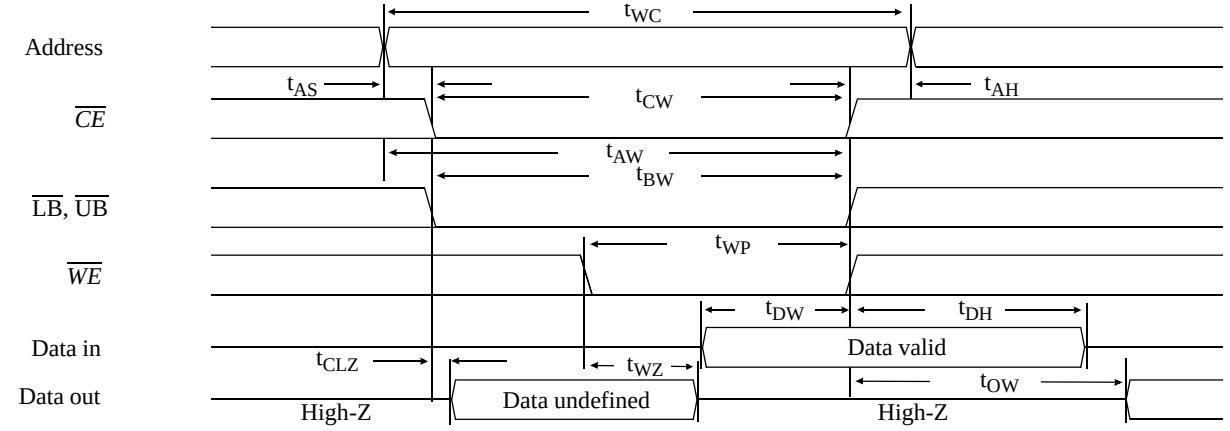
		-10		-12		-15		-20		-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	25	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	7	–	8	–	10	–	15	–	17	–	ns	
Address setup to write end	t_{AW}	7	–	8	–	10	–	15	–	17	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	7	–	8	–	10	–	15	–	17	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	7	–	10	–	12	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High-Z	t_{WZ}	–	4	–	5	–	6	–	8	–	8	ns	4, 5
Output active from write end	t_{OW}	1	–	1	–	1	–	1	–	2	–	ns	4, 5
Byte enable Low to write end	t_{BW}	7	–	8	–	12	–	15	–	17	–	ns	4, 5

Shaded areas indicate preliminary information.

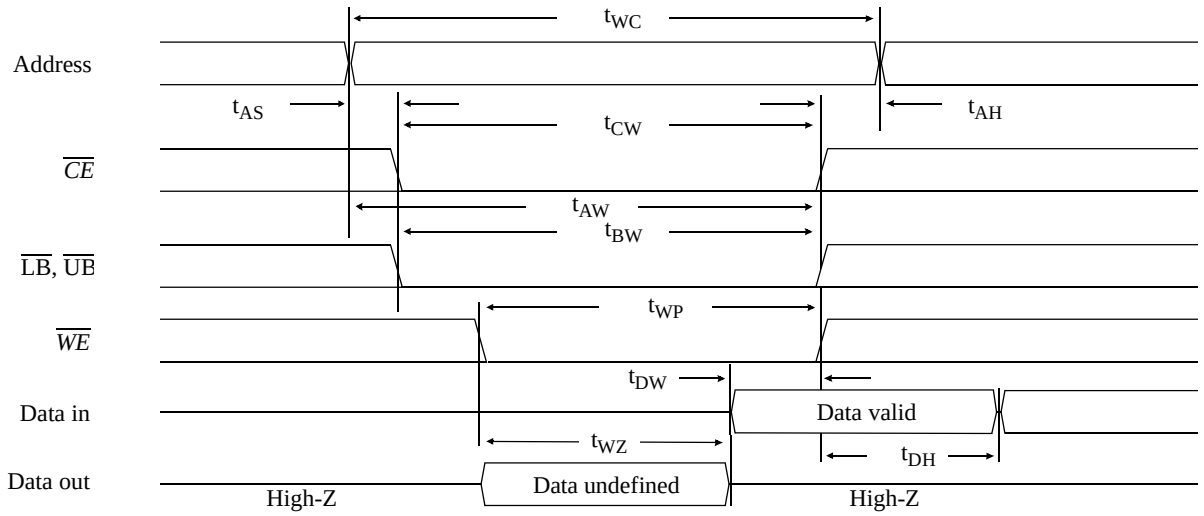
Write waveform 1 [10,11]



Write waveform 2 [10,11]



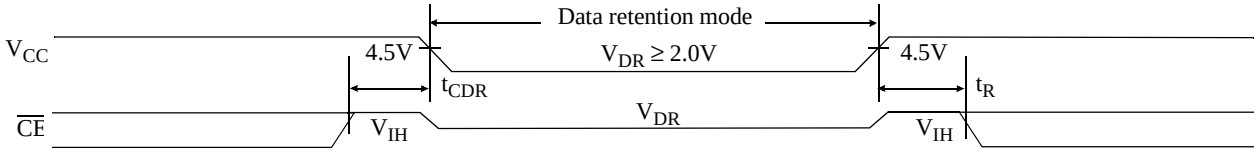
Write waveform 3 [10,11]



Data retention characteristics [13]

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V $\overline{CE} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ *or* $V_{in} \leq 0.2V$	2.0	–	V
Data retention current	I_{CCDR}		–	500	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B, except as noted.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 3 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

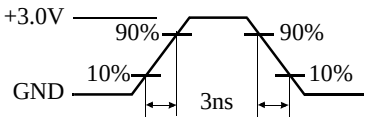


Figure A: Input pulse

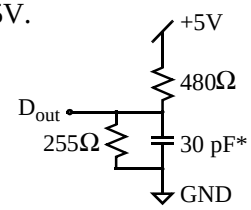


Figure B: Output load

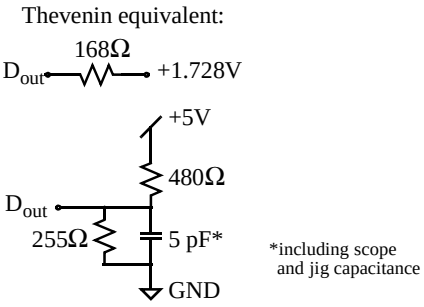


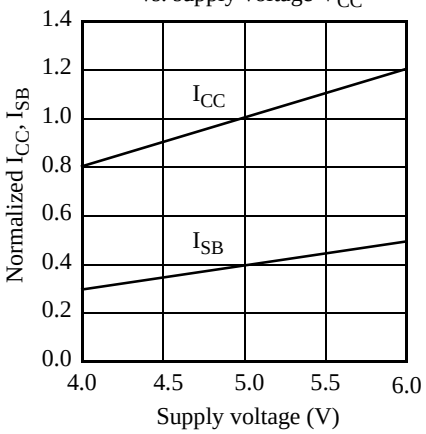
Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WZ}, t_{OW}

Notes

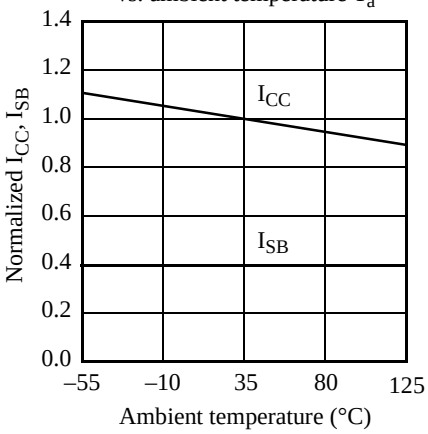
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be High during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 This data applies to the AS7C4098 only. The AS7C34098 functions similarly.
13 2V data retention applies to commercial temperature range operation only.

Typical DC and AC characteristics [12]

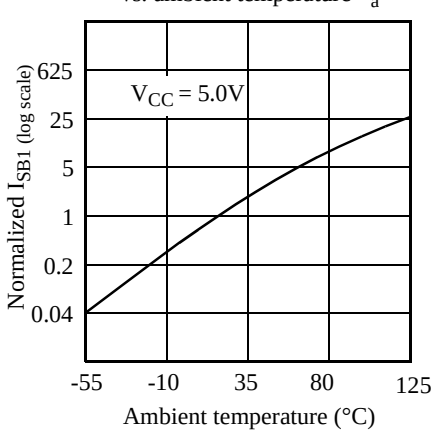
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



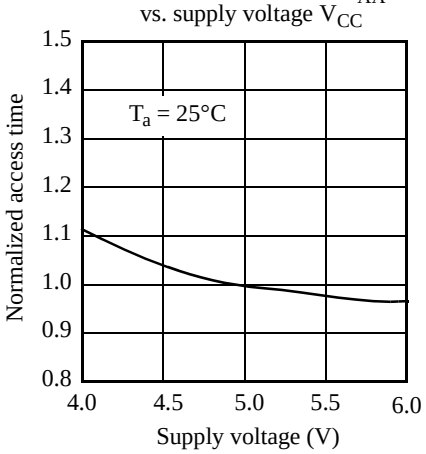
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



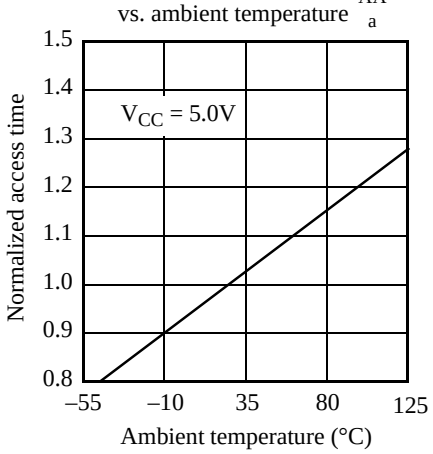
Normalized supply current I_{SB1} vs. ambient temperature $_a$



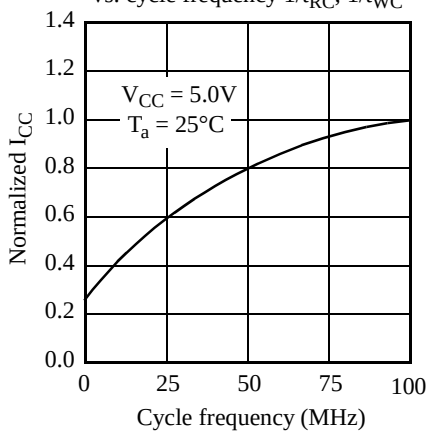
Normalized access time t_{AA} vs. supply voltage V_{CC}



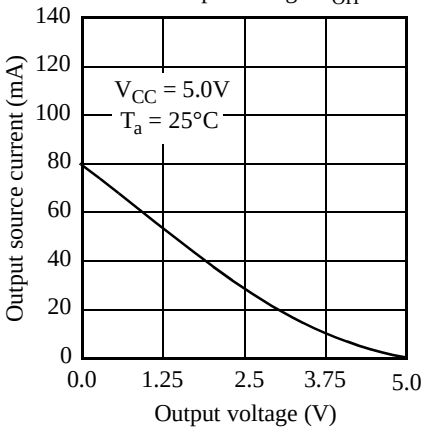
Normalized access time t_{AA} vs. ambient temperature $_a$



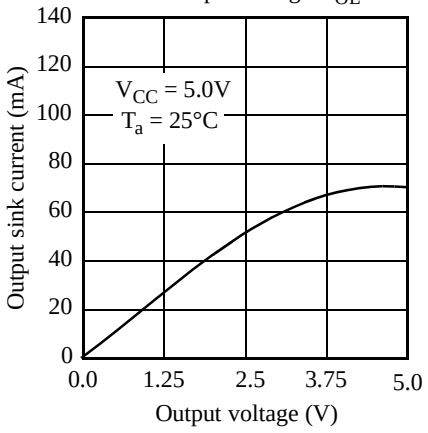
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



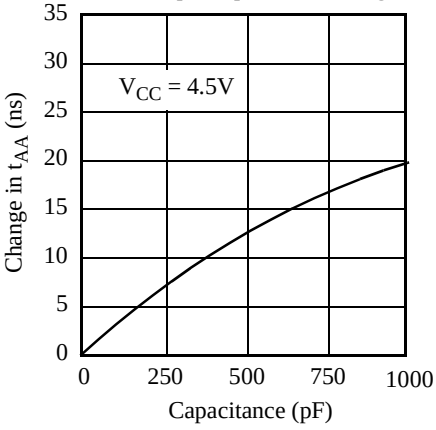
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}



Typical access time change Δt_{AA} vs. output capacitive loading



AS7C4098 ordering codes

Package	Version		10 ns	12 ns	15 ns	20 ns	25 ns
SOJ	Commercial temperature	5V		AS7C4098-12JC	AS7C4098-15JC	AS7C4098-20JC	AS7C4098-25JC
		3.3V		AS7C34098-12JC	AS7C34098-15JC	AS7C34098-20JC	AS7C34098-25JC
	Industrial temperature	5V		AS7C4098-12JI	AS7C4098-15JI	AS7C4098-20JI	AS7C4098-25JI
		3.3V		AS7C34098-12JI	AS7C34098-15JI	AS7C34098-20JI	AS7C34098-25JI
TSOP II	Commercial temperature	5V		AS7C4098-12TC	AS7C4098-15TC	AS7C4098-20TC	AS7C4098-25TC
		3.3V		AS7C34098-12TC	AS7C34098-15TC	AS7C34098-20TC	AS7C34098-25TC
	Industrial temperature	5V		AS7C4098-12TI	AS7C4098-15TI	AS7C4098-20TI	AS7C4098-25TI
		3.3V		AS7C34098-12TI	AS7C34098-15TI	AS7C34098-20TI	AS7C34098-25TI

Shaded areas indicate preliminary information.

AS7C4098 part numbering system

AS7C	X	4098	–XX	X	X
SRAM prefix	Blank = 5V CMOS 3 = 3.3V CMOS	Device number	Access time	Package:J = SOJ 400 mil T = TSOP II 400 mil	Temperature range, C = Commercial:0°C to 70°C I = Industrial: -40°C to 85°C