

Distributed by:

JAMECO[®]
ELECTRONICS

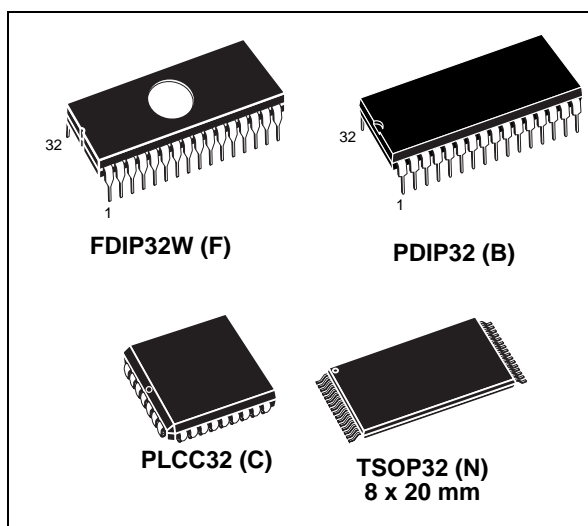
www.Jameco.com ♦ 1-800-831-4242

The content and copyrights of the attached
material are the property of its owner.

Jameco Part Number 697961

1 Mbit (128 Kbit x 8) UV EPROM and OTP EPROM**Features**

- $5\text{v} \pm 10\%$ Supply Voltage in Read Operation
- Access Time: 35ns
- Low Power Consumption:
 - Active Current: 30 mA at 5 MHz
 - Standby Current: 100 μA
- Programming Voltage: $12.75\text{V} \pm 0.25\text{V}$
- Programming Time: 100 μs /word
- Electronic Signature
 - Manufacturer Code: 20h
 - Device Code: 05h
- ECOPACK® packages available



Contents

- 1 Summary description 5**
- 2 Device description 8**
 - 2.1 Read mode 8
 - 2.2 Standby mode 8
 - 2.3 Two-line output control 8
 - 2.4 System considerations 9
 - 2.5 Programming 9
 - 2.6 Presto II programming algorithm 9
 - 2.7 Program Inhibit 10
 - 2.8 Program Verify 10
 - 2.9 Electronic Signature 10
 - 2.10 Erasure operation (applies to UV EPROM) 11
- 3 Maximum ratings 12**
- 4 DC and AC characteristics 13**
- 5 Package mechanical data 18**
 - 5.1 32-pin Ceramic Frit-seal DIP, with round window (FDIP32WA) 18
 - 5.2 32-pin Plastic DIP, 600 mils width (PDIP32) 19
 - 5.3 32-lead Rectangular Plastic Leaded Chip Carrier (PLCC32) 20
 - 5.4 32-lead Plastic Thin Small Outline, 8x20 mm (TSOP32) 21
- 6 Part numbering 22**
- 7 Revision history 23**

List of tables

| | | |
|-----------|---|----|
| Table 1. | Signal Descriptions | 6 |
| Table 2. | Operating Modes | 8 |
| Table 3. | Electronic Signature | 11 |
| Table 4. | Absolute Maximum Ratings | 12 |
| Table 5. | Read Mode DC Characteristics | 13 |
| Table 6. | Programming Mode DC Characteristics | 13 |
| Table 7. | Capacitance | 14 |
| Table 8. | AC Measurement Conditions | 14 |
| Table 9. | Read Mode AC Characteristics | 15 |
| Table 10. | Read Mode AC Characteristics | 16 |
| Table 11. | Programming Mode AC Characteristics | 17 |
| Table 12. | FDIP32WA package mechanical data | 18 |
| Table 13. | PDIP32 package mechanical data | 19 |
| Table 14. | PLCC32 package mechanical data | 20 |
| Table 15. | TSOP32 package mechanical data | 21 |
| Table 16. | Ordering information scheme | 22 |
| Table 17. | Document revision history | 23 |

List of figures

| | | |
|------------|---|----|
| Figure 1. | Logic Diagram | 5 |
| Figure 2. | DIP Connections | 6 |
| Figure 3. | LCC Connections | 7 |
| Figure 4. | TSOP Connections | 7 |
| Figure 5. | Programming Flowchart | 10 |
| Figure 6. | AC Testing Input Output Waveform | 14 |
| Figure 7. | AC Testing Load Circuit | 14 |
| Figure 8. | Read Mode AC Waveforms | 16 |
| Figure 9. | Programming and Verify Modes AC Waveforms | 17 |
| Figure 10. | FDIP32WA package outline | 18 |
| Figure 11. | PDIP32 package outline | 19 |
| Figure 12. | PLCC32 package outline | 20 |
| Figure 13. | TSOP32 package outline | 21 |

1 Summary description

The M27C1001 is a 1 Mbit EPROM offered in the two ranges: UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large programs and is organized as 131,072 words of 8 bits.

The FDIP32W (window ceramic frit-seal package) has a transparent lid that enables the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C1001 is offered in PDIP32, PLCC32 and TSOP32 (8 x 20 mm) packages.

In order to meet environmental requirements, ST offers the M27C1001 in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at: www.st.com.

See [Figure 1: Logic Diagram](#) and [Table 1: Signal Descriptions](#) for a brief overview of the signals connected to this device.

Figure 1. Logic Diagram

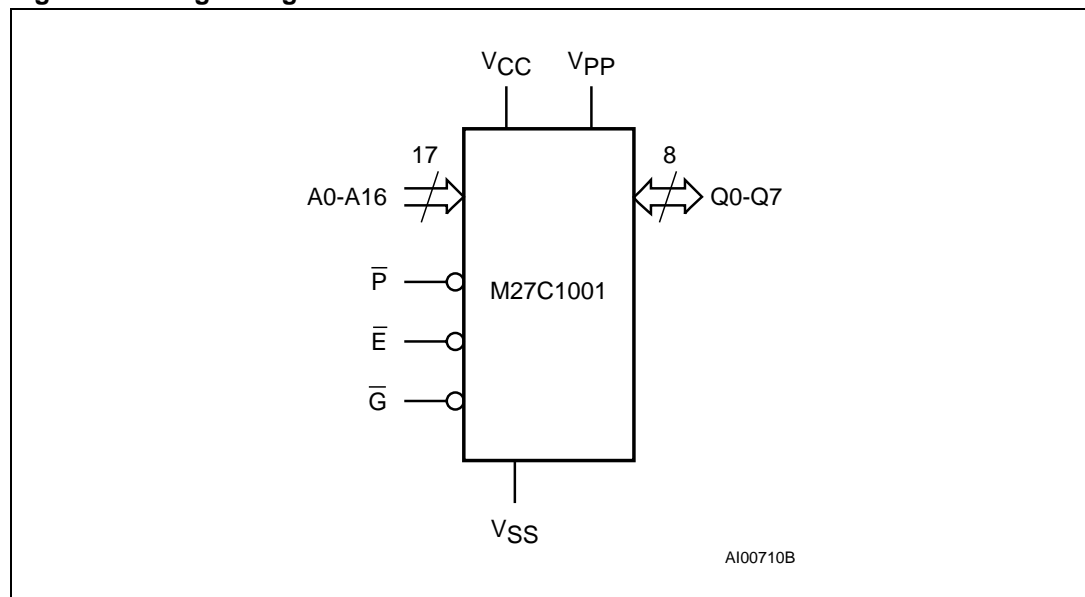


Table 1. Signal Descriptions

| Signal | Description |
|-----------------|--------------------------|
| A0-A16 | Address Inputs |
| Q0-Q7 | Data Outputs |
| \bar{E} | Chip Enable |
| \bar{G} | Output Enable |
| \bar{P} | Program |
| V _{PP} | Program Supply |
| V _{CC} | Supply Voltage |
| V _{SS} | Ground |
| NC | Not Connected Internally |

Figure 2. DIP Connections

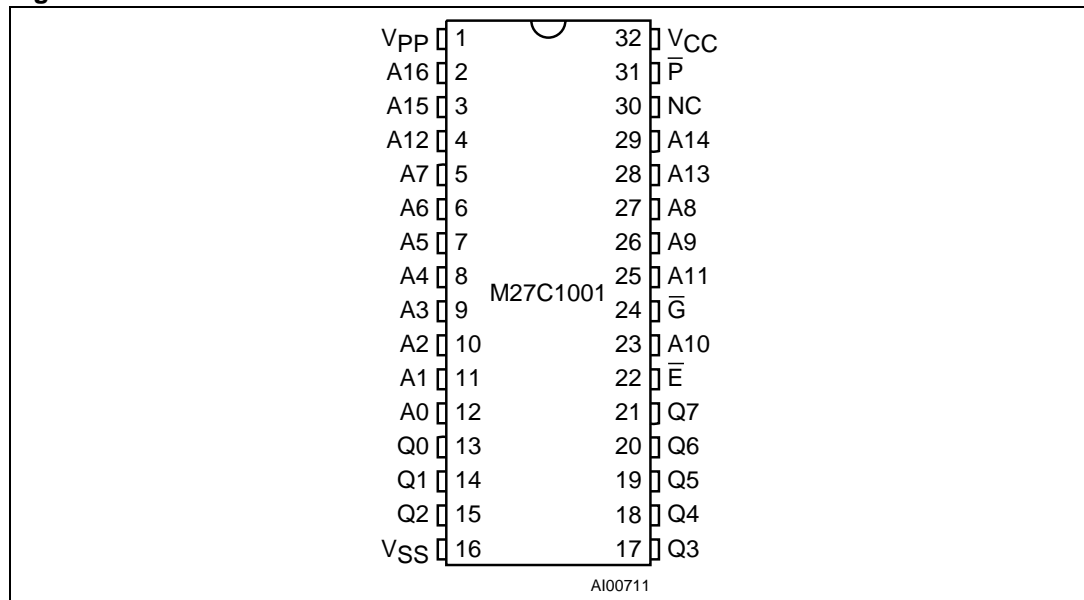


Figure 3. LCC Connections

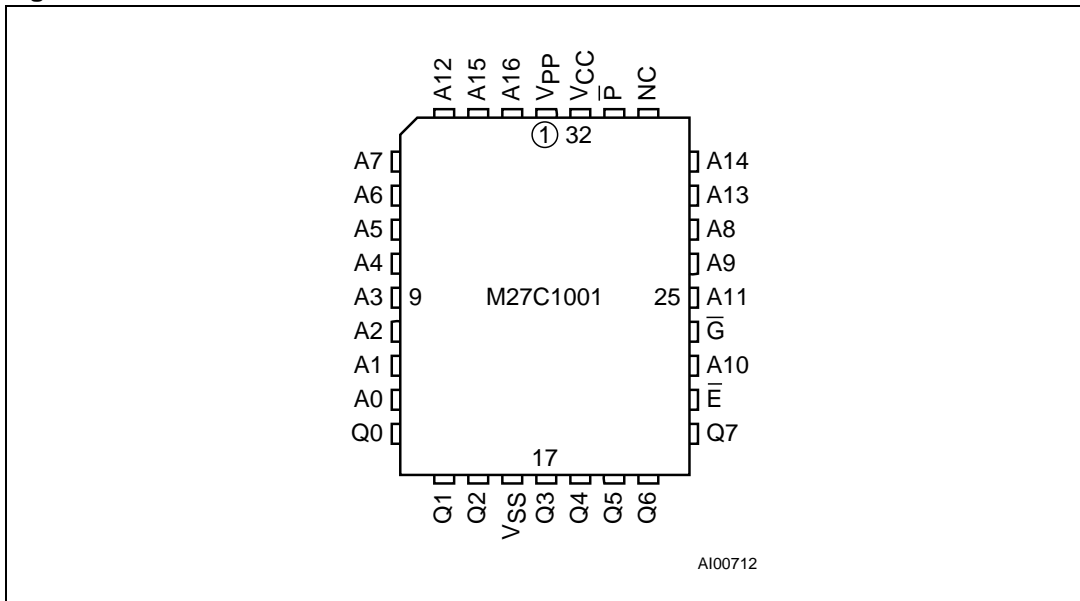
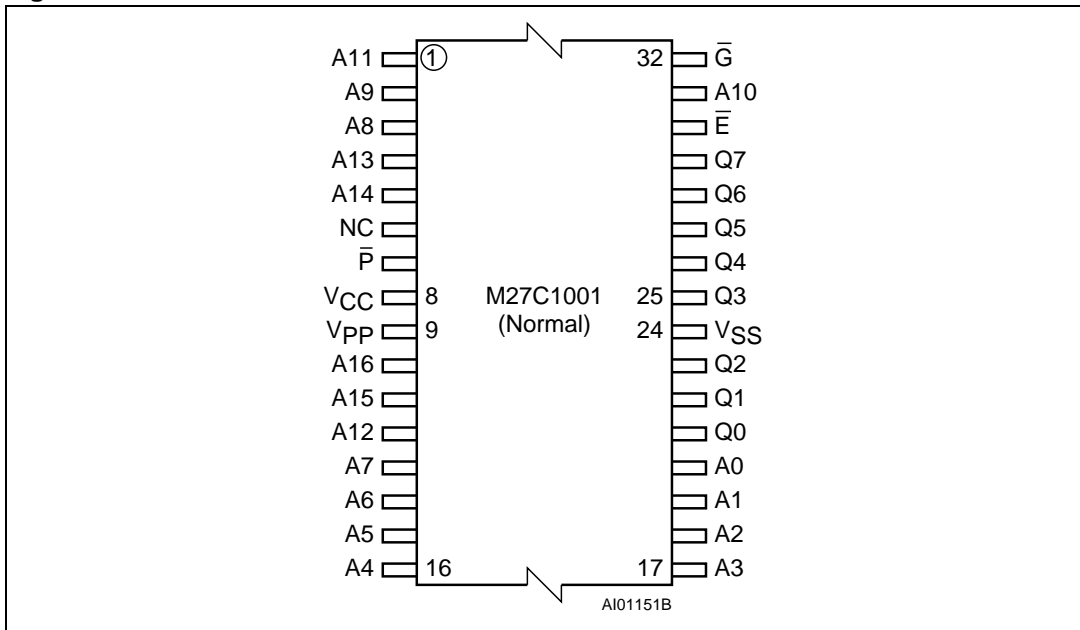


Figure 4. TSOP Connections



2 Device description

[Table 2](#) lists the operating modes of the M27C1001. A single power supply is required in Read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Table 2. Operating Modes

| Mode | \bar{E} | \bar{G} | \bar{P} | A9 | V_{PP} | Q7-Q0 |
|----------------------|-----------|-----------|----------------|----------|----------------------|----------|
| Read | V_{IL} | V_{IL} | X | X | V_{CC} or V_{SS} | Data Out |
| Output Disable | V_{IL} | V_{IH} | X | X | V_{CC} or V_{SS} | Hi-Z |
| Program | V_{IL} | V_{IH} | V_{IL} Pulse | X | V_{PP} | Data In |
| Verify | V_{IL} | V_{IL} | V_{IH} | X | V_{PP} | Data Out |
| Program Inhibit | V_{IH} | X | X | X | V_{PP} | Hi-Z |
| Standby | V_{IH} | X | X | X | V_{CC} or V_{SS} | Hi-Z |
| Electronic Signature | V_{IL} | V_{IL} | V_{IH} | V_{ID} | V_{CC} | Codes |

Note: $X = V_{IH}$ or V_{IL} , $V_{ID} = 12V \pm 0.5V$.

2.1 Read mode

The M27C1001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\bar{E}) is the power control and should be used for device selection. Output Enable (\bar{G}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from \bar{E} to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of \bar{G} , assuming that \bar{E} has been low and the addresses have been stable for at least $t_{AVQV} - t_{GLQV}$.

2.2 Standby mode

The M27C1001 has a standby mode which reduces the supply current from 30mA to 100 μ A. The M27C1001 is placed in the standby mode by applying a CMOS high signal to the \bar{E} input. When in the standby mode, the outputs are in a high impedance state, independent of the \bar{G} input.

2.3 Two-line output control

Because EPROMs are usually used in larger memory arrays, this product features a 2-line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, \bar{E} should be decoded and used as the primary device selecting function, while \bar{G} should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This

ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

2.4 System considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC} , has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of \bar{E} . The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and V_{SS} . This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

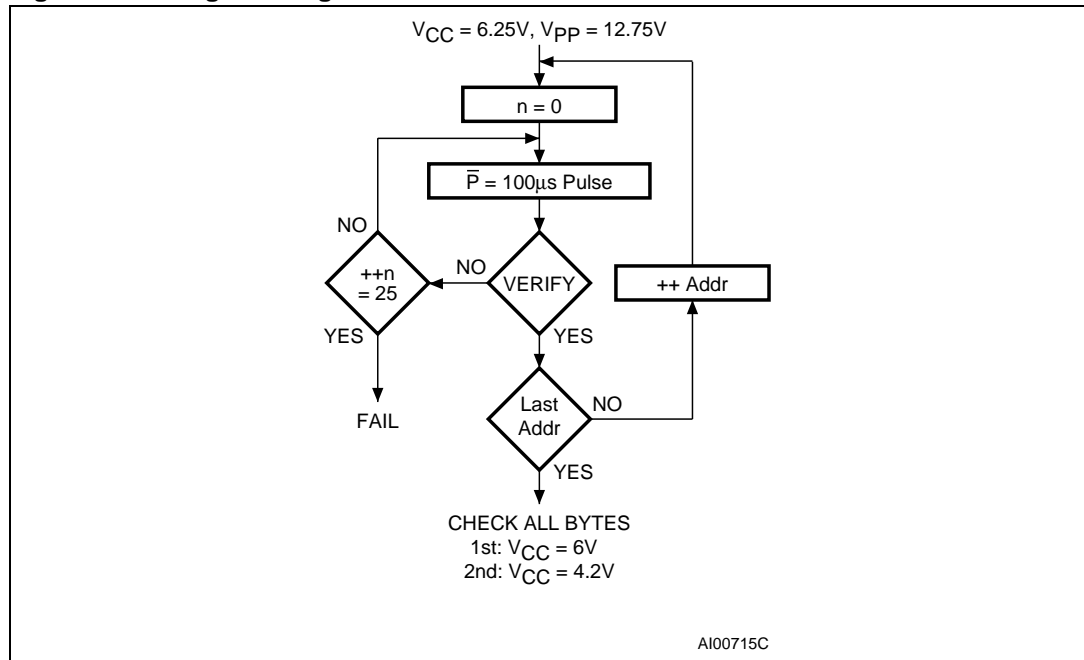
2.5 Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C1001 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0's will be programmed, both '1's and '0's can be present in the data word. The only way to change a '0' to a '1' is by die exposition to ultraviolet light (UV EPROM). The M27C1001 is in the programming mode when V_{PP} input is at 12.75V, \bar{E} is at V_{IL} and \bar{P} is pulsed to V_{IL} . The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be $6.25\text{V} \pm 0.25\text{V}$.

2.6 Presto II programming algorithm

Presto II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in a typical time of 13 seconds. Programming with Presto II involves in applying a sequence of 100 μs program pulses to each byte until a correct verify occurs (see [Figure 5](#)). During programming and verify operation, a Margin mode circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in Margin mode provides necessary margin to each programmed cell.

Figure 5. Programming Flowchart



2.7 Program Inhibit

Programming of multiple M27C1001s in parallel with different data is also easily accomplished. Except for \bar{E} , all like inputs including \bar{G} of the parallel M27C1001 may be common. A TTL low level pulse applied to a M27C1001's \bar{P} input, with \bar{E} low and V_{PP} at 12.75V, will program that M27C1001. A high level \bar{E} input inhibits the other M27C1001s from being programmed.

2.8 Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with \bar{E} and \bar{G} at V_{IL} , \bar{P} at V_{IH} , V_{PP} at 12.75V and V_{CC} at 6.25V.

2.9 Electronic Signature

The Electronic Signature (ES) mode enables the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the M27C1001. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1001, with $V_{PP} = V_{CC} = 5\text{V}$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the STMicroelectronics M27C1001, these two identifier bytes are given in [Table 3](#) and can be read-out on outputs Q7 to Q0.

Table 3. Electronic Signature

| Identifier | A0 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Hex Data |
|---------------------|----------|----|----|----|----|----|----|----|----|----------|
| Manufacturer's Code | V_{IL} | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Device Code | V_{IH} | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05h |

2.10 Erasure operation (applies to UV EPROM)

The erasure characteristics of the M27C1001 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1001 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm² power rating. The M27C1001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

3 Maximum ratings

Table 4. Absolute Maximum Ratings⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------------|--|------------|------|
| T_A | Ambient Operating Temperature ⁽²⁾ | –40 to 125 | °C |
| T_{BIAS} | Temperature Under Bias | –50 to 125 | °C |
| T_{STG} | Storage Temperature | –65 to 150 | °C |
| V_{IO} ⁽³⁾ | Input or Output Voltage (except A9) | –2 to 7 | V |
| V_{CC} | Supply Voltage | –2 to 7 | V |
| V_{A9} ⁽³⁾ | A9 Voltage | –2 to 13.5 | V |
| V_{PP} | Program Supply Voltage | –2 to 14 | V |

1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.
3. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns.
Maximum DC voltage on Output is VCC +0.5V with possible overshoot to VCC +2V for a period less than 20ns.

4 DC and AC characteristics

$T_A = 0$ to 70°C , -40 to 85°C or -40 to 125°C ; $V_{CC} = 5\text{V} \pm 5\%$ or $5\text{V} \pm 10\%$; $V_{PP} = V_{CC}$

Table 5. Read Mode DC Characteristics (1)

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|----------------|-------------------------------|---|------------------------|--------------|---------------|
| I_{LI} | Input Leakage Current | $0\text{V} \leq V_{IN} \leq V_{CC}$ | | ± 10 | μA |
| I_{LO} | Output Leakage Current | $0\text{V} \leq V_{OUT} \leq V_{CC}$ | | ± 10 | μA |
| I_{CC} | Supply Current | $\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$, $I_{OUT} = 0\text{mA}$, $f = 5\text{MHz}$ | | 30 | mA |
| I_{CC1} | Supply Current (Standby) TTL | $\bar{E} = V_{IH}$ | | 1 | mA |
| I_{CC2} | Supply Current (Standby) CMOS | $\bar{E} > V_{CC} - 0.2\text{V}$ | | 100 | μA |
| I_{PP} | Program Current | $V_{PP} = V_{CC}$ | | 10 | μA |
| V_{IL} | Input Low Voltage | | -0.3 | 0.8 | V |
| $V_{IH}^{(2)}$ | Input High Voltage | | 2 | $V_{CC} + 1$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1\text{mA}$ | | 0.4 | V |
| V_{OH} | Output High Voltage TTL | $I_{OH} = -400\mu\text{A}$ | 2.4 | | V |
| | Output High Voltage CMOS | $I_{OH} = -100\mu\text{A}$ | $V_{CC} - 0.7\text{V}$ | | V |

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

2. Maximum DC voltage on Output is $V_{CC} + 0.5\text{V}$.

$T_A = 25^\circ\text{C}$; $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$; $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$

Table 6. Programming Mode DC Characteristics (1)

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|----------|-------------------------|----------------------------------|------|----------------|---------------|
| I_{LI} | Input Leakage Current | $V_{IL} \leq V_{IN} \leq V_{IH}$ | | ± 10 | μA |
| I_{CC} | Supply Current | | | 50 | mA |
| I_{PP} | Program Current | $\bar{E} = V_{IL}$ | | 50 | mA |
| V_{IL} | Input Low Voltage | | -0.3 | 0.8 | V |
| V_{IH} | Input High Voltage | | 2 | $V_{CC} + 0.5$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1\text{mA}$ | | 0.4 | V |
| V_{OH} | Output High Voltage TTL | $I_{OH} = -400\mu\text{A}$ | 2.4 | | V |
| V_{ID} | A9 Voltage | | 11.5 | 12.5 | V |

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$

Table 7. Capacitance (1)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|-----------|--------------------|----------------|-----|-----|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | | 6 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | | 12 | pF |

1. Sampled only, not 100% tested.

Table 8. AC Measurement Conditions

| Parameter | High Speed | Standard |
|---------------------------------------|--------------------|--------------------|
| Input Rise and Fall Times | $\leq 10\text{ns}$ | $\leq 20\text{ns}$ |
| Input Pulse Voltages | 0 to 3V | 0.4V to 2.4V |
| Input and Output Timing Ref. Voltages | 1.5V | 0.8V and 2V |

Figure 6. AC Testing Input Output Waveform

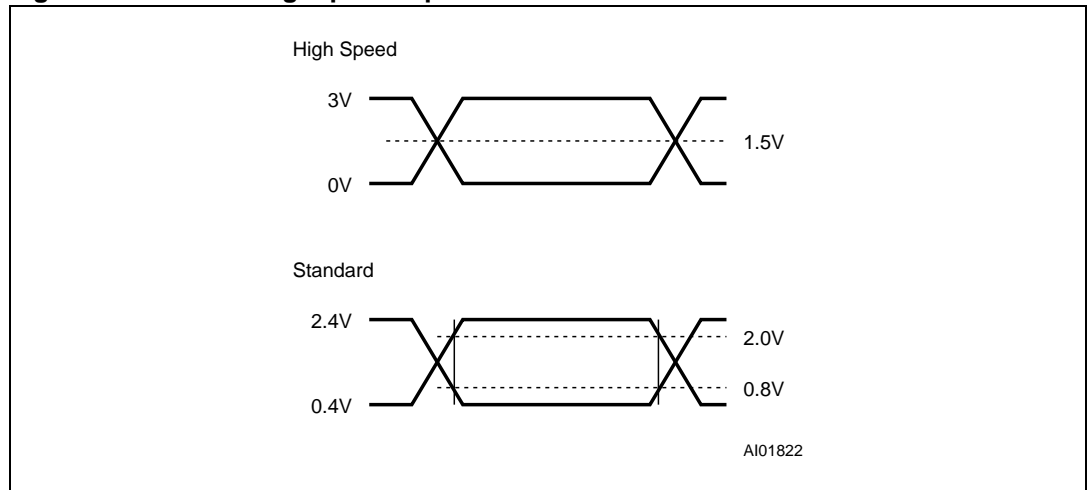
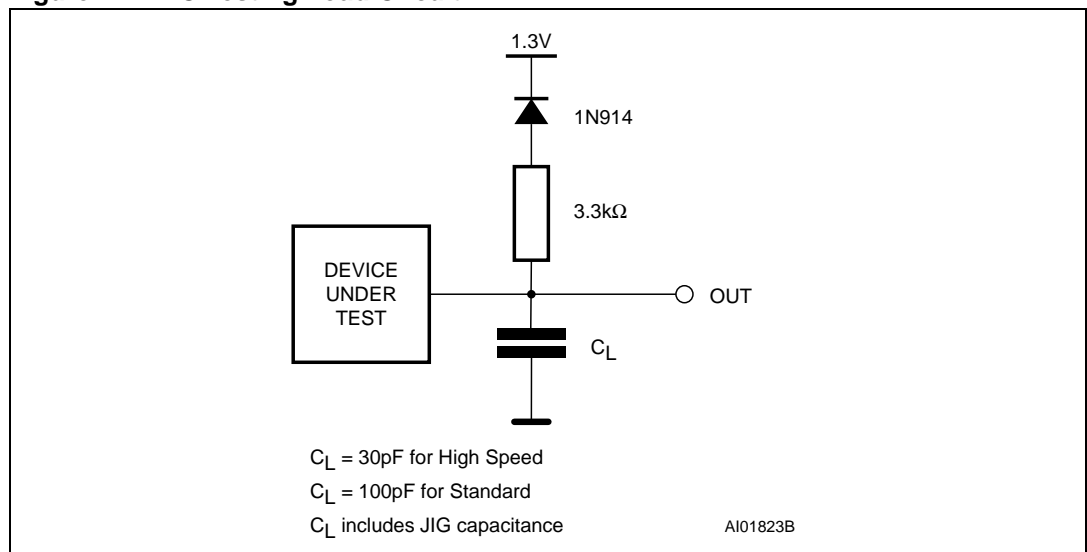


Figure 7. AC Testing Load Circuit



$T_A = 0$ to 70°C , -40 to 85°C or -40 to 125°C ; $V_{CC} = 5\text{V} \pm 5\%$ or $5\text{V} \pm 10\%$; $V_{PP} = V_{CC}$

Table 9. Read Mode AC Characteristics (1)

| Symbol | Alt | Parameter | Test Condition | M27C1001 | | | | | | | | Unit |
|------------------|-----------|---|--|----------|------|------|------|------|------|------|------|------|
| | | | | -35 (2) | | -45 | | -60 | | -70 | | |
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{AVQV} | t_{ACC} | Address Valid to Output Valid | $\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$ | | 35 | | 45 | | 60 | | 70 | ns |
| t_{ELQV} | t_{CE} | Chip Enable Low to Output Valid | $\bar{G} = V_{IL}$ | | 35 | | 45 | | 60 | | 70 | ns |
| t_{GLQV} | t_{OE} | Output Enable Low to Output Valid | $\bar{E} = V_{IL}$ | | 25 | | 25 | | 30 | | 35 | ns |
| $t_{EHQZ}^{(3)}$ | t_{DF} | Chip Enable High to Output Hi-Z | $\bar{G} = V_{IL}$ | 0 | 25 | 0 | 25 | 0 | 30 | 0 | 30 | ns |
| $t_{GHQZ}^{(3)}$ | t_{DF} | Output Enable High to Output Hi-Z | $\bar{E} = V_{IL}$ | 0 | 25 | 0 | 25 | 0 | 30 | 0 | 30 | ns |
| t_{AXQX} | t_{OH} | Address Transition to Output Transition | $\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$ | 0 | | 0 | | 0 | | 0 | | ns |

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .
2. Speed obtained with High Speed AC measurement conditions.
3. Sampled only, not 100% tested.

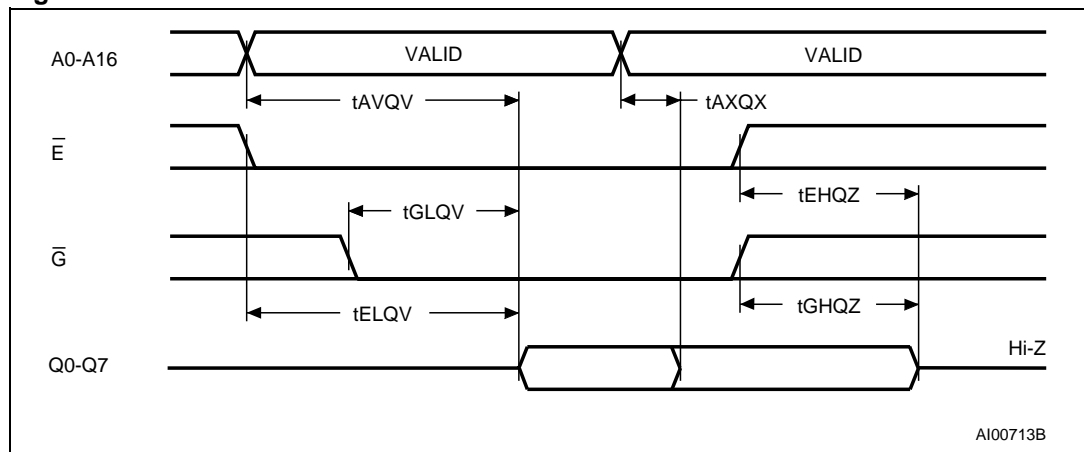
$T_A = 0$ to 70°C , -40 to 85°C or -40 to 125°C ; $V_{CC} = 5\text{V} \pm 5\%$ or $5\text{V} \pm 10\%$; $V_{PP} = V_{CC}$

Table 10. Read Mode AC Characteristics (1)

| Symbol | Alt | Parameter | Test Condition | M27C1001 | | | | | | | | Unit |
|------------------|-----------|---|--------------------------------------|----------|-----|-----|-----|-----|-----|---------------------|-----|------|
| | | | | -80 | | -90 | | -10 | | -12/-15/ -20/-25 | | |
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{AVQV} | t_{ACC} | Address Valid to Output Valid | $\bar{E} = V_{IL}, \bar{G} = V_{IL}$ | | 80 | | 90 | | 100 | | 120 | ns |
| t_{ELQV} | t_{CE} | Chip Enable Low to Output Valid | $\bar{G} = V_{IL}$ | | 80 | | 90 | | 100 | | 120 | ns |
| t_{GLQV} | t_{OE} | Output Enable Low to Output Valid | $\bar{E} = V_{IL}$ | | 40 | | 45 | | 50 | | 60 | ns |
| $t_{EHQZ}^{(2)}$ | t_{DF} | Chip Enable High to Output Hi-Z | $\bar{G} = V_{IL}$ | 0 | 30 | 0 | 30 | 0 | 30 | 0 | 40 | ns |
| $t_{GHQZ}^{(2)}$ | t_{DF} | Output Enable High to Output Hi-Z | $\bar{E} = V_{IL}$ | 0 | 30 | 0 | 30 | 0 | 30 | 0 | 40 | ns |
| t_{AXQX} | t_{OH} | Address Transition to Output Transition | $\bar{E} = V_{IL}, \bar{G} = V_{IL}$ | 0 | | 0 | | 0 | | 0 | | ns |

- V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .
- Sampled only, not 100% tested.

Figure 8. Read Mode AC Waveforms



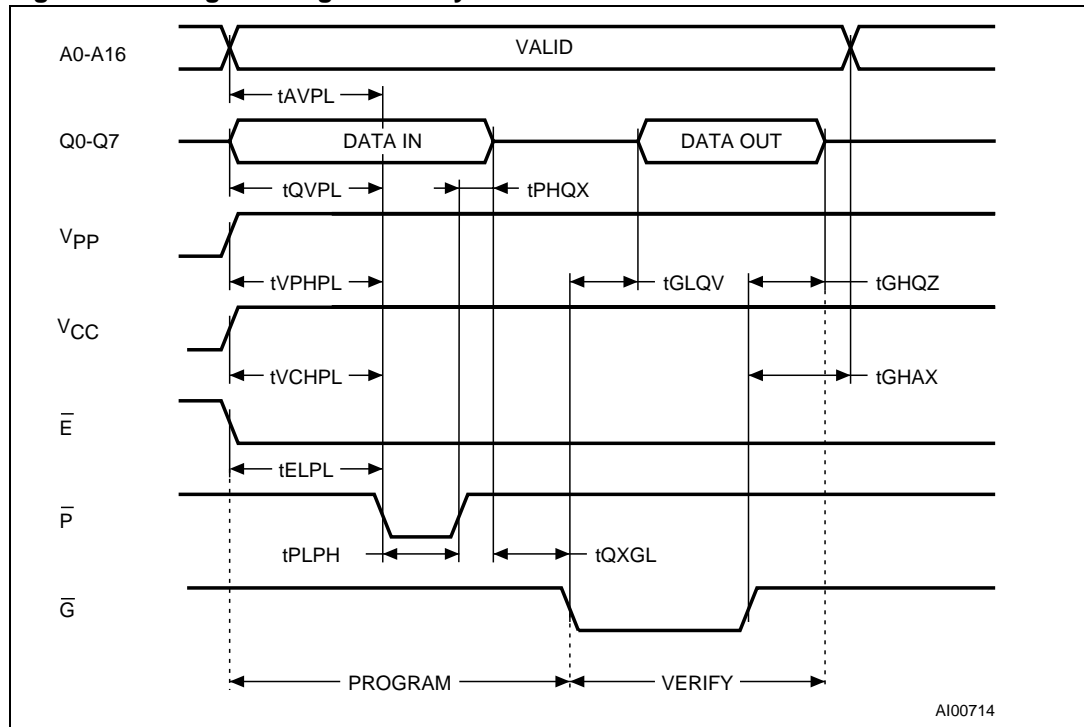
$T_A = 25\text{ }^\circ\text{C}$; $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$; $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$

Table 11. Programming Mode AC Characteristics (1)

| Symbol | Alt | Parameter | Test Condition | Min. | Max. | Unit |
|------------------|-----------|--|----------------|------|------|---------------|
| t_{AVPL} | t_{AS} | Address Valid to Program Low | | 2 | | μs |
| t_{QVPL} | t_{DS} | Input Valid to Program Low | | 2 | | μs |
| t_{VPHPL} | t_{VPS} | V_{PP} High to Program Low | | 2 | | μs |
| t_{VCHPL} | t_{VCS} | V_{CC} High to Program Low | | 2 | | μs |
| t_{ELPL} | t_{CES} | Chip Enable Low to Program Low | | 2 | | μs |
| t_{PLPH} | t_{PW} | Program Pulse Width | | 95 | 105 | μs |
| t_{PHQX} | t_{DH} | Program High to Input Transition | | 2 | | μs |
| t_{QXGL} | t_{OES} | Input Transition to Output Enable Low | | 2 | | μs |
| t_{GLQV} | t_{OE} | Output Enable Low to Output Valid | | | 100 | ns |
| $t_{GHQZ}^{(2)}$ | t_{DFP} | Output Enable High to Output Hi-Z | | 0 | 130 | ns |
| t_{GHAX} | t_{AH} | Output Enable High to Address Transition | | 0 | | ns |

- V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .
- Sampled only, not 100% tested.

Figure 9. Programming and Verify Modes AC Waveforms



5 Package mechanical data

5.1 32-pin Ceramic Frit-seal DIP, with round window (FDIP32WA)

Figure 10. FDIP32WA package outline

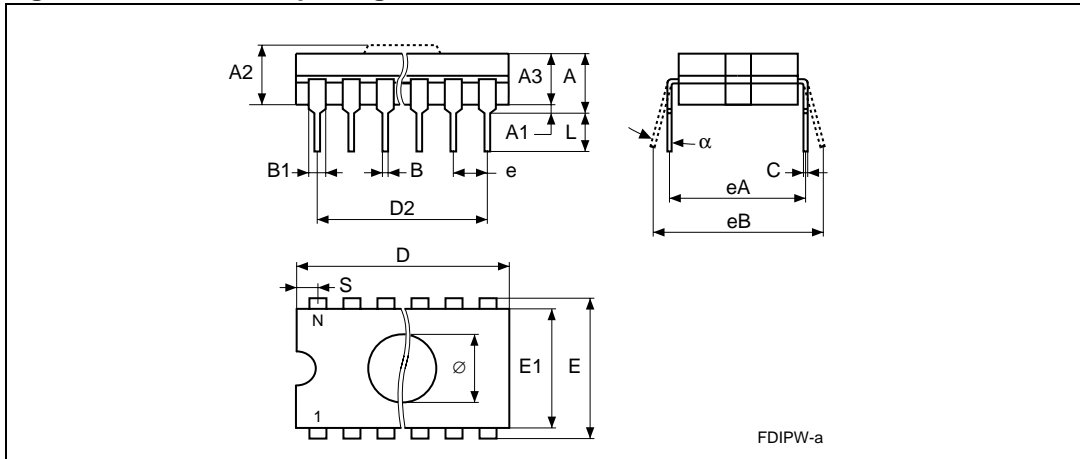


Table 12. FDIP32WA package mechanical data

| Symbol | millimeters | | | inches | | |
|--------|-------------|-------|-------|--------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 5.72 | | | 0.225 |
| A1 | 0.51 | | 1.40 | 0.020 | | 0.055 |
| A2 | 3.91 | | 4.57 | 0.154 | | 0.180 |
| A3 | 3.89 | | 4.50 | 0.153 | | 0.177 |
| B | 0.41 | | 0.56 | 0.016 | | 0.022 |
| B1 | | 1.45 | | | 0.057 | |
| C | 0.23 | | 0.30 | 0.009 | | 0.012 |
| D | 41.73 | | 42.04 | 1.643 | | 1.655 |
| D2 | | 38.10 | | | 1.500 | |
| e | | 2.54 | | | 0.100 | |
| E | | 15.24 | | | 0.600 | |
| E1 | 13.06 | | 13.36 | 0.514 | | 0.526 |
| eA | | 14.99 | | | 0.590 | |
| eB | 16.18 | | 18.03 | 0.637 | | 0.710 |
| L | 3.18 | | 4.10 | 0.125 | | 0.161 |
| N | | 32 | | | 32 | |
| S | 1.52 | | 2.49 | 0.060 | | 0.098 |
| Ø | | 7.11 | | | 0.280 | |
| α | 4° | | 11° | 4° | | 11° |

5.2 32-pin Plastic DIP, 600 mils width (PDIP32)

Figure 11. PDIP32 package outline

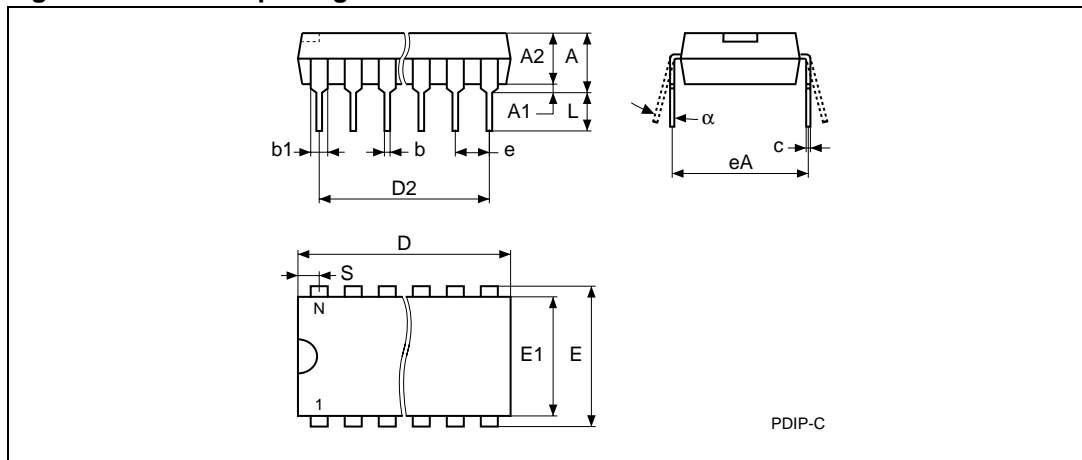


Table 13. PDIP32 package mechanical data

| Symbol | millimeters | | | inches | | |
|----------|-------------|-------|-------|--------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 4.83 | | | 0.190 |
| A1 | 0.38 | | | 0.015 | | |
| A2 | | 3.81 | | | 0.150 | |
| b | 0.41 | | 0.53 | 0.016 | | 0.021 |
| b1 | 1.14 | | 1.65 | 0.045 | | 0.065 |
| c | 0.23 | | 0.38 | 0.009 | | 0.015 |
| D | 41.78 | | 42.29 | 1.645 | | 1.665 |
| D2 | | 38.10 | | | 1.500 | |
| eA | | 15.24 | | | 0.600 | |
| e | | 2.54 | | | 0.100 | |
| E | 15.24 | | 15.88 | 0.600 | | 0.625 |
| E1 | 13.46 | | 13.97 | 0.530 | | 0.550 |
| S | 1.65 | | 2.21 | 0.065 | | 0.087 |
| L | 3.05 | | 3.56 | 0.120 | | 0.140 |
| α | 0° | | 15° | 0° | | 15° |
| N | | 32 | | | 32 | |

5.3 32-lead Rectangular Plastic Leaded Chip Carrier (PLCC32)

Figure 12. PLCC32 package outline

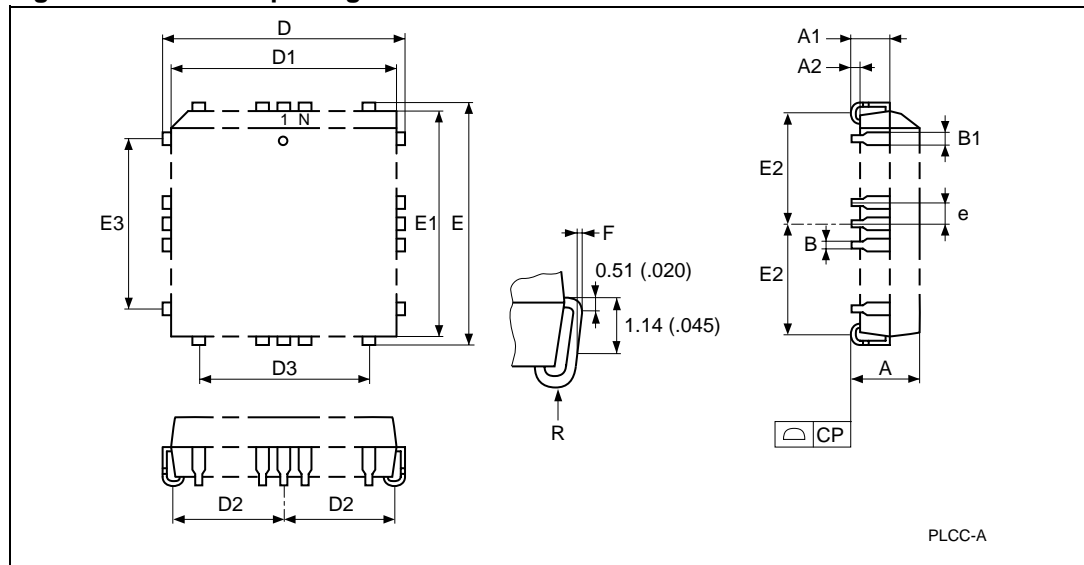


Table 14. PLCC32 package mechanical data

| Symbol | millimeters | | | inches | | |
|--------|-------------|-------|-------|--------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 3.18 | | 3.56 | 0.125 | | 0.140 |
| A1 | 1.53 | | 2.41 | 0.060 | | 0.095 |
| A2 | 0.38 | | | 0.015 | | |
| B | 0.33 | | 0.53 | 0.013 | | 0.021 |
| B1 | 0.66 | | 0.81 | 0.026 | | 0.032 |
| CP | | | 0.10 | | | 0.004 |
| D | 12.32 | | 12.57 | 0.485 | | 0.495 |
| D1 | 11.35 | | 11.51 | 0.447 | | 0.453 |
| D2 | 4.78 | | 5.66 | 0.188 | | 0.223 |
| D3 | | 7.62 | | | 0.300 | |
| E | 14.86 | | 15.11 | 0.585 | | 0.595 |
| E1 | 13.89 | | 14.05 | 0.547 | | 0.553 |
| E2 | 6.05 | | 6.93 | 0.238 | | 0.273 |
| E3 | | 10.16 | | | 0.400 | |
| e | | 1.27 | | | 0.050 | |
| F | 0.00 | | 0.13 | 0.000 | | 0.005 |
| R | | 0.89 | | | 0.035 | |
| N | | 32 | | | 32 | |

5.4 32-lead Plastic Thin Small Outline, 8x20 mm (TSOP32)

Figure 13. TSOP32 package outline

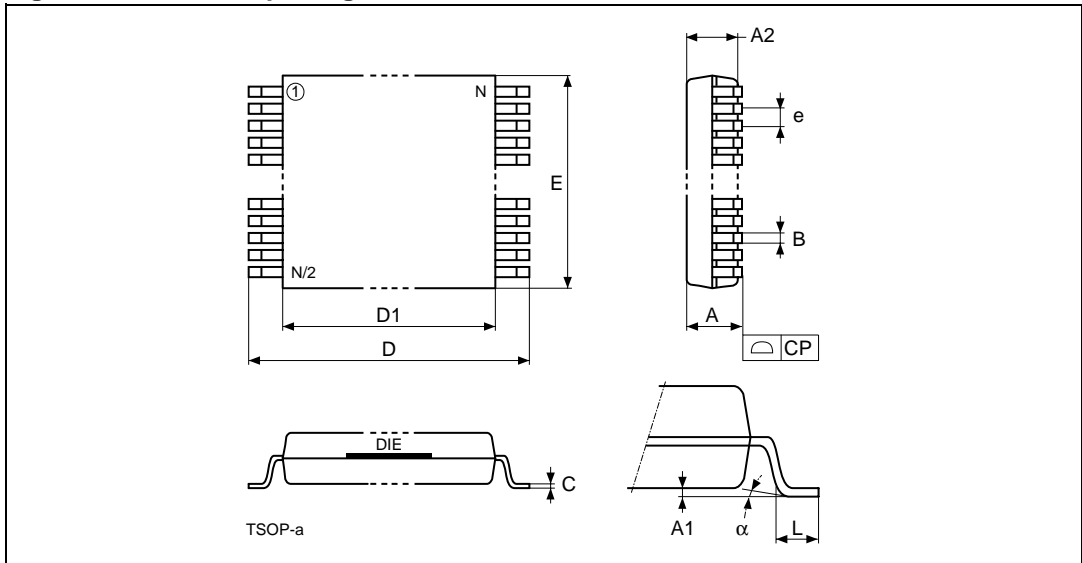


Table 15. TSOP32 package mechanical data

| Symbol | millimeters | | | inches | | |
|----------|-------------|-------|--------|--------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.200 | | | 0.0472 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 0.950 | | 1.050 | 0.0374 | | 0.0413 |
| B | 0.170 | | 0.250 | 0.0067 | | 0.0098 |
| C | 0.100 | | 0.210 | 0.0039 | | 0.0083 |
| CP | | | 0.100 | | | 0.0039 |
| D | 19.800 | | 20.200 | 0.7795 | | 0.7953 |
| D1 | 18.300 | | 18.500 | 0.7205 | | 0.7283 |
| e | | 0.500 | | | 0.0197 | |
| E | 7.900 | | 8.100 | 0.3110 | | 0.3189 |
| L | 0.500 | | 0.700 | 0.0197 | | 0.0276 |
| N | | 32 | | | 32 | |
| α | 0° | | 5° | 0° | | 5° |

6 Part numbering

Table 16. Ordering information scheme

| | | | | | | |
|---|----------|-----|---|---|---|----|
| Example: | M27C1001 | -35 | X | C | 1 | TR |
| Device Type M27 | | | | | | |
| Supply Voltage C = 5V | | | | | | |
| Device Function 1001 = 1 Mbit (128Kb x 8) | | | | | | |
| Speed -35 ⁽¹⁾ = 35 ns -10 = 100 ns -45 = 45 ns -12 = 120 ns -60 = 60 ns -15 = 150 ns -70 = 70 ns -20 = 200 ns -80 = 80 ns -25 = 250 ns -90 = 90 ns | | | | | | |
| V_{CC} Tolerance blank = ± 10% X = ± 5% | | | | | | |
| Package F = FDIP32W C = PLCC32 B = PDIP32 N = TSOP32: 8 x 20 mm | | | | | | |
| Temperature Range 1 = 0 to 70 °C 3 = -40 to 125 °C 6 = -40 to 85 °C | | | | | | |
| Options TR = ECOPACK® package, Tape & Reel Packing | | | | | | |

1. High Speed, see AC Characteristics section for further information.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

7 Revision history

Table 17. Document revision history

| Date | Revision | Changes |
|----------------|----------|--|
| September 1998 | 1 | First Issue |
| 24-Jan-2000 | 2 | 35ns speed class added (Table 8A, Table 16) |
| 20-Sep-2000 | 3 | AN620 Reference removed |
| 04-Jun-2002 | 4 | PLCC32 Package mechanical data and drawing clarified (Table 14 and Figure 12) TSOP32 Package mechanical data clarified (Table 15) |
| 12-Apr-2006 | 5 | Removed LCC32W package and Additional Burn-in option. Converted to new template. Added ECOPACK® information. |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED REPRESENTATIVE OF ST, ST PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS, WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2006 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com