

KM416C1000B, KM416C1200B KM416V1000B, KM416V1200B

CMOS DRAM

1M x 16Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-5,-6 or -7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 1Mx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

Part Identification

- KM416C1000B/B-L (5V, 4K Ref.)
- KM416C1200B/B-L (5V, 1K Ref.)
- KM416V1000B/B-L (3.3V, 4K Ref.)
- KM416V1200B/B-L (3.3V, 1K Ref.)

Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-5	396	576	605	880
-6	360	540	550	825
-7	324	504	495	770

Refresh Cycles

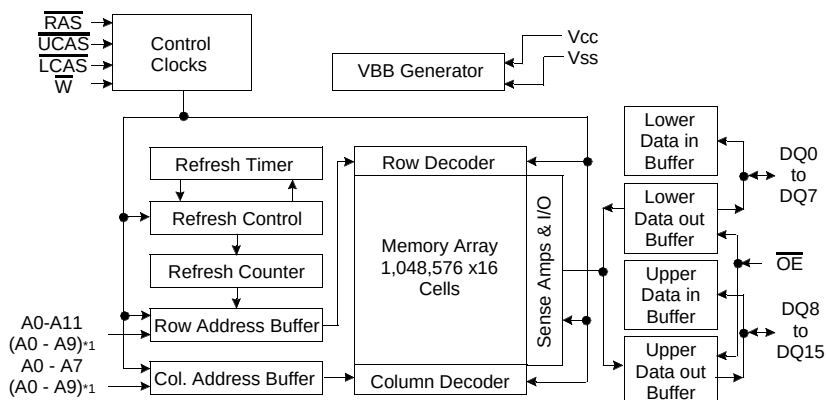
Part NO.	VCC	Refresh cycle	Refresh period	
			Normal	L-ver
C1000B	5V	4K	64ms	128ms
V1000B	3.3V			
C1200B	5V	1K	16ms	128ms
V1200B	3.3V			

Performance Range

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{PC}	Remark
-5	50ns	15ns	90ns	35ns	5V/3.3V
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V

- Fast Page Mode operation
- 2 $\overline{\text{CAS}}$ Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in 42-pin SOJ 400mil and 50(44)-pin TSOP(II) 400mil packages
- Single +5V $\pm 10\%$ power supply (5V product)
- Single +3.3V $\pm 0.3V$ power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



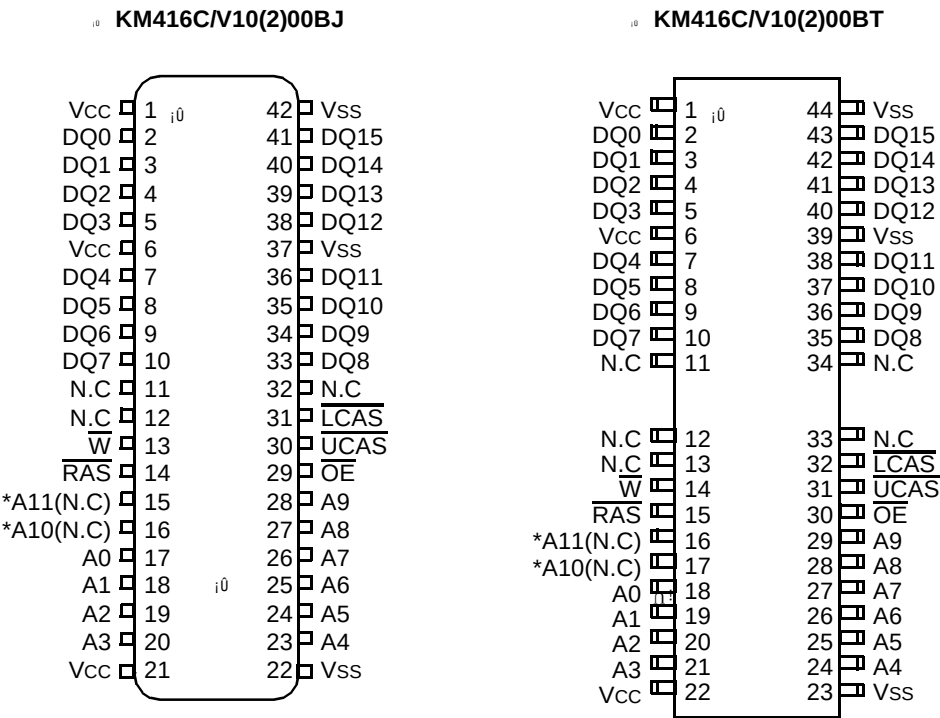
Note) *1 : 1K Refresh

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.



ELECTRONICS

PIN CONFIGURATION (Top Views)



*A10 and A11 are N.C for KM416C/V1200B(5V/3.3V, 1K Ref. product)

J : 400mil 42 SOJ
T : 400mil 50(44) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A9	Address Inputs (1K Product)
DQ0 - 15	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5V)
	Power(+3.3V)
N.C	No Connection

KM416C1000B, KM416C1200B KM416V1000B, KM416V1200B

CMOS DRAM

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	2.4	-	V _{CC} +1.0 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	-1.0 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Max	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{IN} +0.3V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-5	5	μA
	Output High Voltage Level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{IN} +0.5V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-5	5	μA
	Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

KM416C1000B, KM416C1200B KM416V1000B, KM416V1200B

CMOS DRAM

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max				Units
			KM416V1000B	KM416V1200B	KM416C1000B	KM416C1200B	
I _{CC1}	Don't care	-5	110	160	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
I _{CC2}	Normal L	Don't care	2	2	2	2	mA
			1	1	1	1	mA
I _{CC3}	Don't care	-5	110	160	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
I _{CC4}	Don't care	-5	100	100	100	100	mA
		-6	90	90	90	90	mA
		-7	80	80	80	80	mA
I _{CC5}	Normal L	Don't care	1	1	1	1	mA
			200	200	200	200	uA
I _{CC6}	Don't care	-5	110	160	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
I _{CC7}	L	Don't care	400	300	450	350	uA
I _{CCS}	L	Don't care	200	200	250	250	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{UCAS}$, $\overline{LCAS}$ cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$)

I_{CC3}* : $\overline{RAS}$ -only Refresh Current ($\overline{UCAS}=\overline{LCAS}=V_{IH}$, $\overline{RAS}$ cycling @t_{RC}=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}=V_{IL}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @t_{PC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @t_{RC}=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$ =0.2V,

Din=Don't care, t_{RC}=31.25us(4K/L-ver), 125us(1K/L-ver),

t_{RAS}=t_{RASmin}~300ns

I_{CCS} : Self Refresh Current

$\overline{RAS}=\overline{UCAS}=\overline{LCAS}=V_{IL}$, $\overline{W}=\overline{OE}=A_0 \sim A_{11}=V_{CC}-0.2V$ or 0.2V,

DQ0 ~ DQ15=V_{CC}-0.2V, 0.2V or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC}.



KM416C1000B, KM416C1200B KM416V1000B, KM416V1200B

CMOS DRAM

CAPACITANCE ($T_A=25^\circ\text{C}$, $V_{CC}=5\text{V}$ or 3.3V , $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A11]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ15]	CDQ	-	7	pF

AC CHARACTERISTICS ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, See note 1,2)

Test condition (5V device) : $V_{CC}=5.0\text{V} \pm 10\%$, $V_{ih}/V_{il}=2.4/0.8\text{V}$, $V_{oh}/V_{ol}=2.4/0.4\text{V}$

Test condition (3.3V device) : $V_{CC}=3.3\text{V} \pm 0.3\text{V}$, $V_{ih}/V_{il}=2.2/0.7\text{V}$, $V_{oh}/V_{ol}=2.0/0.8\text{V}$

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		ns	
Read-modify-write cycle time	t _{RWC}	133		155		185		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		50		60		70	ns	3,4,9
Access time from $\overline{\text{CAS}}$	t _{CAC}		15		15		20	ns	3,4
Access time from column address	t _{AA}		25		30		35	ns	3,9
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t _{OFF}	0	13	0	15	0	20	ns	5
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	30		40		50		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10K	60	10K	70	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	13		15		20		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	50		60		70		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	13	10K	15	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	37	20	45	20	50	ns	4
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	15	35	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		ns	10
Column address hold time	t _{CAH}	10		10		15		ns	10
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	25		30		35		ns	
Read command set-up time	t _{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	7
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	7
Write command hold time	t _{WCH}	10		10		15		ns	
Write command pulse width	t _{WP}	10		10		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	13		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	t _{DS}	0		0		0		ns	8,16
Data hold time	t _{DH}	10		10		15		ns	8,16
Refresh period (1K, Normal)	t _{REF}		16		16		16	ms	
Refresh period (4K, Normal)	t _{REF}		64		64		64	ms	
Refresh period (L-ver)	t _{REF}		128		128		128	ms	
Write command set-up time	t _{WCS}	0		0		0		ns	6
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	36		40		50		ns	6,12
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	73		85		95		ns	6
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	48		55		60		ns	6
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t _{CPWD}	53		60		65		ns	6
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CSR}	5		5		5		ns	14
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		10		15		ns	15
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time (CBR counter test cycle)	t _{CPT}	20		20		25		ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		30		35		40	ns	3
Fast Page mode cycle time	t _{PC}	35		40		45		ns	
Fast Page read-modify-write cycle time	t _{PRWC}	76		80		95		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	t _{CP}	10		10		10		ns	11
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t _{RASP}	50	200K	60	200K	70	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	30		35		40		ns	
$\overline{\text{OE}}$ access time	t _{OEA}		13		15		20	ns	3
$\overline{\text{OE}}$ to data delay	t _{OED}	13		15		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	t _{OEZ}	0	13	0	15	0	20	ns	
$\overline{\text{OE}}$ command hold time	t _{OEH}	13		15		20		ns	
$\overline{\text{RAS}}$ pulse width (C-B-R self refresh)	t _{RASS}	100		100		100		us	17
$\overline{\text{RAS}}$ precharge time (C-B-R self refresh)	t _{RPS}	90		110		130		ns	17
$\overline{\text{CAS}}$ hold time (C-B-R self refresh)	t _{CHS}	-50		-50		-50		ns	17

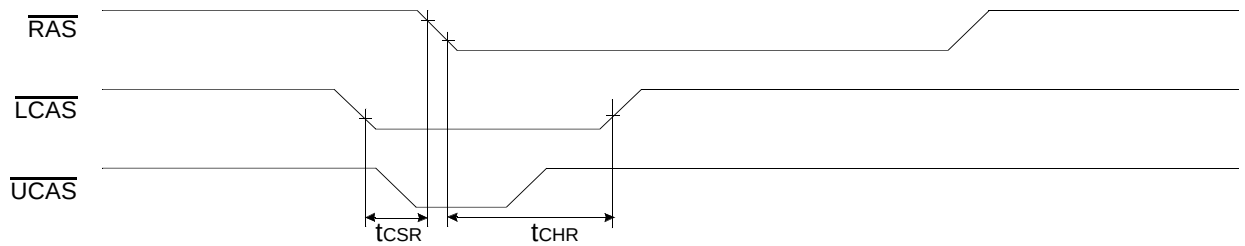
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or $\overline{\text{CBR}}$ cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL} . $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1TTL(3.3V) loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
6. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \leq t_{\text{WCS}}(\text{min})$, the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \leq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \leq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \leq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \leq t_{\text{CPWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in ealy write cycles and to the $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
9. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .

KM416C/V10(2)00B/BL Truth Table

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ0 - DQ7	DQ8-DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

10. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{CAS}$ rising edge.
11. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
12. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
13. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
14. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
15. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



16. t_{DS} , t_{DH} is independently specified for lower byte $D_{IN}(0-7)$, upper byte $D_{IN}(8-15)$
17. 4096(4K Ref.)/1024(1K Ref.) of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification (L-version).

This datasheet has been downloaded from:

www.DatasheetCatalog.com

Datasheets for electronic components.