M2732A
32K (4K x 8) UV ERASABLE PROM

Military

- **250 ns (M2732A-25) Maximum Access Time ... HMOS* -E Technology**
- **Compatible to High Speed 5 MHz MiAPX 86/10 MPU ... Zero Wait State**
- **Military Temperature Range: −55°C to +125°C (T_C)**
- **Industry Standard Pinout ... JEDEC Approved**
- **Two Line Control**
- **Low Standby Current ... 35 mA Max.**

The Intel M2732A is a 5V only, 32,768 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard M2732A's access time is 450 ns with speed selection (M2732A-25) available at 250 ns. The access time is compatible to high performance microprocessors, such as the 5 MHz MiAPX 86/10. In these systems, the M2732A allows the microprocessor to operate without the addition of WAIT states.

An important M2732A feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The M2732A has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 115 mA, while the maximum standby current is only 35 mA, a 66% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

The M2732A is fabricated with HMOS-E technology, Intel's high speed N-channel MOS Silicon Gate Technology.

*HMOS is a patented process of Intel Corporation.

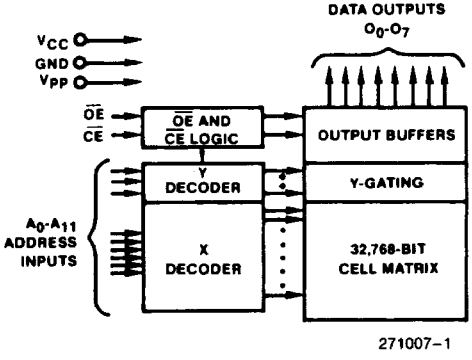

Figure 1. Block Diagram

Mode Selection

Mode \ Pins	CE (18)	OE/V_{PP} (20)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

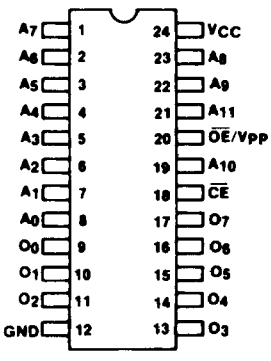

Figure 2. Configuration

Pin Names

A_0-A_{11}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0-O_7	Outputs

October 1986
Order Number: 271007-001

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages with Respect to Ground . . . . . +6V to −0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming . . . . +22V to −0.3V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. AND A.C. OPERATING CONDITIONS DURING READ

	M2732A-25	M2732A-45
Operating Temperature Range (T_C)	−55°C to +125°C	−55°C to +125°C
V_{CC} Power Supply	5V ±10%	5V ±10%

READ OPERATION

D.C. CHARACTERISTICS

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ(1)	Max		
I_{IL}	Input Load Current			10	μA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.5V
I_{CC1}	V_{CC} Current (Standby)			35	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}	V_{CC} Current (Active)			115	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} ±400 μA

NOTE:
1. Typical values are for T_C = 25°C and nominal supply voltages.

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A.C. CHARACTERISTICS

Symbol	Parameter	M2732A-25			M2732A-45			Unit	Test Conditions
		Min	Typ(1)	Max	Min	Typ(1)	Max		
t_{ACC}	Address to Output Delay			250			450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay			250			450	ns	$\overline{OE}$ = V_{IL}
t_{OE}	Output Enable to Output Delay	10		100	10		150	ns	$\overline{CE}$ = V_{IL}
t_{DF}(2)	Output Enable High to Output Float	0		90	0		130	ns	$\overline{CE}$ = V_{IL}
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0			0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

CAPACITANCE (1), (2)

T_C(5) = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

A.C. TEST CONDITIONS

Output Load ..... 1 TTL gate, 100Ω Resistor and C_L = 100 pF

Input Rise and Fall Times ..... ≤20 ns

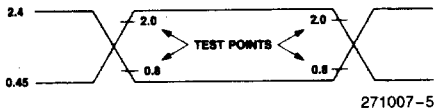
Input Pulse Levels ..... 0.45V to 2.4V

Timing Measurement Reference Level

Inputs ..... 0.8V and 2V

Outputs ..... 0.8V and 2V

A.C. TESTING, OUTPUT WAVEFORM



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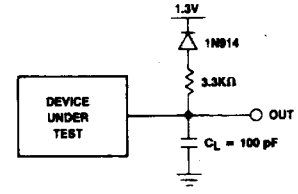
A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

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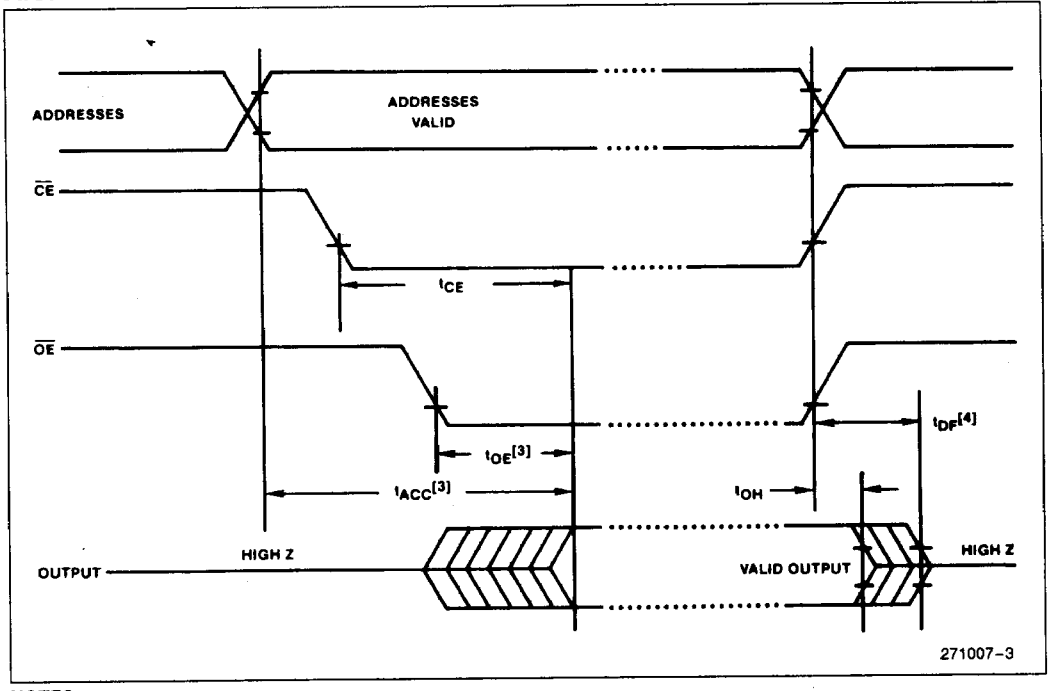
A.C. WAVEFORMS



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NOTES:

1. Typical values are for T_C = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven.
5. Case temperatures are "instant on".

DEVICE OPERATION

The five modes of operation of the M2732A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 21V.

Table 1. Mode Selection

Mode \ Pins	CE (18)	OE/V_{PP} (20)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Read Mode

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The M2732A has a standby mode which reduces the active power current by 66%, from 115 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the outputs pins are only active when data is desired from a particular memory device.

Programming

Programming is the same as Intel's M2732 except for the programming voltage. In the program mode the M2732A $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 21V (25V for the M2732). ***Exceeding 21.5V will damage the M2732A.***

Initially, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The M2732A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of the multiple M2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled M2732As.

Program Inhibit

Programming of multiple M2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M2732As may be common. A TTL level program pulse applied to a M2732A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that M2732A. A high level $\overline{CE}$ input inhibits the other M2732As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

ERASURE CHARACTERISTICS

The erasure characteristics of the M2732A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the M2732A window to prevent unintentional erasure.

The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M2732A should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

PROGRAMMING

D.C. PROGRAMMING CHARACTERISTICS(1)

T_C = 25°C ±5°C; V_{CC} = 5V ±5%; V_{PP} = 21V ±0.5V

Symbol	Parameter	Limits				Test Conditions
		Min	Typ	Max	Unit	
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{OL}	Output Low Voltage During Verify			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4			V	I_{OH} = −400 μA
I_{CC}	V_{CC} Supply Current		85	125	mA	
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except OE/V_{PP})	2.0		V_{CC} + 1	V	
I_{PP}	V_{PP} Supply Current			35	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$

NOTE:
1. When programming the M2732A, a 0.1 μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

A.C. PROGRAMMING CHARACTERISTICS

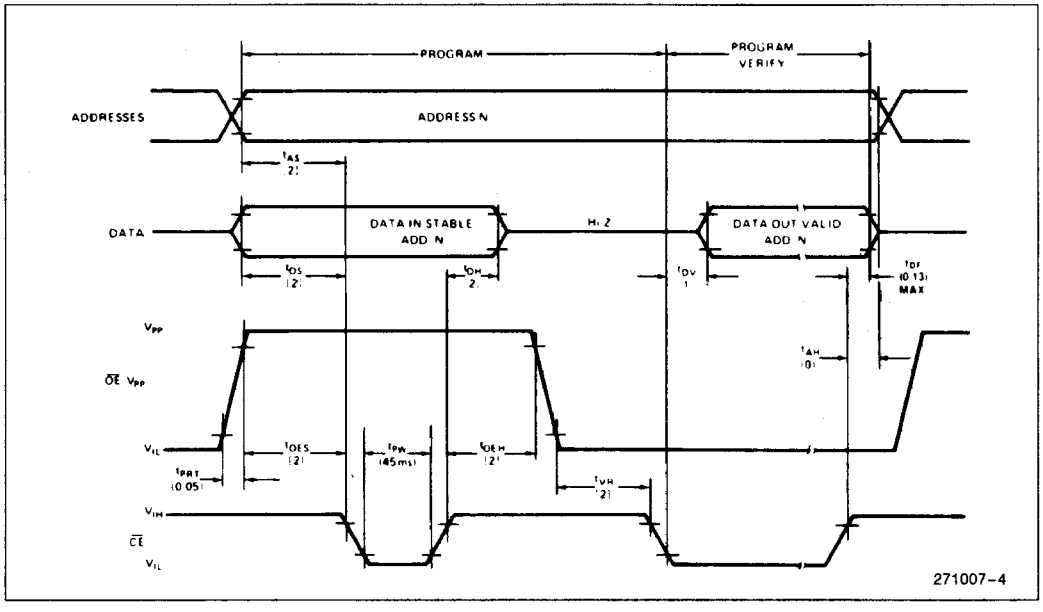
T_C = 25°C ±5°C; V_{CC} = 5V ±5%; V_{PP} = 21V ±0.5V

Symbol	Parameter	Limits				Test Conditions*
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{OEH}	OE Hold Time	2			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DF}	Chip Enable to Output Float Delay	0		130	ns	
t_{DV}	Data Valid from $\overline{CE}$			1	µs	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}
t_{PW}	$\overline{CE}$ Pulse Width During Programming	45	50	55	ms	
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming	50			ns	
t_{VR}	V_{PP} Recovery Time	2			µs	

*A.C. TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 1.0V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

PROGRAMMING WAVEFORMS



NOTES:
1. All times shown in ( ) are minimum and in µs unless otherwise specified.
2. The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.