M5M417800DJ,TP -5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (2097152-WORD BY 8-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.
The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417800DXX-5,-5S	50	13	25	13	90	655
M5M417800DXX-6,-6S	60	15	30	15	110	540
M5M417800DXX-7,-7S	70	20	35	20	130	475

XX=J,TP

- Standard 28 pin SOJ,28 pin TSOP
- Single 5V ±10%supply
- Low stand-by power dissipation
  - 2.75mW (Max) ---------- CMOS Input level
  - 1.10mW (Max)* ---------- CMOS Input level
- Low operating power dissipation
  - M5M417800Dxx- 5,-5S ---------- 800.0mW (Max)
  - M5M417800Dxx- 6,-6S ---------- 660.0mW (Max)
  - M5M417800Dxx- 7,-7S ---------- 580.0mW (Max)
- Self refresh capability*
  - self refresh current ---------- 200.0µA(Max)
- Fast-page mode , Read-modify-write,$\overline{RAS}$-only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
  Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A_0~A_{10})
  - *Applicable to self refresh version (M5M417800DJ,TP -5S,-6S,-7S : option only)

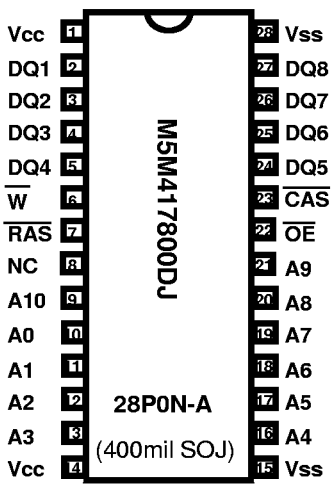
APPLICATION

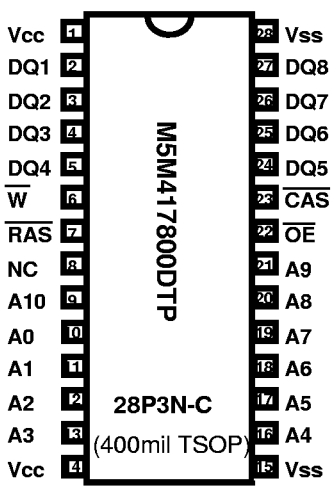
Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin Name	Function
A_0-A_{10}	Address Inputs
DQ1-DQ8	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)





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FUNCTION

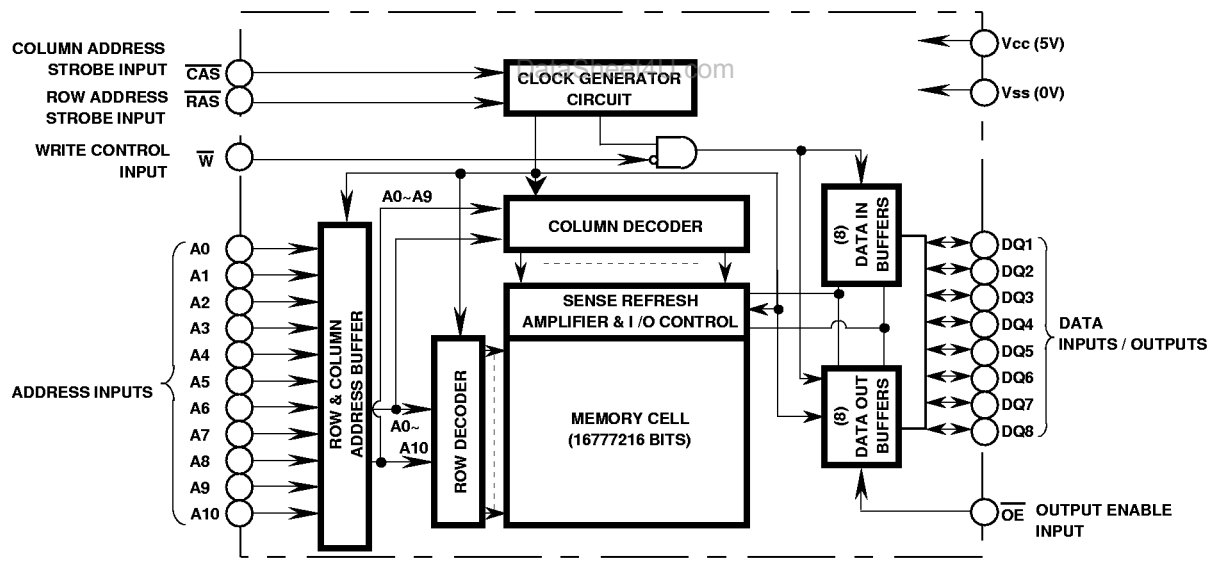
In addition to normal read, write, and read-modify-write operations, the M5M417800DJ, TP provide a number of other functions, e.g., fast page mode, $\overline{RAS}$ only refresh, and delayed-write. The input condition and output state for each mode are shown in Table 1.

Table 1 Input condition and output state for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1 ~ 7	V
VI	Input voltage		-1 ~ 7	V
V0	Output voltage		-1 ~ 7	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss

** : ViL(min.) is -2.0V when undershoot width is less than 25ns.(The width is defined as the period when the voltage level below Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ 5.5V	-10		10	µA
I_I	Input current		0V ≤ V_{IN} ≤ 5.5V, Other inputs pins=0V	-10		10	µA
$I_{CC1\ (AV)}$	Average supply current from Vcc operating (Note 3,4)	M5M417800D-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			145	mA
		M5M417800D-6,-6S				120	
		M5M417800D-7,-7S				105	
I_{CC2}	Supply current from Vcc , stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≥ Vcc -0.2V,output open			0.5	
$I_{CC3\ (AV)}$	Average supply current from Vcc refreshing (Note 3)	M5M417800D-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			145	mA
		M5M417800D-6,-6S				120	
		M5M417800D-7,-7S				105	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	M5M417800D-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M417800D-6,-6S				70	
		M5M417800D-7,-7S				60	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M417800D-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			145	mA
		M5M417800D-6,-6S				120	
		M5M417800D-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.

3: Icc1 (AV), Icc3 (AV) , Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I\ (A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I\ (CLK)}$	Input capacitance, clock inputs				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

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SWITCHING CHARACTERISTICS (Ta=0 ~70 °C, Vcc=5V ±10%, Vss=0V, unless otherwise noted , see notes 5,12,13)

Symbol	Parameter	Limits						Unit
		M5M417800D-5,-5S		M5M417800D-6,-6S		M5M417800D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$ (Note 6,7)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 6,8)		50		60		70	ns
t_{AA}	Column address access time (Note 6,9)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (Note 6,10)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$ (Note 6)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low (Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 11)	0	13	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (Note 11)	0	13	0	15	0	15	ns

Note 5: An initial pause of 500µs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-Only refresh cycles or by $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIHmin or lower than VILmax except $\overline{RAS}$ transition time.

6: Measured with a load circuit equivalent to 2TTL loads and 100pF.

7: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

8: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

9: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

10: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

11: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq$ I±10 µAI) with no reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted) (Notes 12,13)

Symbol	Parameter	Limits						Unit
		M5M417800D-5,-5S		M5M417800D-6,-6S		M5M417800D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time		32		32		32	ms
t_{REF*}	Refresh cycle time		128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note14)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note15)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note16)	0	7	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	13		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note17)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low (Note17)	0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note18)	13		15		15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data (Note18)	13		15		15		ns
t_T	Transition time (Note19)	1	50	1	50	1	50	ns

Note 12: The timing requirements are assumed t_T =5ns.

13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14: $t_{RCD(max)}$ is specified as a reference value only to guarantee the valid operation. If t_{RCD} is less than $t_{RCD(max)}$, access time is controlled by t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_H + t_{ASC(min)}$.

15: $t_{RAD(max)}$ is specified as a reference value only to guarantee the valid operation. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled by t_{AA}.

16: $t_{ASC(max)}$ is specified as a reference value only to guarantee the valid operation. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled by t_{CAC}.

17: Either t_{DZC} or t_{DZO} must be satisfied.

18: Either t_{CDD} or t_{ODD} must be satisfied.

19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M417800D-5,-5S		M5M417800D-6,-6S		M5M417800D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	25		30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M417800D-5,-5S		M5M417800D-6,-6S		M5M417800D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M417800D-5,-5S		M5M417800D-6,-6S		M5M417800D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note21)	131		155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	91	10000	105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	54	10000	60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	54		60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note22)	36		40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note22)	73		85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note22)	48		55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	8		10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		ns

Note 21: t_{RWC} is defined as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference values only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. Under conditions other than those specified above (for delayed write) ,DQ output(at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is invalid.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M417800D-5,-5S		M5M417800D-6,-6S		M5M417800D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	76		85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note24)	85	125000	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note25)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note22)	53		60		65		ns

Note 23: For those timing requirements which are not listed above, parameters of regular cycles are applicacble.

24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed. It is defined as $t_{RAS(min)} = t_{CSH(min)} + t_{CP(min)}$.

25: $t_{CP(max)}$ is specified as a reference value only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M417800D-5,-5S		M5M417800D-6,-6S		M5M417800D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc=5V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC8\ (AV)}$	Average supply current from Vcc Slow - Refresh cycle (note 5)	M5M417800D (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling or $\overline{RAS}$ cycling & $\overline{CAS}$ ≤ 0.2V $\overline{OE}$&$\overline{WE}$ ≤ 0.2V or OE&WE ≥ Vcc-0.2V A0 ~ A10 ≤ 0.2V or A0 ~ A10 ≥ Vcc-0.2V tREF=128mS (2048cycles) output = OPEN tRAS=tRASmin. ~1µS			500	µA
$I_{CC9\ (AV)}$ *	Average supply current from Vcc Self - Refresh cycle (note 5)	M5M417800D (S)	$\overline{RAS}$ = $\overline{CAS}$ ≤ 0.2V output = OPEN			200	µA

TIMING REQUIREMENTS (Ta=0 ~70 °C, Vcc=5V ±10%, Vss=0V, unless otherwise noted) (Notes 12,13)

Symbol	Parameter	Limits						Unit
		M5M417800D-5S		M5M417800D-6S		M5M417800D-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		µs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In the case of distributed refresh

The last / first full refresh cycles (2K) must be made within tNS / tSN before / after self refresh , on the condition that tNS≤ 32 ms and tSN ≤ 32 ms.

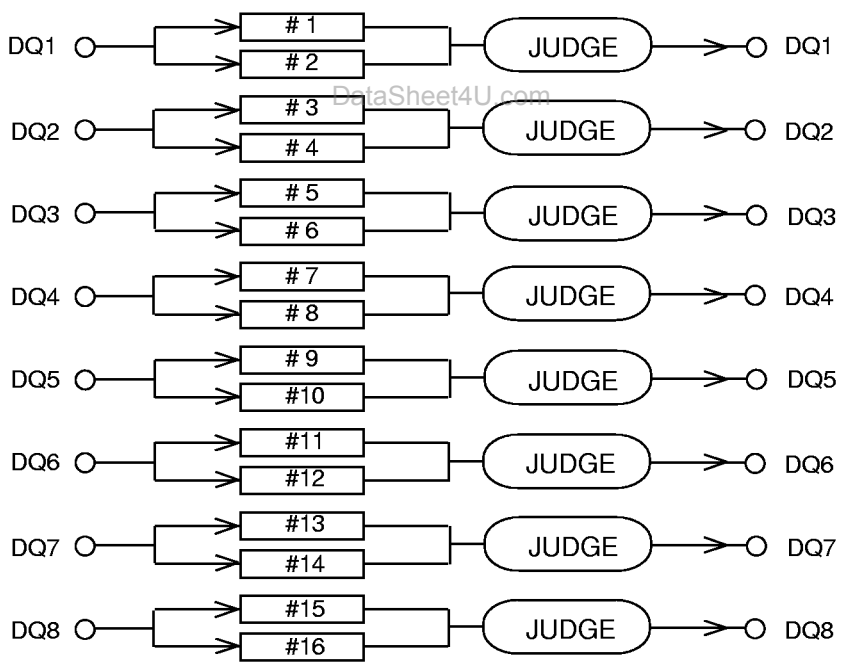
(2) In the case of burst refresh

The last / first full refresh cycles (2K) must be made within tNS / tSN before / after self refresh , on the condition that tNS + tSN ≤ 32 ms.

TEST Mode SET Cycle (Note 27)

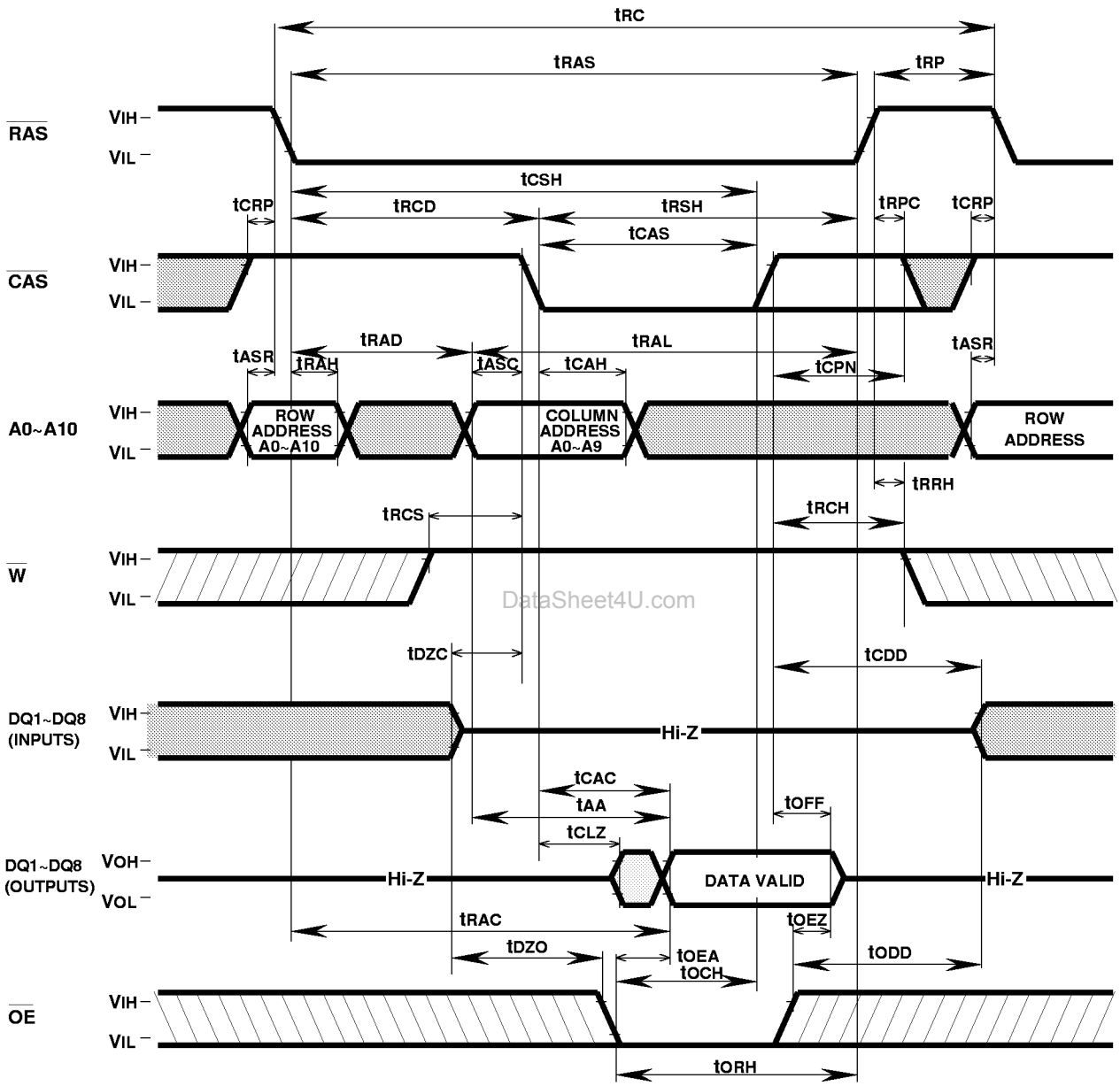
Symbol	Parameter	Limits						Unit
		M5M417800D-5,-5S		M5M417800D-6,-6S		M5M417800D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note27 : The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth) . Adreess of CA0 is not required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 2 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2 bits, respectively. High state indicates that they are same. Low state indicates that they are not same. These high and low outputs are used to determine Pass and Fail respectively.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 28)

Read Cycle

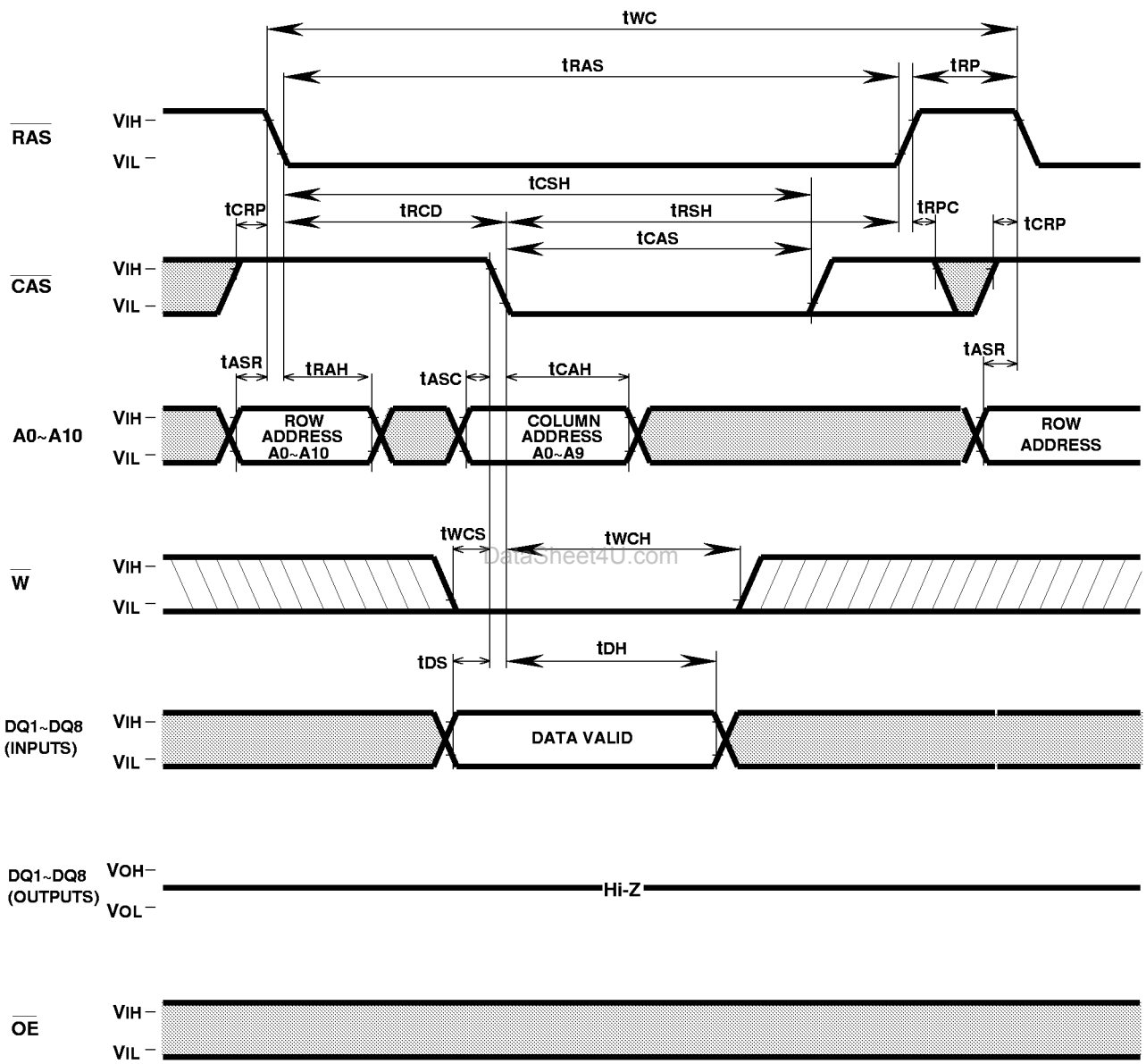


Note 28

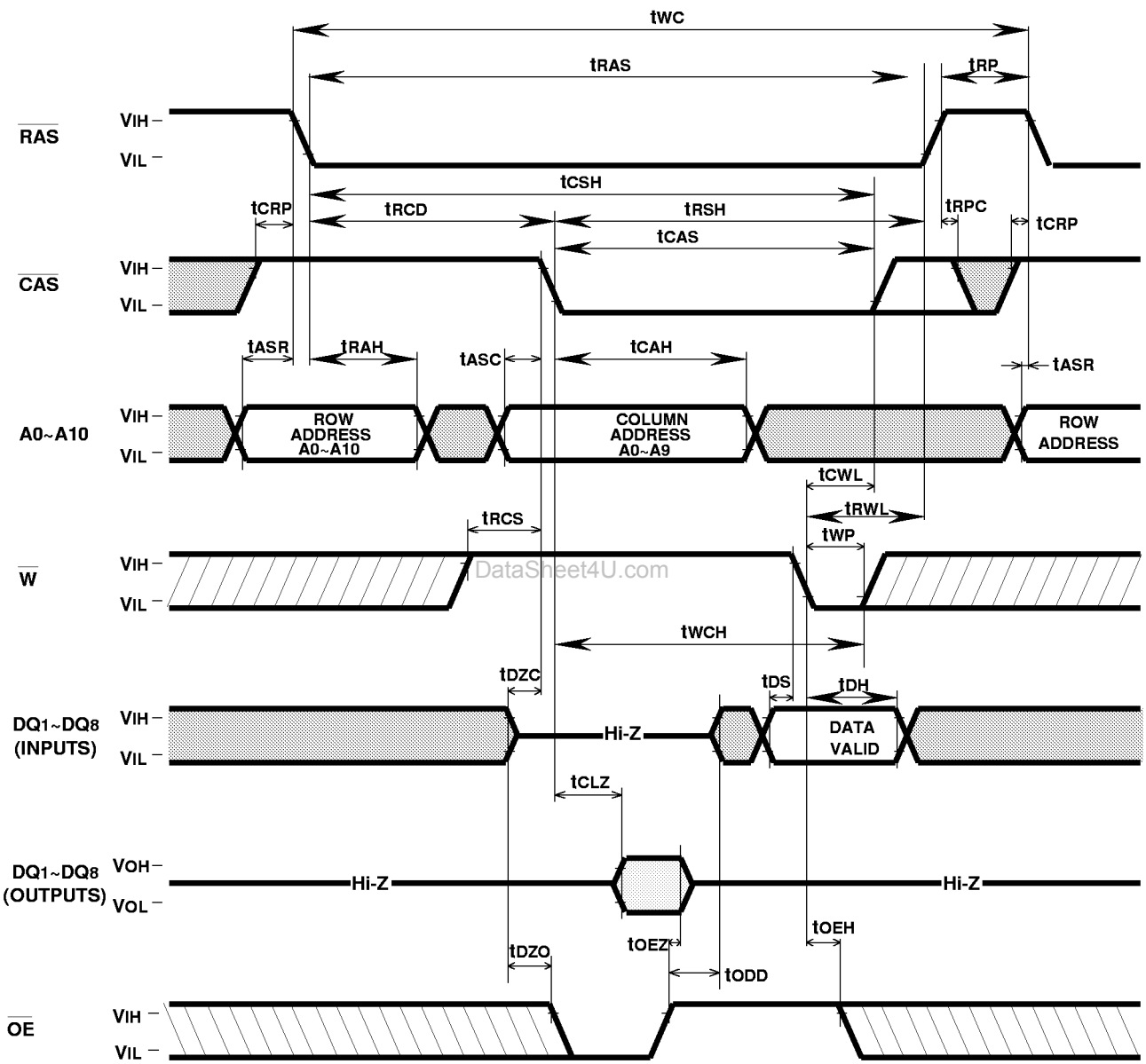
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

Write Cycle (Early write)



Write Cycle (Delayed write)



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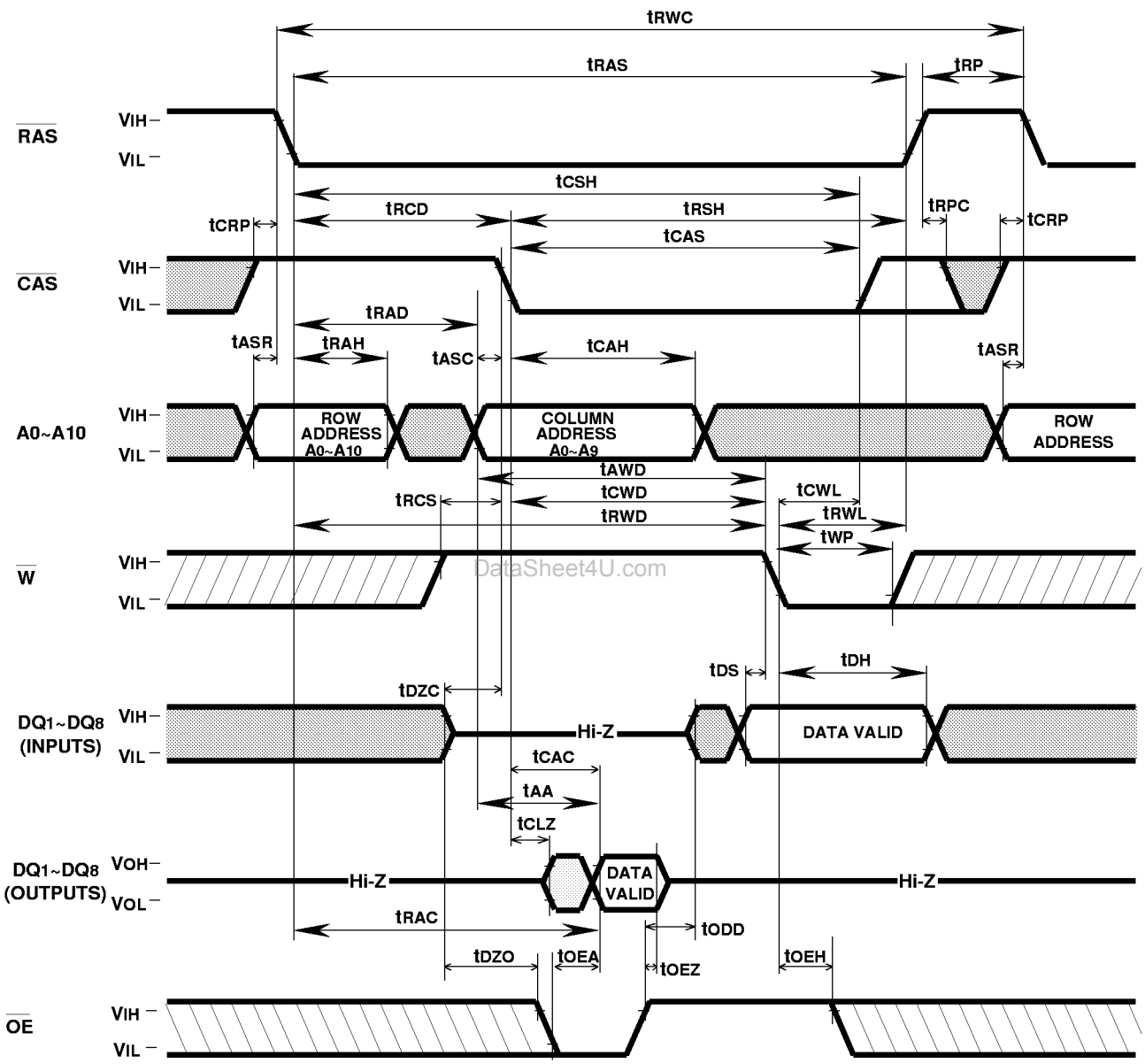
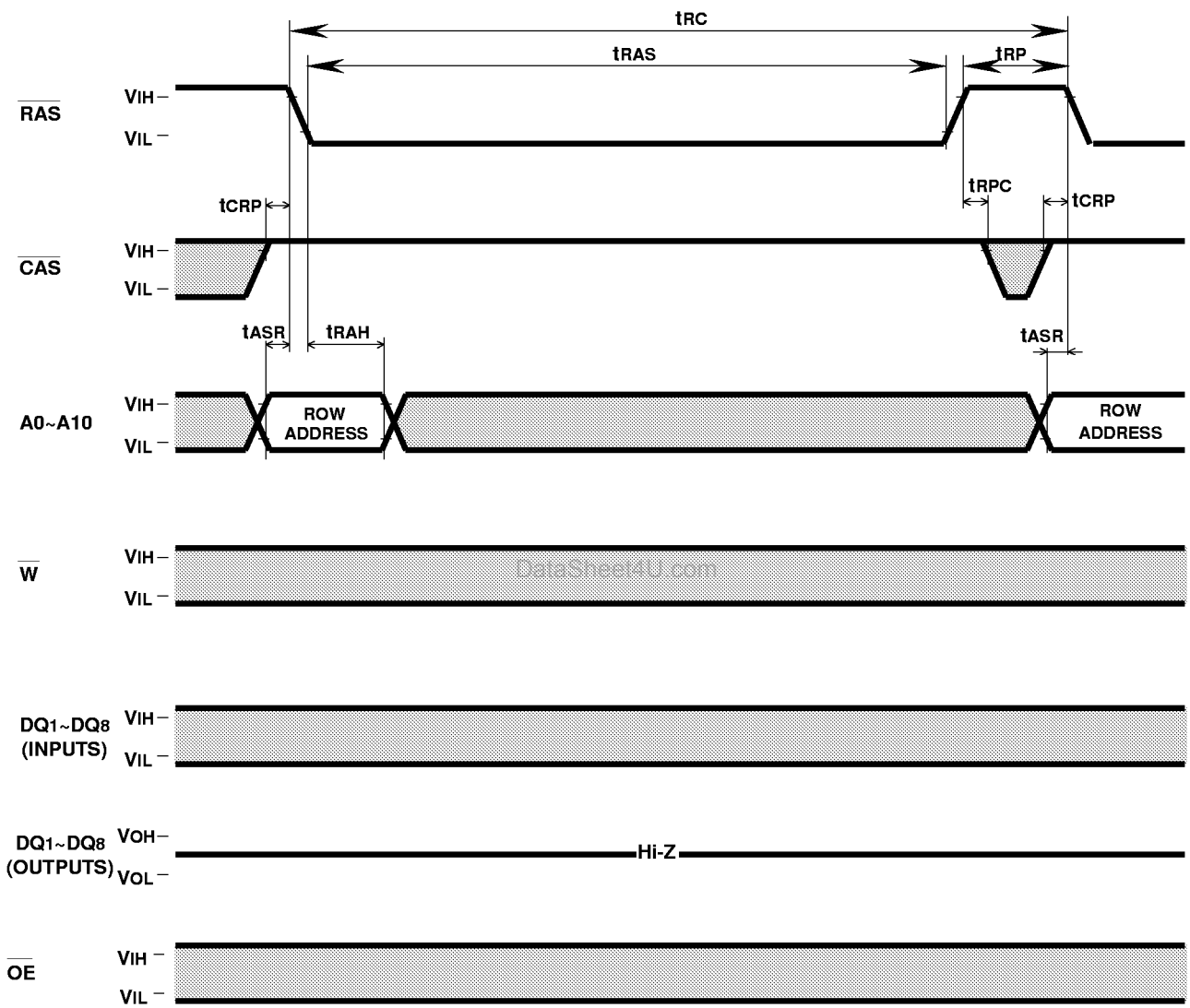
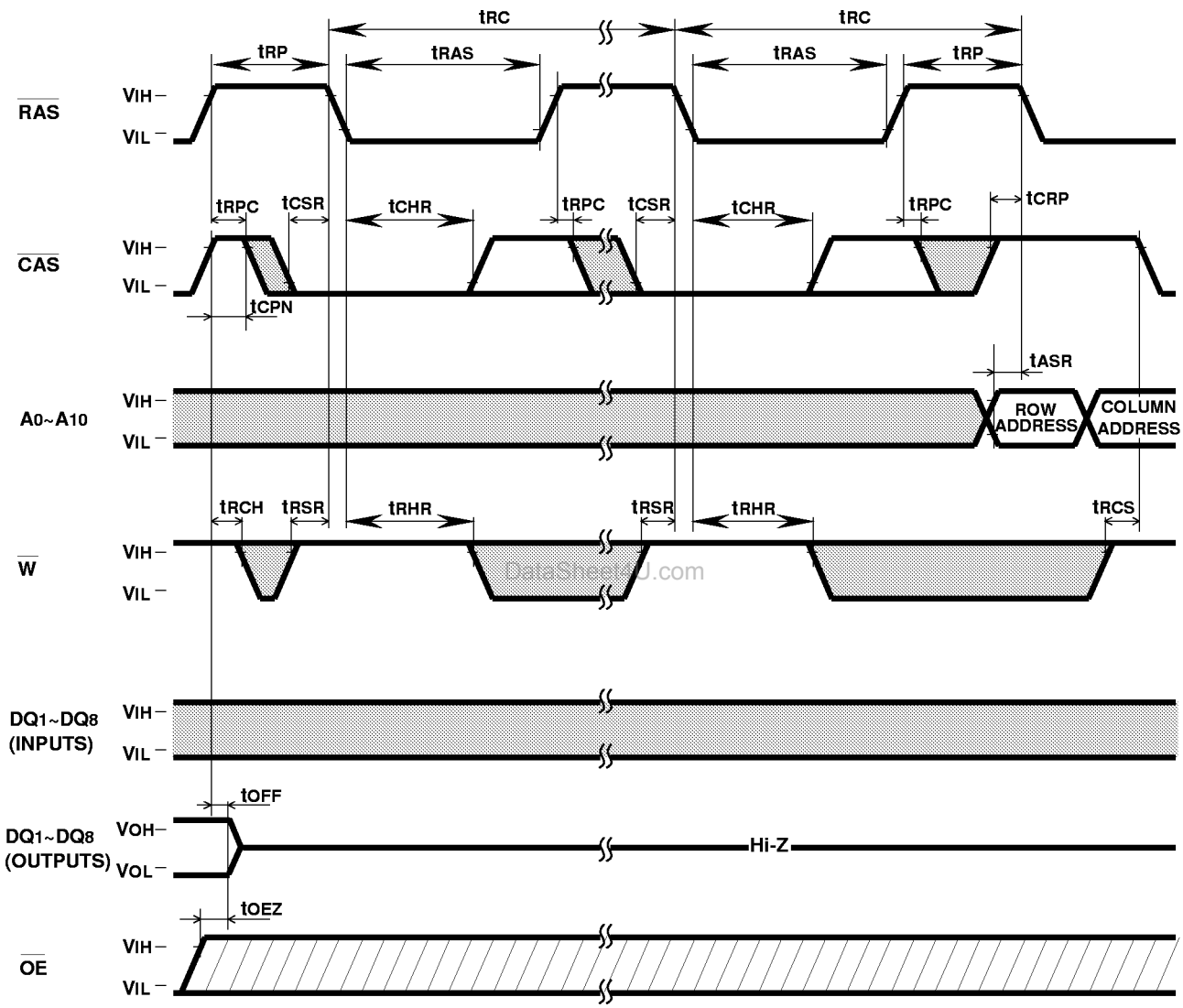
Read-Write, Read-Modify-Write Cycle



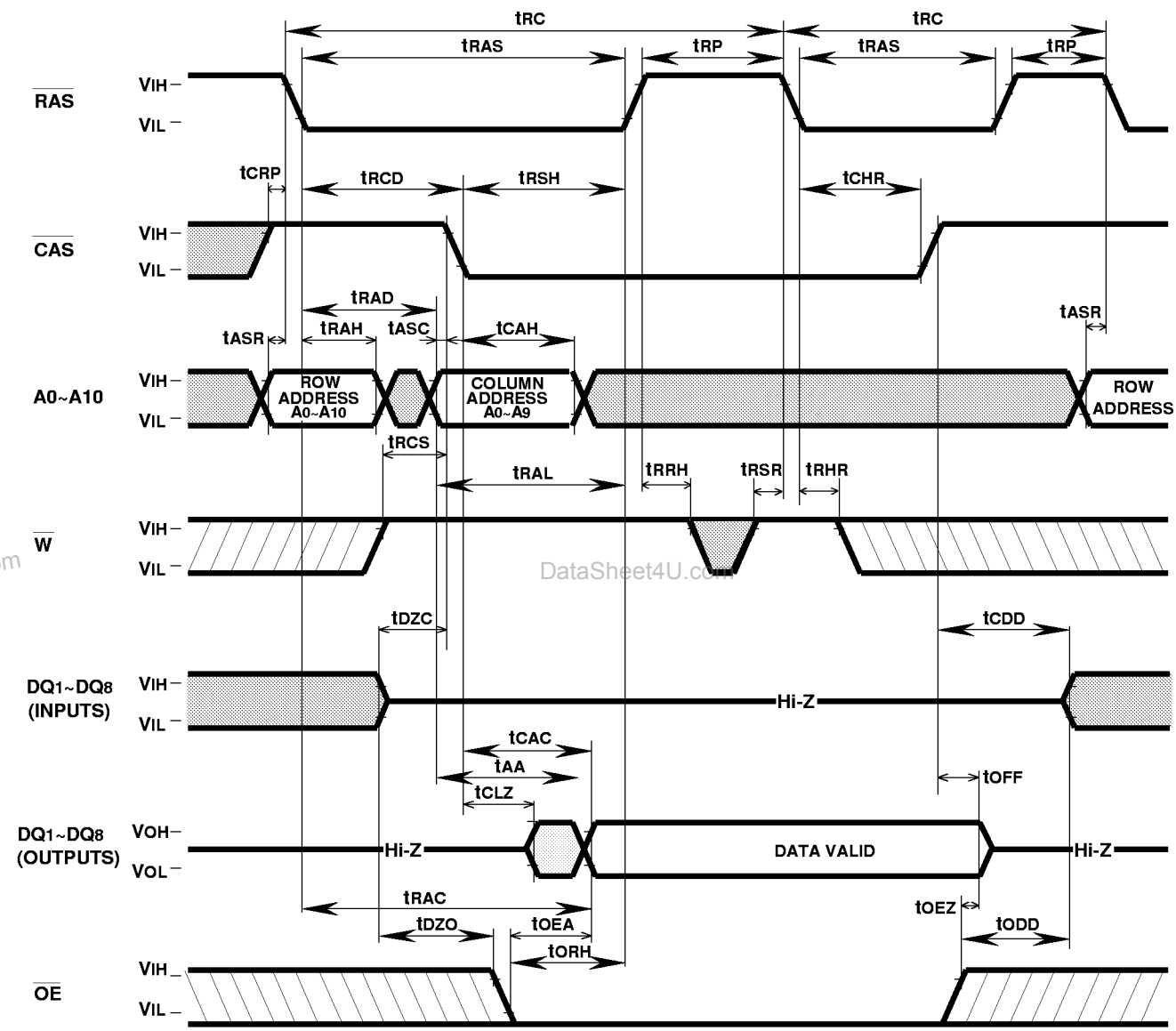
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle , Slow Refresh Cycle

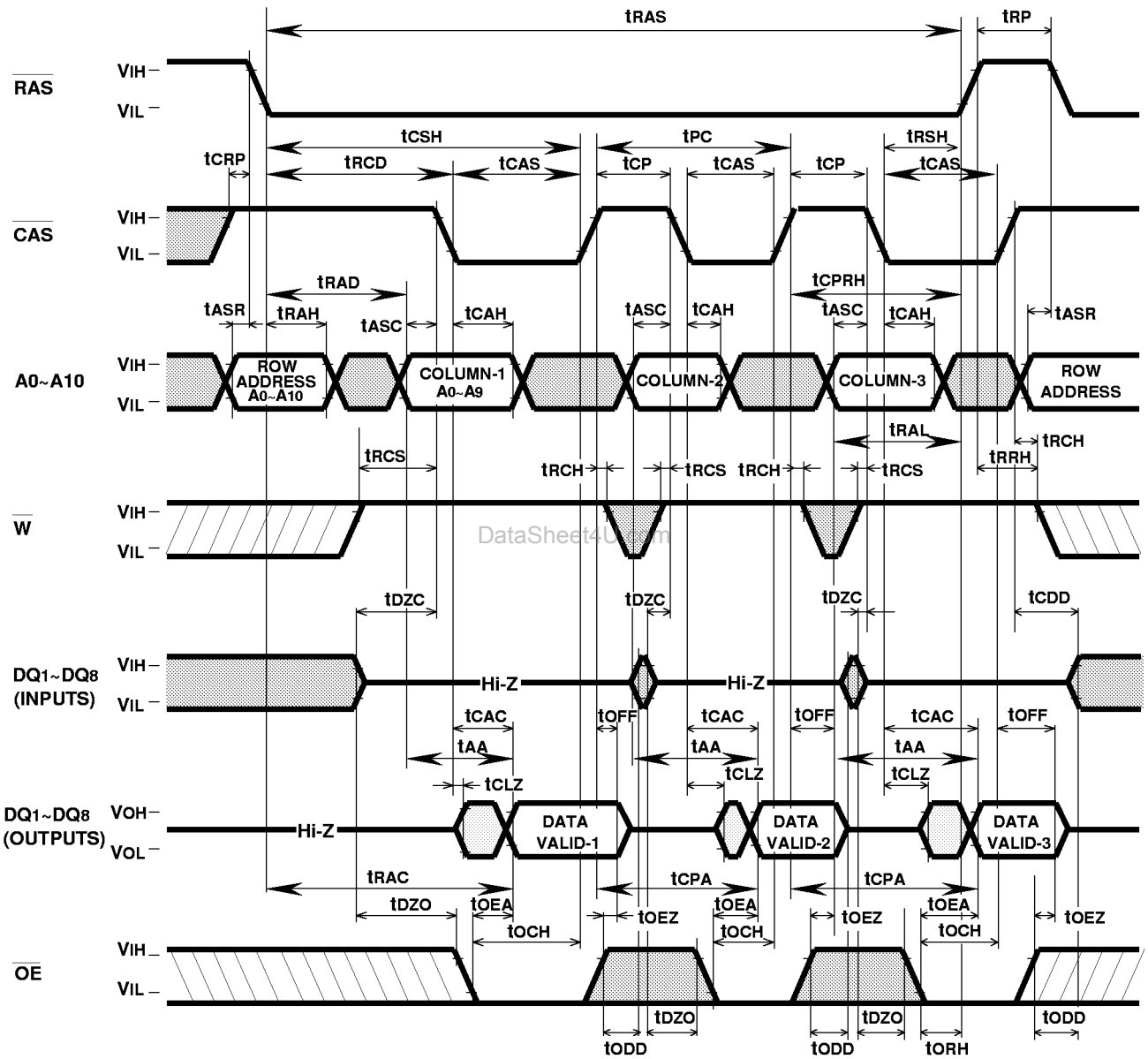


Hidden Refresh Cycle (Read) (Note 29)

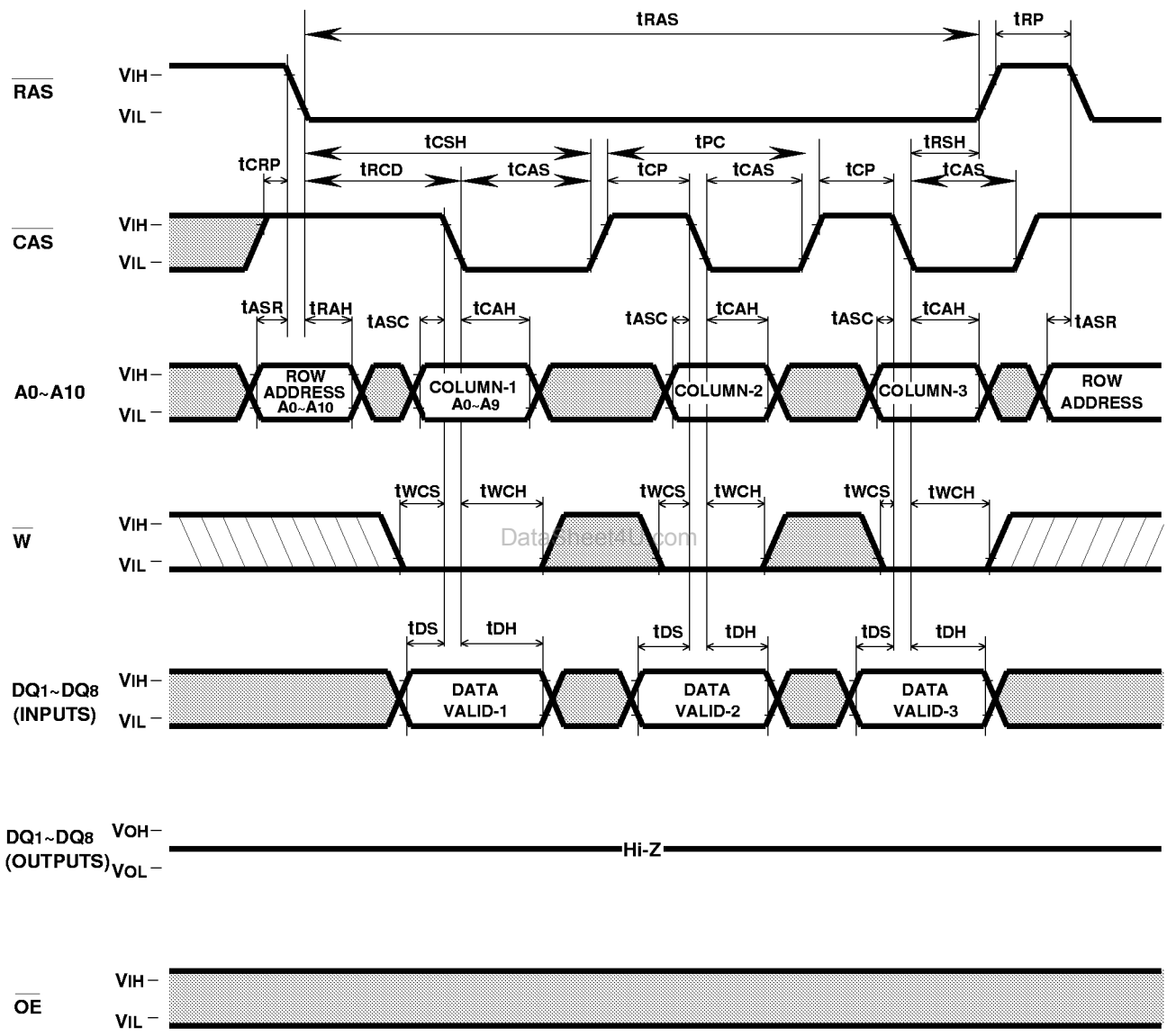


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above. And in any cycle, tRSR&tRHR should be satisfied not to enter TEST MODE .

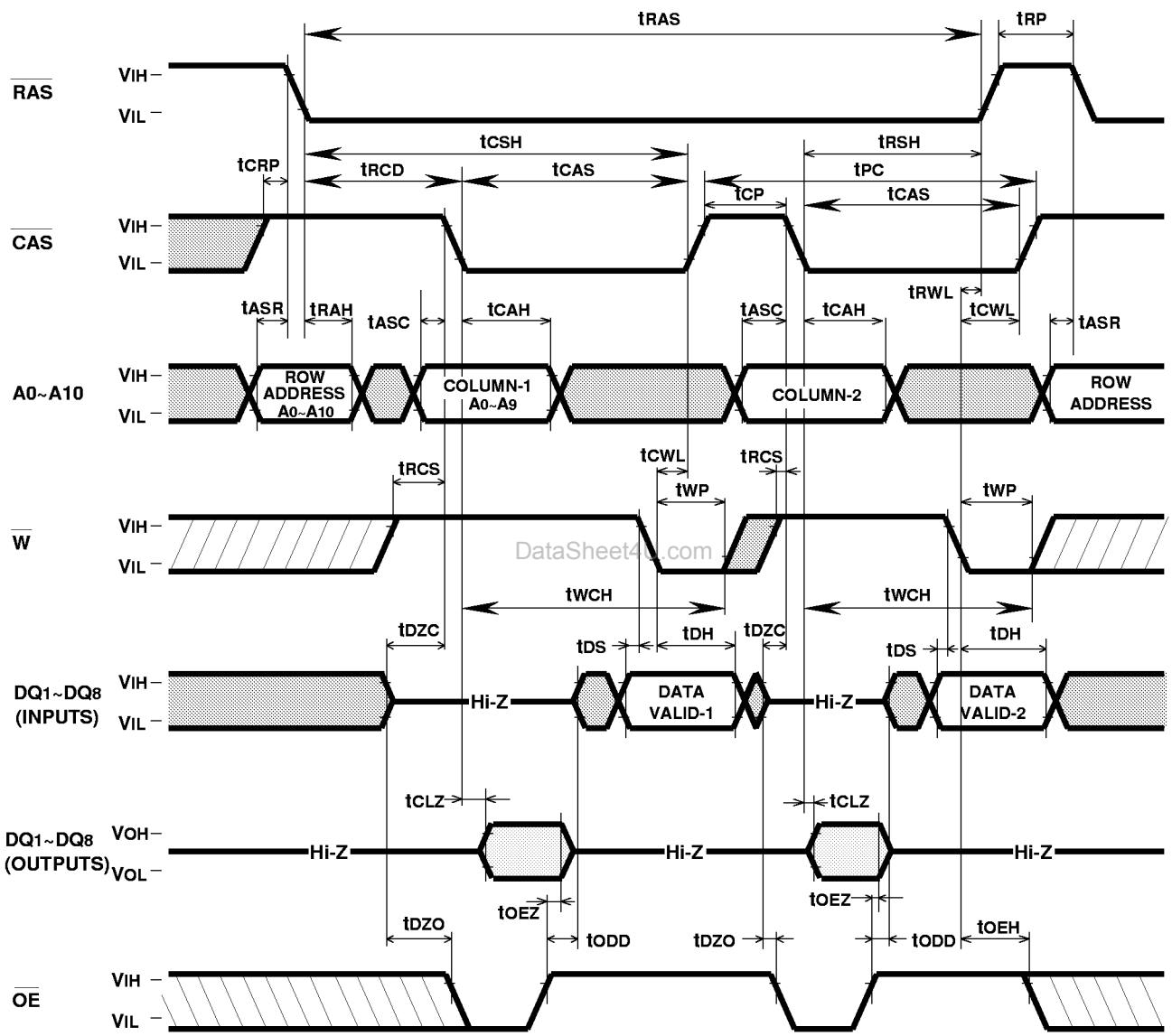
Fast Page Mode Read Cycle



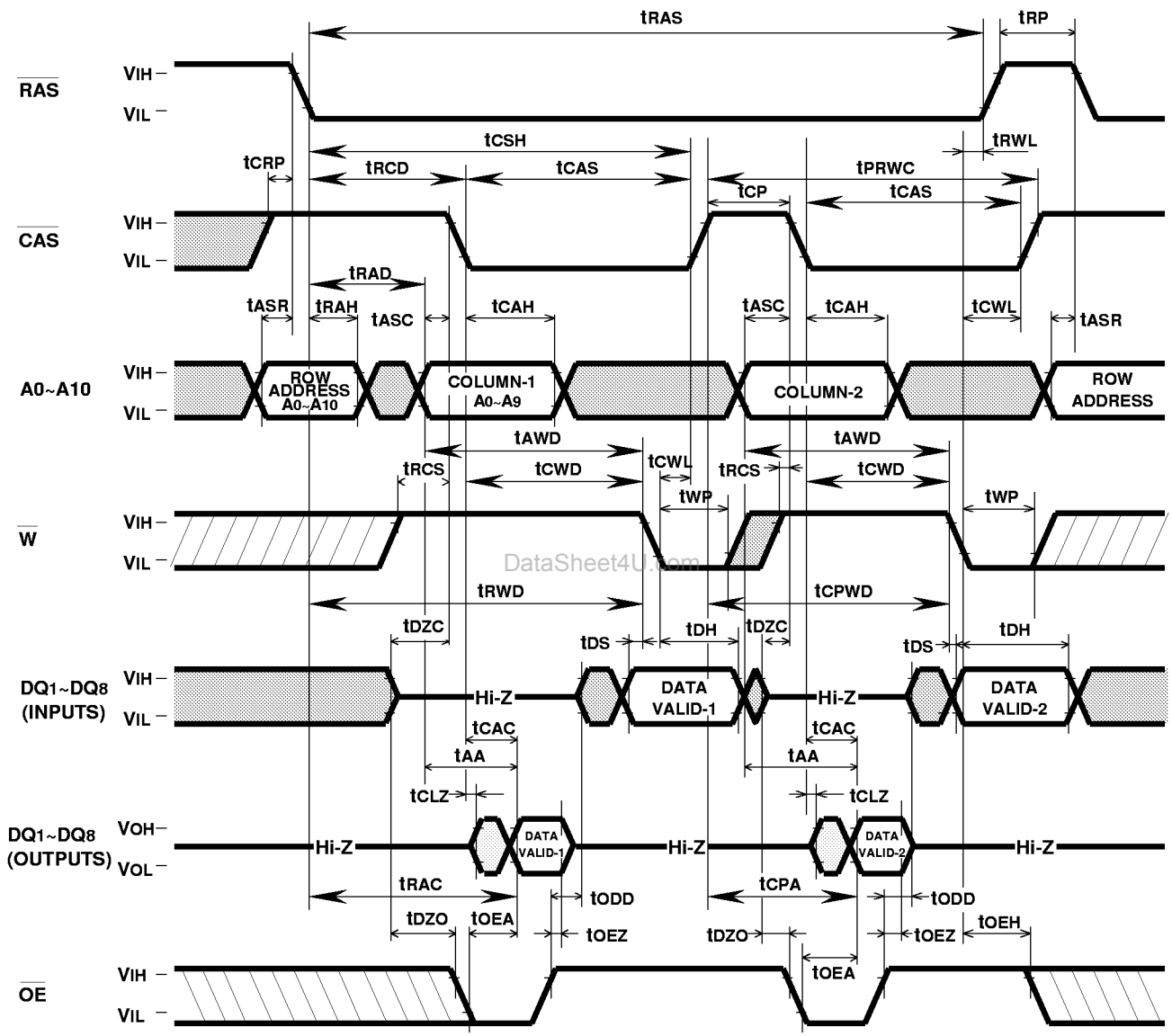
Fast Page Mode Write Cycle (Early Write)



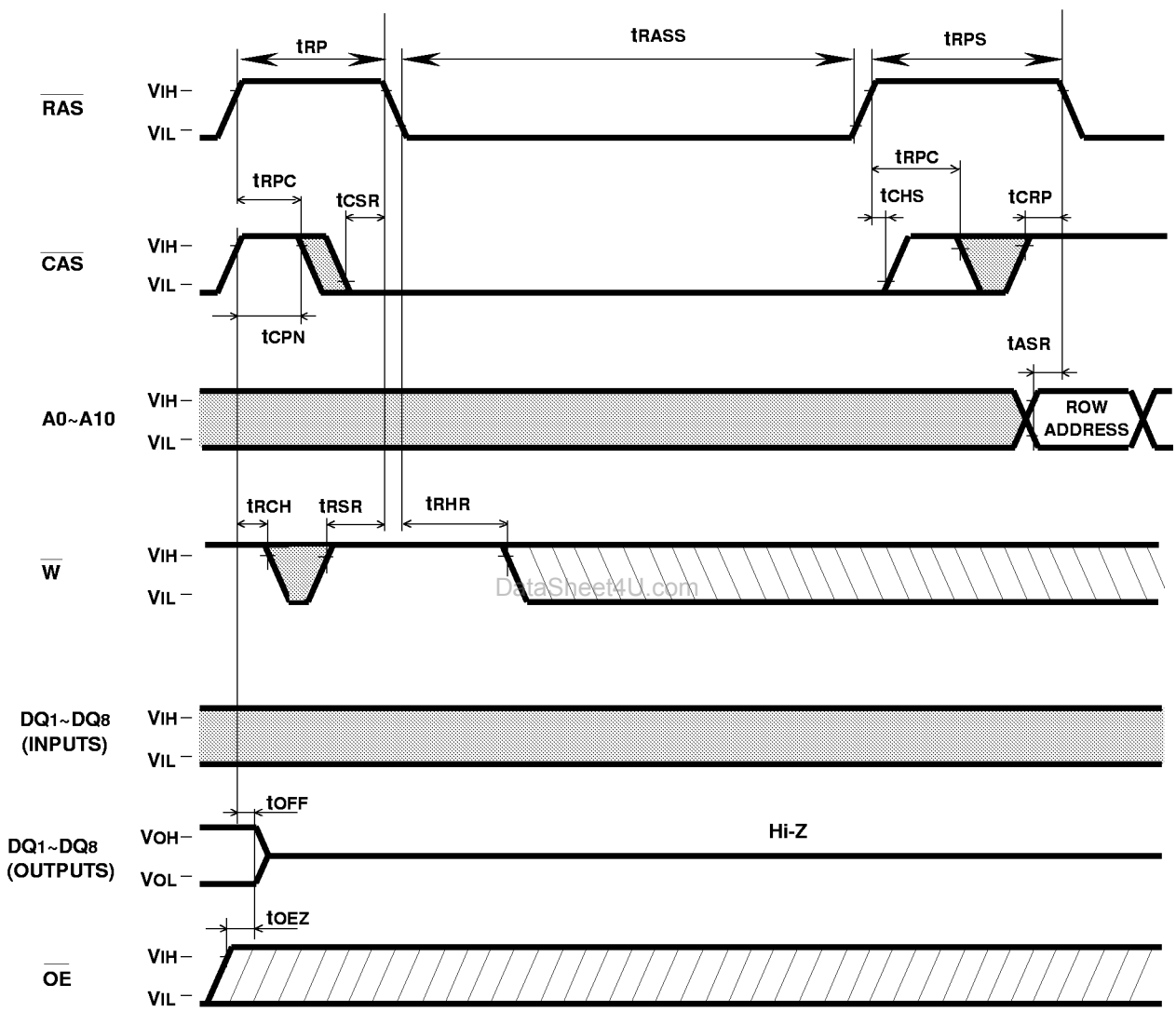
Fast-Page Mode Write Cycle (Delayed Write)



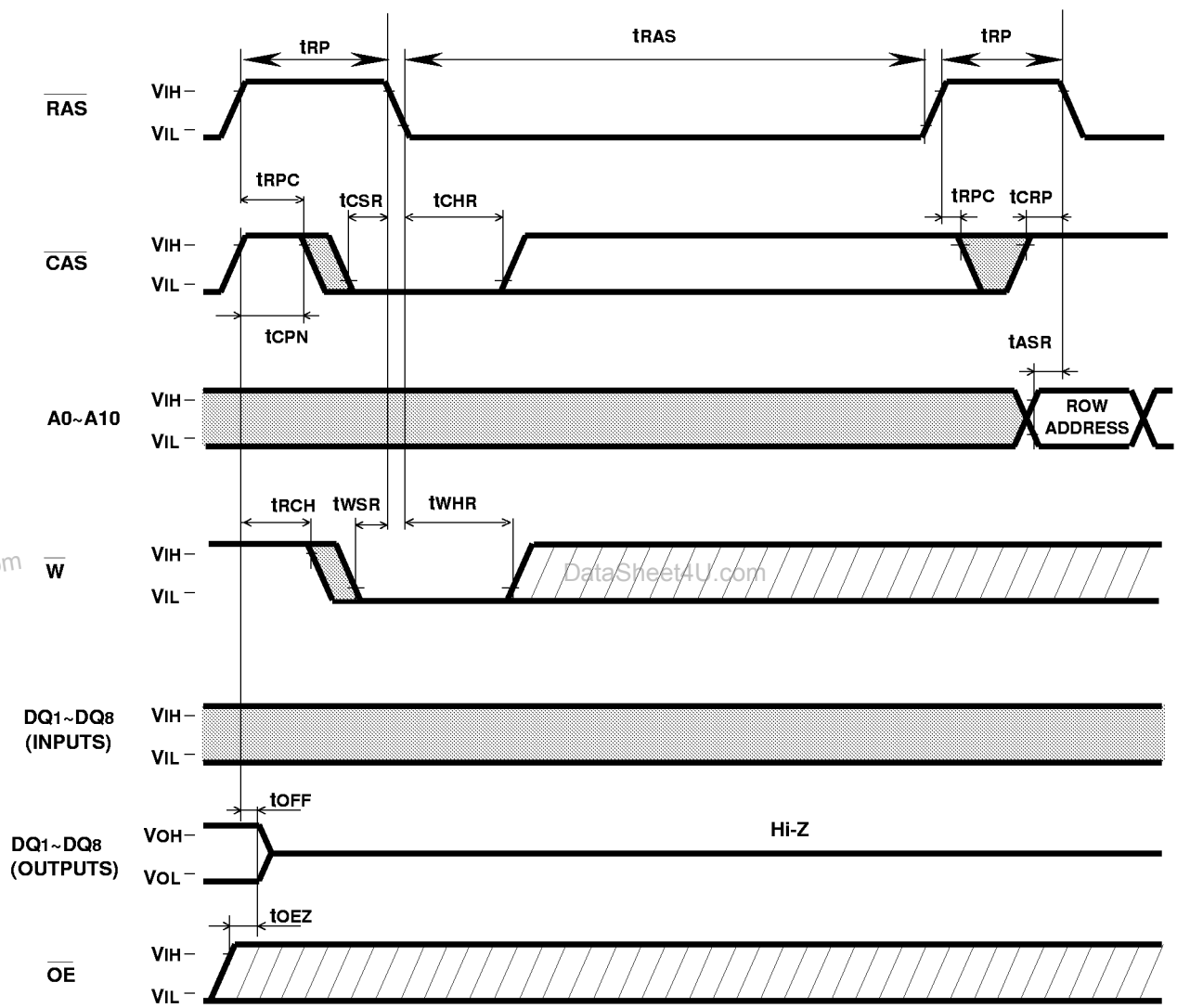
Fast Page Mode Read-Write,Read-Modify-Write Cycle



Self Refresh Cycle



TEST Mode SET Cycle (Note 27)



Note 27 : This cycle can be used for initialized cycle after power-up , however entried into Test Mode.