ADVANCE INFORMATION

T-46-13-26

28F400BX-T/B, 28F004BX-T/B
4 MBIT (256K x16, 512K x8) BOOT BLOCK FLASH MEMORY FAMILY

- x8/x16 Input/Output Architecture
  - 28F400BX-T, 28F400BX-B
  - For High Performance and High Integration 16-bit and 32-bit CPUs
- x8-only Input/Output Architecture
  - 28F004BX-T, 28F004BX-B
  - For Space Constrained 8-bit Applications
- Optimized High Density Blocked Architecture
  - One 16 KB Protected Boot Block
  - Two 8 KB Parameter Blocks
  - One 96 KB Main Block
  - Three 128 KB Main Blocks
  - Top or Bottom Boot Locations
- Extended Cycling Capability
  - 100,000 Block Erase Cycles
- Automated Word/Byte Write and Block Erase
  - Command User Interface
  - Status Registers
  - Erase Suspend Capability
- SRAM-Compatible Write Interface
- Automatic Power Savings Feature
  - 1 mA Typical I_{CC} Active Current in Static Operation
- Very High-Performance Read
  - 60/80 ns Maximum Access Time
  - 30/40 ns Maximum Output Enable Time
- Low Power Consumption
  - 20 mA Typical x8 Active Read Current
  - 25 mA Typical x16 Active Read Current
- Deep Power-Down/Reset Input
  - 0.2 μA I_{CC} Typical
  - Acts as Reset for Boot Operations
- Extended Temperature Operation
  - $-40°C$ to $+85°C$
- Write Protection for Boot Block
- Hardware Data Protection Feature
  - Erase/Write Lockout During Power Transitions
- Industry Standard Surface Mount Packaging
  - 28F400BX: JEDEC ROM Compatible
    - 44-Lead PSOP
    - 56-Lead TSOP
  - 28F004BX: 40-Lead TSOP
- 12V Word/Byte Write and Block Erase
  - V_{PP} = 12V $\pm$5% Standard
  - V_{PP} = 12V $\pm$10% Option
- ETOX™ III Flash Technology
  - 5V Read

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November 1992
Order Number: 290451-002

Intel's 4 Mbit Flash Memory Family is an extension of the Boot Block Architecture which includes block-selective erasure, automated write and erase operations and standard microprocessor interface. The 4 Mbit Flash Memory Family enhances the Boot Block Architecture by adding more density and blocks, x8/x16 input/output control, very high speed, low power, an industry standard ROM compatible pinout and surface mount packaging. The 4 Mbit flash family is an easy upgrade from Intel's 2 Mbit Boot Block Flash Memory Family.

The Intel 28F400BX-T/B are 16-bit wide flash memory offerings. These high density flash memories provide user selectable bus operation for either 8-bit or 16-bit applications. The 28F400BX-T and 28F400BX-B are 4,194,304-bit non-volatile memories organized as either 524,288 bytes or 262,144 words of information. They are offered in 44-Lead plastic SOP and 56-Lead TSOP packages. The x8/x16 pinout conforms to the industry standard ROM/EPROM pinout.

The Intel 28F004BX-T/B are 8-bit wide flash memories with 4,194,304 bits organized as 524,288 bytes of information. They are offered in a 40-Lead TSOP package, which is ideal for space-constrained portable systems.

These devices use an integrated Command User Interface (CUI) and Write State Machine (WSM) for simplified word/byte write and block erasure. The 28F400BX-T/28F004BX-T provide block locations compatible with Intel's MCS-186 family, 80286, i386™, i486™, i860™ and 80960CA microprocessors. The 28F400BX-B/28F004BX-B provide compatibility with Intel's 80960KX and 80960SX families as well as other embedded microprocessors.

The boot block includes a data protection feature to protect the boot code in critical applications. With a maximum access time of 60 ns, these 4 Mbit flash devices are very high performance memories which interface at zero-wait-state to a wide range of microprocessors and microcontrollers. A deep power-down mode lowers the total V_{CC} power consumption to 1 μW. This is critical in handheld battery powered systems. For very low power applications using a 3.3V supply, refer to the Intel 28F400BX-T/B, 28F004BX-T/B 4 Mbit Boot Block Flash Memory Family datasheet.

Manufactured on Intel's 0.8 micron ETOX™ III process, the 4 Mbit flash memory family provides world class quality, reliability and cost-effectiveness at the 4 Mbit density level.

1.0 PRODUCT FAMILY OVERVIEW

Throughout this datasheet the 28F400BX refers to both the 28F400BX-T and 28F400BX-B devices and 28F004BX refers to both the 28F004BX-T and 28F004BX-B devices. The 4 Mbit flash memory family refers to both the 28F400BX and 28F004BX products. This datasheet comprises the specifications for four separate products in the 4 Mbit flash memory family. Section 1 provides an overview of the 4 Mbit flash memory family including applications, pinouts and pin descriptions. Sections 2 and 3 describe in detail the specific memory organizations for the 28F400BX and 28F004BX products respectively. Section 4 combines a description of the family's principles of operations. Finally Section 5 describes the family's operating specifications.

Product Family

X8/X16 Products	X8-Only Products
28F400BX-T	28F004BX-T
28F400BX-B	28F004BX-B

1.1 Main Features

The 28F400BX/28F004BX boot block flash memory family is a very high performance 4 Mbit (4,194,304 bit) memory family organized as either 256 KWords (262,144 words) of 16 bits each or 512 KBytes (524,288 bytes) of 8 bits each.

Seven Separately Erasable Blocks including a **Hardware-Lockable boot block** (16,384 Bytes), **Two parameter blocks** (8,192 Bytes each) and **Four main blocks** (1 block of 98,304 Bytes and 3 blocks of 131,072 Bytes) are included on the 4 Mbit family. An erase operation erases one of the main blocks in typically 2.4 seconds and the boot or parameter blocks in typically 1.0 seconds independent of the remaining blocks. Each block can be independently erased and programmed 100,000 times.

The Boot Block is located at either the top (28F400BX-T, 28F004BX-T) or the bottom (28F400BX-B, 28F004BX-B) of the address map in order to accommodate different microprocessor protocols for boot code location. The **hardware lockable boot block** provides the most secure code storage. The boot block is intended to store the kernel code required for booting-up a system. When the $\overline{PWD}$ pin is between 11.4V and 12.6V the boot block is unlocked and program and erase operations can be performed. When the $\overline{PWD}$ pin is at or below 6.5V the boot block is locked and program and erase operations to the boot block are ignored.

The 28F400BX products are available in the ROM/EPROM compatible pinout and housed in the 44-Lead PSOP (Plastic Small Outline) package and the 56-Lead TSOP (Thin Small Outline, 1.2mm thick) package as shown in Figures 3 and 4. The 28F004BX products are available in the 40-Lead TSOP (1.2mm thick) package as shown in Figure 5.

The **Command User Interface (CUI)** serves as the interface between the microprocessor or microcontroller and the internal operation of the 28F400BX and 28F004BX flash products.

Program and Erase Automation allows program and erase operations to be executed using a two-write command sequence to the CUI. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations, including verifications, thereby unburdening the microprocessor or microcontroller. Writing of memory data is performed in word or byte increments for the 28F400BX family and in byte increments for the 28F004BX family typically within 9 μs which is a 100% improvement over current flash memory products.

The **Status Register (SR)** indicates the status of the WSM and whether the WSM successfully completed the desired program or erase operation.

Maximum Access Time of **60 ns (TACC)** is achieved over the commercial temperature range (0°C to 70°C), 5% V_{CC} supply voltage range (4.75V to 5.25V) and 30 pF output load. Maximum Access Time of **70 ns (TACC)** is achieved over the commercial temperature range, 10% V_{CC} supply range (4.5V to 5.5V) and 100 pF output load.

I_{PP} maximum Program current is 40 mA for x16 operation and 30 mA for x8 operation. I_{PP} Erase current is 30 mA maximum. V_{PP} erase and programming voltage is 11.4V to 12.6V (V_{PP} = 12V ± 5%) under all operating conditions. As an option, V_{PP} can also vary between 10.8V to 13.2V (V_{PP} = 12V ± 10%) with a guaranteed number of 100 block erase cycles.

Typical I_{CC} Active Current of 25 mA is achieved for the X16 products (28F400BX). **Typical I_{CC} Active Current of 20 mA** is achieved for the X8 products (28F400BX, 28F004BX). Refer to the I_{CC} active current derating curves in this datasheet.

The 4 Mbit boot block flash family is also designed with an Automatic Power Savings (APS) feature to minimize system battery current drain and allows for very low power designs. Once the device is accessed to read array data, APS mode will immediately put the memory in static mode of operation where I_{CC} active current is typically 1 mA until the next read is initiated.

When the $\overline{CE}$ and $\overline{PWD}$ pins are at V_{CC} and the $\overline{BYTE}$ pin (28F400BX-only) is at either V_{CC} or GND the **CMOS Standby** mode is enabled where I_{CC} is typically **50 μA.**

A **Deep Power-Down Mode** is enabled when the $\overline{PWD}$ pin is at ground minimizing power consumption and providing write protection during power-up conditions. **I_{CC} current** during deep power-down mode is **0.20 μA typical**. An initial maximum access time or Reset Time of 300 ns is required from $\overline{PWD}$ switching until outputs are valid. Equivalently, the device has a maximum wake-up time of 215 ns until writes to the Command User Interface are recognized. When $\overline{PWD}$ is at ground the WSM is reset, the Status Register is cleared and the entire device is protected from being written to. This feature prevents data corruption and protects the code stored in the device during system reset. The system Reset pin can be tied to $\overline{PWD}$ to reset the memory to normal read mode upon activation of the Reset pin. With on-chip program/erase automation in the 4 Mbit family and the $\overline{PWD}$ functionality for data protection, when the CPU is reset and even if a program or erase command is issued, the device will not recognize any operation until $\overline{PWD}$ returns to its normal state.

For the 28F400BX, Byte-wide or Word-wide Input/Output Control is possible by controlling the $\overline{BYTE}$ pin. When the $\overline{BYTE}$ pin is at a logic low the device is in the byte-wide mode (x8) and data is read and written through DQ[0:7]. During the byte-wide mode, DQ[8:14] are tri-stated and DQ15/A-1 becomes the lowest order address pin. When the $\overline{BYTE}$ pin is at a logic high the device is in the word-wide mode (x16) and data is read and written through DQ[0:15].

1.2 Applications

The 4 Mbit boot block flash family combines high density, high performance, cost-effective flash memories with blocking and hardware protection capabilities. Its flexibility and versatility will reduce costs throughout the product life cycle. Flash memory is ideal for Just-In-Time production flow, reducing system inventory and costs, and eliminating component handling during the production phase.

During the product life cycle, when code updates or feature enhancements become necessary, flash memory will reduce the update costs by allowing either a user-performed code change via floppy disk or a remote code change via a serial link. The 4 Mbit boot block flash family provides full function, blocked flash memories suitable for a wide range of applications. These applications include **Extended PC BIOS and ROM-able** applications storage, Digital Cellular Phone program and data storage, **Telecommunication** boot/firmware, **Printer** firmware/font storage and various other embedded applications where both program and data storage are required.

Reprogrammable systems such as personal computers, are ideal applications for the 4 Mbit flash products. Portable and handheld personal computer applications are becoming more complex with the addition of power management software to take advantage of the latest microprocessor technology, the availability of ROM-based application software, pen tablet code for electronic hand writing, and diagnostic code. Figure 1 shows an example of a 28F400BX-T application.

This increase in software sophistication augments the probability that a code update will be required after the PC is shipped. The 4 Mbit flash products provide an inexpensive update solution for the notebook and handheld personal computers while extending their product lifetime. Furthermore, the 4 Mbit flash products' power-down mode provides added flexibility for these battery-operated portable designs which require operation at very low power levels.

The 4 Mbit flash products also provide excellent design solutions for Digital Cellular Phone and Telecommunication switching applications requiring high performance, high density storage capability coupled with modular software designs, and a small form factor package (X8-only bus). The 4 Mbit's blocking scheme allows for an easy segmentation of the embedded code with; 16 Kbytes of Hardware-Protected Boot code, 4 Main Blocks of program code and 2 Parameter Blocks of 8 Kbytes each for frequently updatable data storage and diagnostic messages (e.g., phone numbers, authorization codes). Figure 2 is an example of such an application with the 28F004BX-T.

These are a few actual examples of the wide range of applications for the 4 Mbit Boot Block flash memory family which enable system designers achieve the best possible product design. Only your imagination limits the applicability of such a versatile product family.

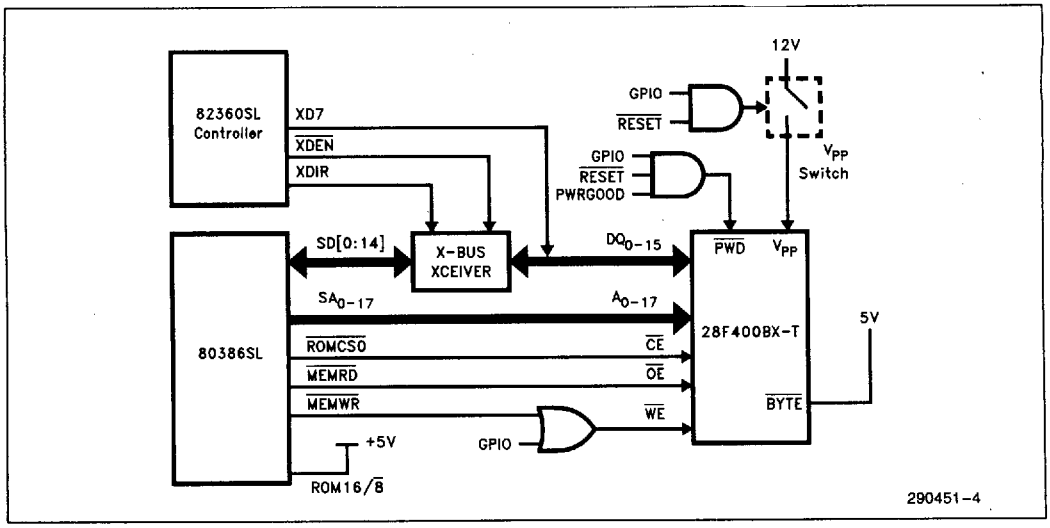

Figure 1. 28F400BX Interface to INTEL386SL™ Microprocessor Superset

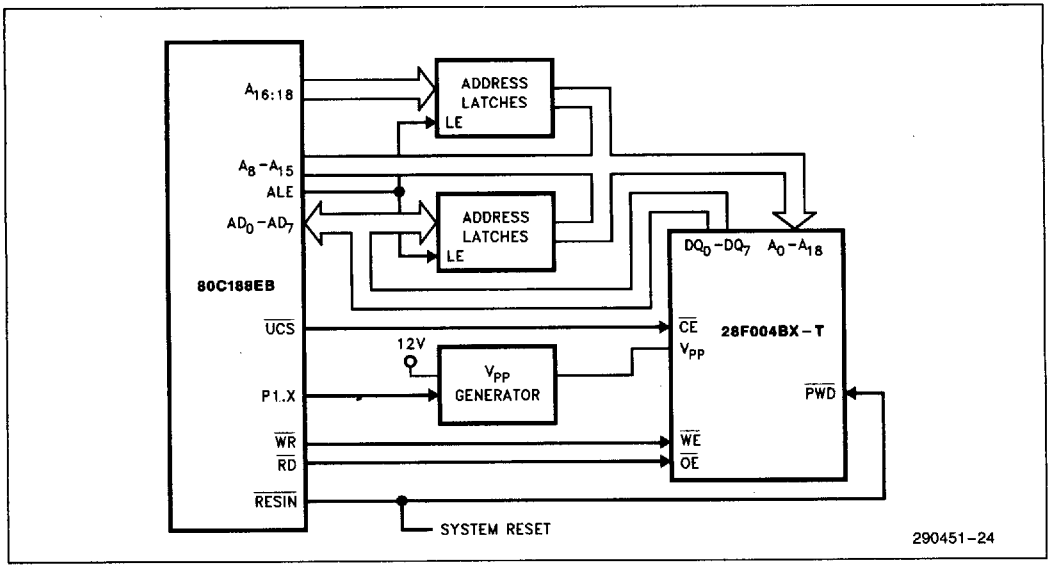

Figure 2. 28F004BX Interface to INTEL 80C188EB 8-Bit Embedded Microprocessor

1.3 Pinouts

The 28F400BX 44-Lead PSOP pinout follows the industry standard ROM/EPROM pinout as shown in Figure 3. Furthermore, the 28F400BX 56-Lead TSOP pinout shown in Figure 4 provides density upgrades to future higher density boot block memories.

The 28F004BX 40-Lead TSOP pinout shown in Figure 5 is 100% compatible and provides a density upgrade for the 2 Mbit Boot Block flash memory or the 28F002BX.

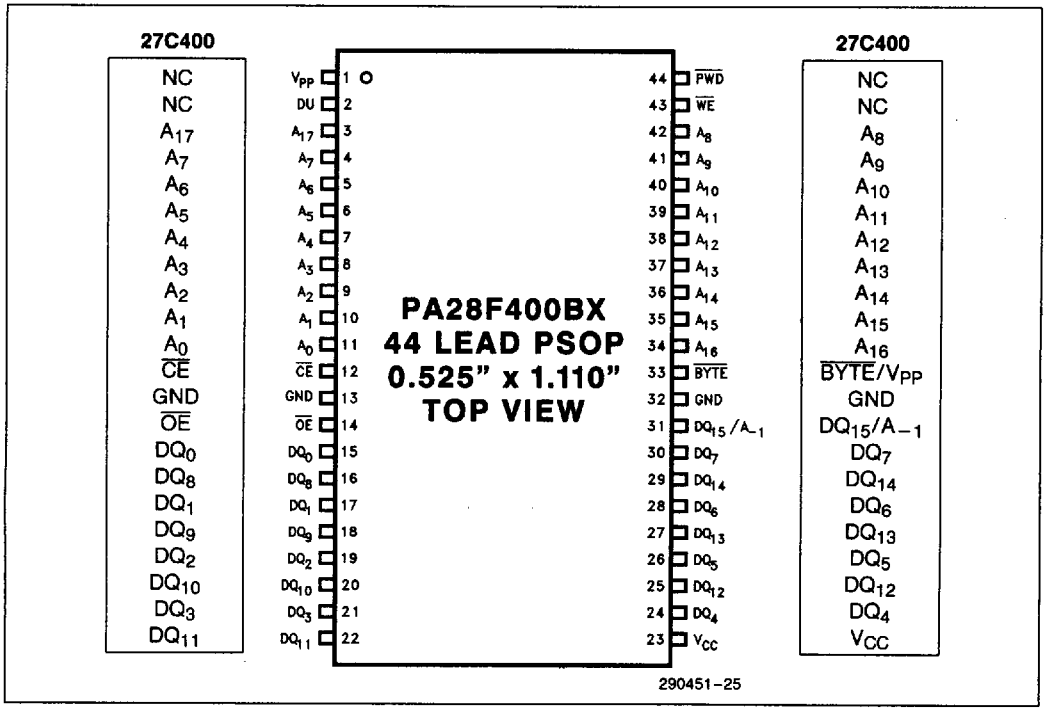

Figure 3. PSOP Lead Configuration for x8/x16 28F400BX

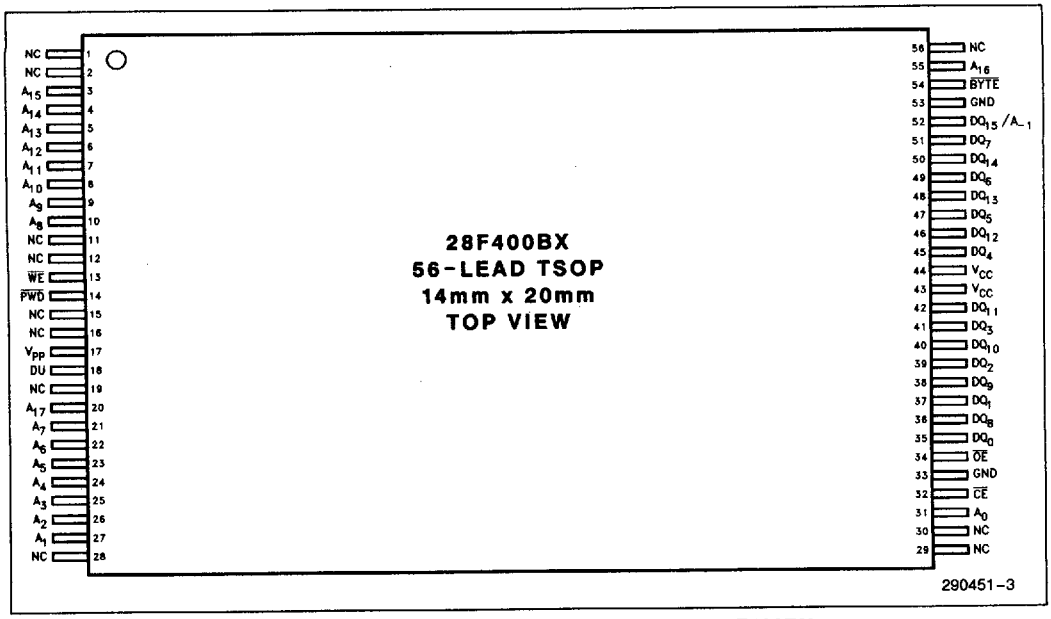

Figure 4. TSOP Lead Configuration for x8/x16 28F400BX

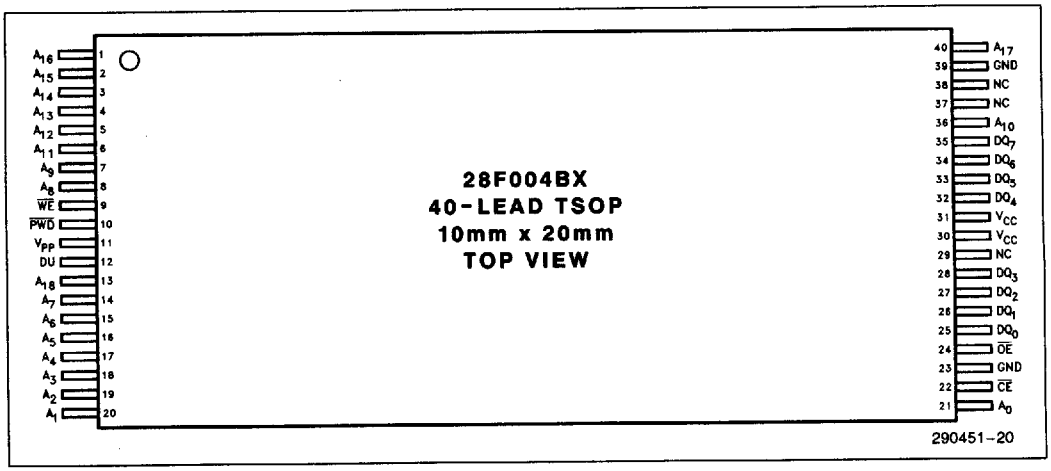

Figure 5. TSOP Lead Configuration for x8 28F004BX

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1.4 28F400BX Pin Descriptions

Symbol	Type	Name and Function
A_0–A_{17}	I	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
A_9	I	**ADDRESS INPUT:** When A_9 is at 12V the signature mode is accessed. During this mode A_0 decodes between the manufacturer and device ID's. When $\overline{BYTE}$ is at a logic low only the lower byte of the signatures are read. DQ_{15}/A_{-1} is a don't care in the signature mode when $\overline{BYTE}$ is low.
DQ_0–DQ_7	I/O	**DATA INPUTS/OUTPUTS:** Inputs array data on the second $\overline{CE}$ and $\overline{WE}$ cycle during a program command. Inputs commands to the command user interface when $\overline{CE}$ and $\overline{WE}$ are active. Data is internally latched during the write and program cycles. Outputs array, intelligent identifier and Status Register data. The data pins float to tri-state when the chip is deselected or the outputs are disabled.
DQ_8–DQ_{15}	I/O	**DATA INPUTS/OUTPUTS:** Inputs array data on the second $\overline{CE}$ and $\overline{WE}$ cycle during a program command. Data is internally latched during the write and program cycles. Outputs array data. The data pins float to tri-state when the chip is deselected or the outputs are disabled as in the byte-wide mode ($\overline{BYTE}$ = "0"). In the byte-wide mode DQ_{15}/A_{-1} becomes the lowest order address for data output on DQ_0-DQ_7.
$\overline{CE}$	I	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels. If $\overline{CE}$ and $\overline{PWD}$ are high, but not at a CMOS high level, the standby current will increase due to current flow through the $\overline{CE}$ and $\overline{PWD}$ input stages.
$\overline{PWD}$	I	**POWER-DOWN:** Provides three-state control. Puts the device in deep power-down mode. Locks the boot block from program/erase. When $\overline{PWD}$ is at logic high level and equals 6.5V maximum the boot block is locked and cannot be programmed or erased. When $\overline{PWD}$ = 11.4V minimum the boot block is unlocked and can be programmed or erased. When $\overline{PWD}$ is at a logic low level the boot block is locked, the deep power-down mode is enabled and the WSM is reset preventing any blocks from being programmed or erased, therefore providing data protection during power transitions. $\overline{PWD}$ terminates any internally timed erase or program activities when it is taken to a logic low. PSD activates the $\overline{CE}$ input stage and requires 300 ns recovery time to transition from deep powerdown to valid data on the outputs or 215 ns delay before the device can recognize valid inputs.
$\overline{OE}$	I	**OUTPUT ENABLE:** Gates the device's outputs through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	I	**WRITE ENABLE:** Controls writes to the Command Register and array blocks. $\overline{WE}$ is active low. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{BYTE}$	I	**$\overline{BYTE}$ ENABLE:** Controls whether the device operates in the byte-wide mode (x8) or the word-wide mode (x16). $\overline{BYTE}$ pin must be controlled at CMOS levels to meet 100A CMOS current in the standby mode. $\overline{BYTE}$ = "0" enables the byte-wide mode, where data is read and programmed on DQ_0–DQ_7 and DQ_{15}/A_{-1} becomes the lowest order address that decodes between the upper and lower byte. DQ_8–DQ_{14} are tri-stated during the byte-wide mode. $\overline{BYTE}$ = "1" enables the word-wide mode where data is read and programmed on DQ_0–DQ_{15}.
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** For erasing memory array blocks or programming data in each block. **Note:** $V_{PP} < V_{PPLMAX}$ memory contents cannot be altered.
V_{CC}		**DEVICE POWER SUPPLY (5V ±10%, 5V ±5%)**
GND		**GROUND:** For all internal circuitry.
NC		**NO CONNECT:** Pin may be driven or left floating.
DU		**DON'T USE PIN:** Pin should not be connected to anything.

1.5 28F004BX Pin Descriptions

Symbol	Type	Name and Function
A_0–A_{18}	I	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
A_9	I	**ADDRESS INPUT:** When A_9 is at 12V the signature mode is accessed. During this mode A_0 decodes between the manufacturer and device ID's.
DQ_0–DQ_7	I/O	**DATA INPUTS/OUTPUTS:** Inputs array data on the second $\overline{CE}$ and $\overline{WE}$ cycle during a program command. Inputs commands to the command user interface when $\overline{CE}$ and $\overline{WE}$ are active. Data is internally latched during the write and program cycles. Outputs array, intelligent identifier and status register data. The data pins float to tri-state when the chip is deselected or the outputs are disabled.
$\overline{CE}$	I	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels. If $\overline{CE}$ and $\overline{PWD}$ are high, but not at a CMOS high level, the standby current will increase due to current flow through the $\overline{CE}$ and $\overline{PWD}$ input stages.
$\overline{PWD}$	I	**POWERDOWN:** Provides Three-State control. Puts the device in deep power-down mode. Locks the Boot Block from program/erase. When $\overline{PWD}$ is at logic high level and equals 6.5V maximum the Boot Block is locked and cannot be programmed or erased. When $\overline{PWD}$ = 11.4V minimum the Boot Block is unlocked and can be programmed or erased. When $\overline{PWD}$ is at a logic low level the Boot Block is locked, the deep power-down mode is enabled and the WSM is reset preventing any blocks from being programmed or erased, therefore providing data protection during power transitions. $\overline{PWD}$ terminates any internally timed erase or program activities when it is taken to a logic low. $\overline{PWD}$ activates the $\overline{CE}$ input stage and requires 300 ns recovery time to transition from deep power-down to valid data on the outputs or 215 ns delay before the device can recognize valid inputs.
$\overline{OE}$	I	**OUTPUT ENABLE:** Gates the device's outputs through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	I	**WRITE ENABLE:** Controls writes to the Command Register and array blocks. $\overline{WE}$ is active low. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse.
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** For erasing memory array blocks or programming data in each block. **NOTE:** $V_{PP} < V_{PPLMAX}$ memory contents cannot be altered.
V_{CC}		**DEVICE POWER SUPPLY (5V ±10%, 5V ±5%)**
GND		**GROUND:** For all internal circuitry.
NC		**NO CONNECT:** Pin may be driven or left floating.
DU		**DON'T USE PIN:** Pin should not be connected to anything.

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2.0 28F400BX WORD/BYTE-WIDE PRODUCTS DESCRIPTION

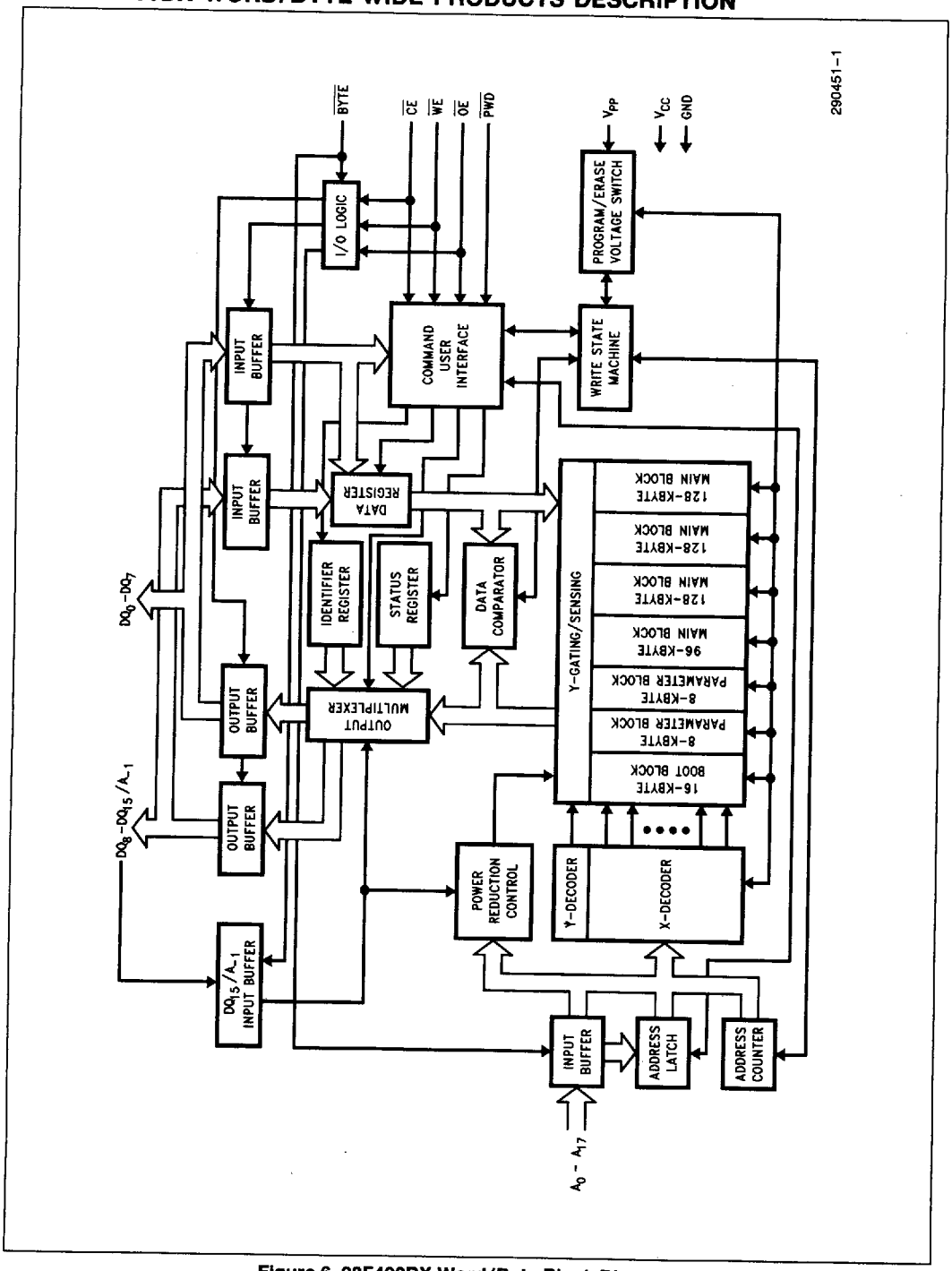

Figure 6. 28F400BX Word/Byte Block Diagram

2.1 28F400BX Memory Organization

2.1.1 BLOCKING

The 28F400BX uses a blocked array architecture to provide independent erasure of memory blocks. A block is erased independently of other blocks in the array when an address is given within the block address range and the Erase Setup and Erase Confirm commands are written to the CUI. The 28F400BX is a random read/write memory, only erasure is performed by block.

2.1.1.1 Boot Block Operation and Data Protection

The 16 Kbyte boot block provides a lock feature for secure code storage. The intent of the boot block is to provide a secure storage area for the kernel code that is required to boot a system in the event of power failure or other disruption during code update. This lock feature ensures absolute data integrity by preventing the boot block from being written or erased when $\overline{PWD}$ is not at 12V. The boot block can be erased and written when $\overline{PWD}$ is held at 12V for the duration of the erase or program operation. This allows customers to change the boot code when necessary while providing security when needed. See the Block Memory Map section for address locations of the boot block for the 28F400BX-T and 28F400BX-B.

2.1.1.2 Parameter Block Operation

The 28F400BX has 2 parameter blocks (8 Kbytes each). The parameter blocks are intended to provide storage for frequently updated system parameters and configuration or diagnostic information. The parameter blocks can also be used to store additional boot or main code. The parameter blocks however, do not have the hardware write protection feature that the boot block has. The parameter blocks provide for more efficient memory utilization when dealing with parameter changes versus regularly blocked devices. See the Block Memory Map section for address locations of the parameter blocks for the 28F400BX-T and 28F400BX-B.

2.1.1.3 Main Block Operation

Four main blocks of memory exist on the 28F400BX (3 x 128 Kbyte blocks and 1 x 96 Kbyte blocks). See the following section on Block Memory Map for the address location of these blocks for the 28F400BX-T and 28F400BX-B products.

2.1.2 BLOCK MEMORY MAP

Two versions of the 28F400BX product exist to support two different memory maps of the array blocks in order to accommodate different microprocessor protocols for boot code location. The 28F400BX-T memory map is inverted from the 28F400BX-B memory map.

2.1.2.1. 28F400BX-B Memory Map

The 28F400BX-B device has the 16 Kbyte boot block located from 00000H to 01FFFH to accommodate those microprocessors that boot from the bottom of the address map at 00000H. In the 28F400BX-B the first 8 Kbyte parameter block resides in memory space from 02000H to 02FFFH. The second 8 Kbyte parameter block resides in memory space from 03000H to 03FFFH. The 96 Kbyte main block resides in memory space from 04000H to 0FFFFH. The three 128 Kbyte main block resides in memory space from 10000H to 1FFFFH, 20000H to 2FFFFH and 30000H to 3FFFFH (word locations). See Figure 7.

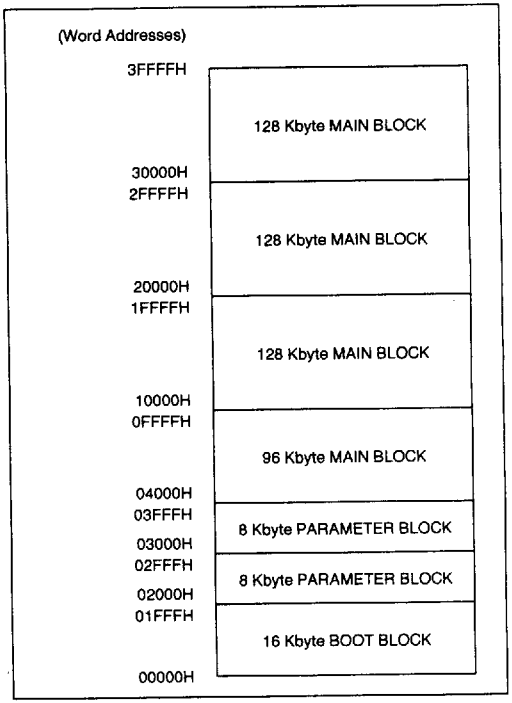

Figure 7. 28F400BX-B Memory Map

2.1.2.2 28F400BX-T Memory Map

The 28F400BX-T device has the 16 Kbyte boot block located from 3E000H to 3FFFFH to accommodate those microprocessors that boot from the top of the address map. In the 28F400BX-T the first 8 Kbyte parameter block resides in memory space from 3D000H to 3DFFFH. The second 8 Kbyte parameter block resides in memory space from 3C000H to 3CFFFH. The 96 Kbyte main block resides in memory space from 30000H to 3BFFFH. The three 128 Kbyte main blocks reside in memory space from 20000H to 2FFFFH, 10000H to 1FFFFH and 00000H to 0FFFFH as shown below in Figure 8.

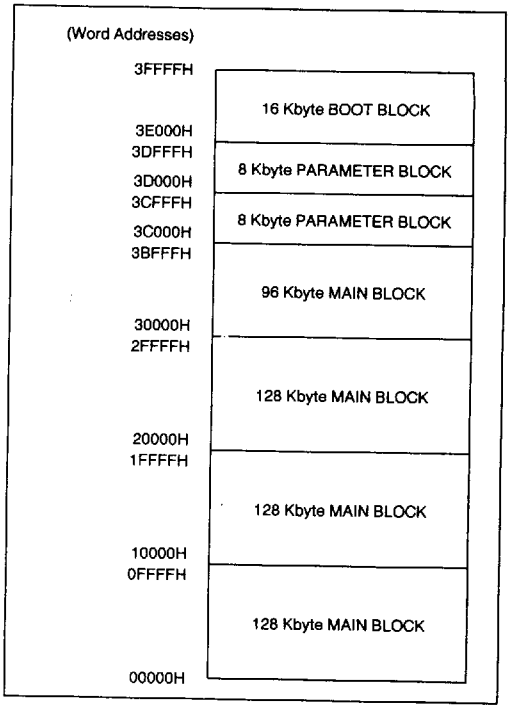

Figure 8. 28F400BX-T Memory Map

3.0 28F004BX PRODUCT DESCRIPTION

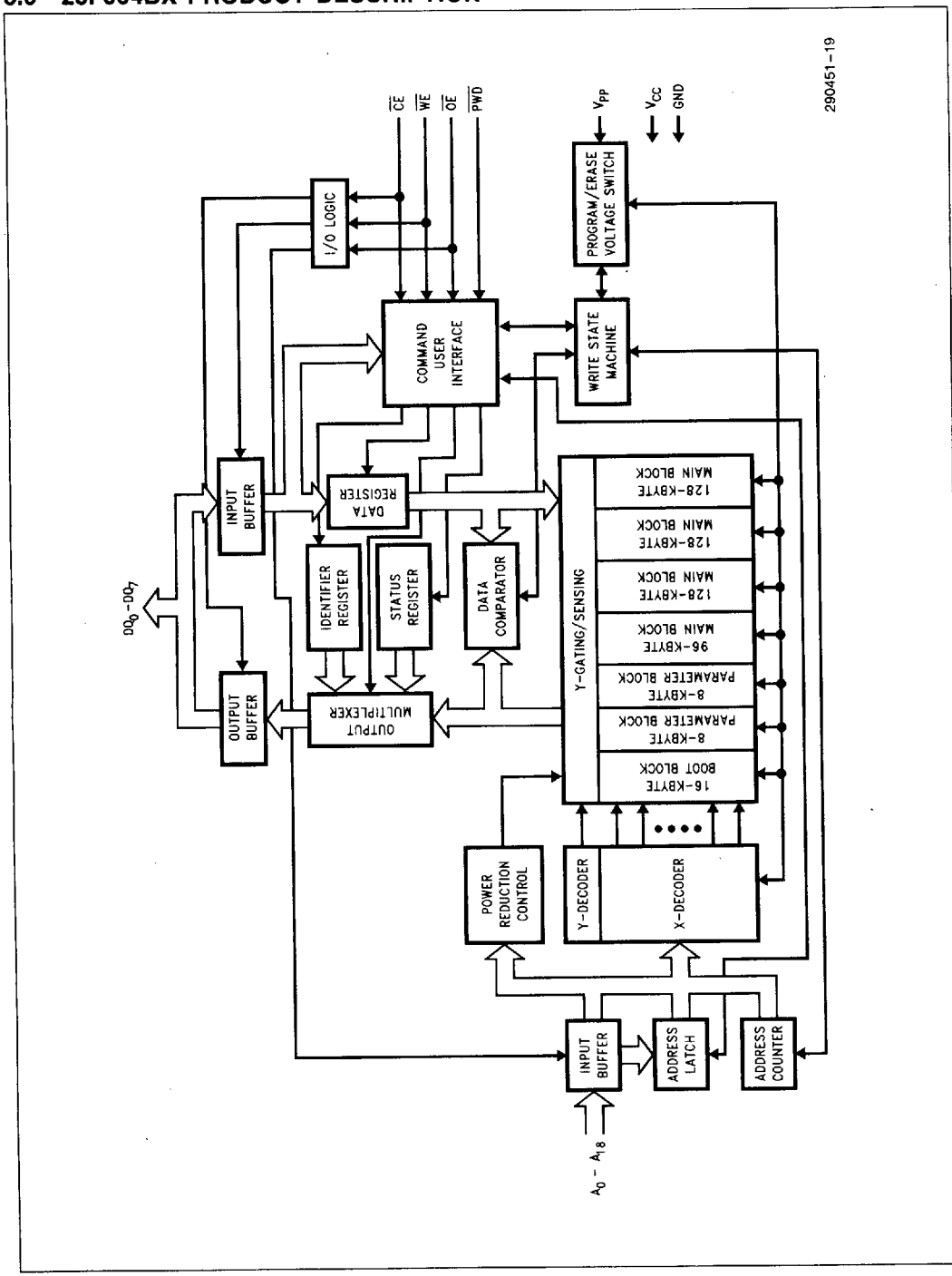

Figure 9. 28F004BX Byte-Wide Block Diagram

3.1 28F004BX Memory Organization

3.1.1 BLOCKING

The 28F004BX uses a blocked array architecture to provide independent erasure of memory blocks. A block is erased independently of other blocks in the array when an address is given within the block address range and the Erase Setup and Erase Confirm commands are written to the CUI. The 28F004BX is a random read/write memory, only erasure is performed by block.

3.1.1.1 Boot Block Operation and Data Protection

The 16 Kbyte boot block provides a lock feature for secure code storage. The intent of the boot block is to provide a secure storage area for the kernel code that is required to boot a system in the event of power failure or other disruption during code update. This lock feature ensures absolute data integrity by preventing the boot block from being programmed or erased when $\overline{PWD}$ is not at 12V. The boot block can be erased and programmed when $\overline{PWD}$ is held at 12V for the duration of the erase or program operation. This allows customers to change the boot code when necessary while still providing security when needed. See the Block Memory Map section for address locations of the boot block for the 28F004BX-T and 28F004BX-B.

3.1.1.2 Parameter Block Operation

The 28F004BX has 2 parameter blocks (8 KBytes each). The parameter blocks are intended to provide storage for frequently updated system parameters and configuration or diagnostic information. The parameter blocks can also be used to store additional boot or main code. The parameter blocks however, do not have the hardware write protection feature that the boot block has. Parameter blocks provide for more efficient memory utilization when dealing with small parameter changes versus regularly blocked devices. See the Block Memory Map section for address locations of the parameter blocks for the 28F004BX-T and 28F004BX-B.

3.1.1.3 Main Block Operation

Four main blocks of memory exist on the 28F004BX (3 × 128 KByte blocks and 1 × 96 KByte blocks). See the following section on Block Memory Map for the address location of these blocks for the 28F004BX-T and 28F004BX-B.

3.1.2 BLOCK MEMORY MAP

Two versions of the 28F004BX product exist to support two different memory maps of the array blocks in order to accommodate different microprocessor protocols for boot code location. The 28F004BX-T memory map is inverted from the 28F004BX-B memory map.

3.1.2.1 28F004BX-B Memory Map

The 28F004BX-B device has the 16 Kbyte boot block located from 00000H to 03FFFH to accommodate those microprocessors that boot from the bottom of the address map at 00000H. In the 28F004BX-B the first 8 Kbyte parameter block resides in memory from 04000H to 05FFFH. The second 8 Kbyte parameter block resides in memory space from 06000H to 07FFFH. The 96 Kbyte main block resides in memory space from 08000H to 1FFFFH. The three 128 Kbyte main block reside in memory space from 20000H to 3FFFFH, 40000H to 5FFFFH and 60000H to 7FFFFH. See Figure 10.

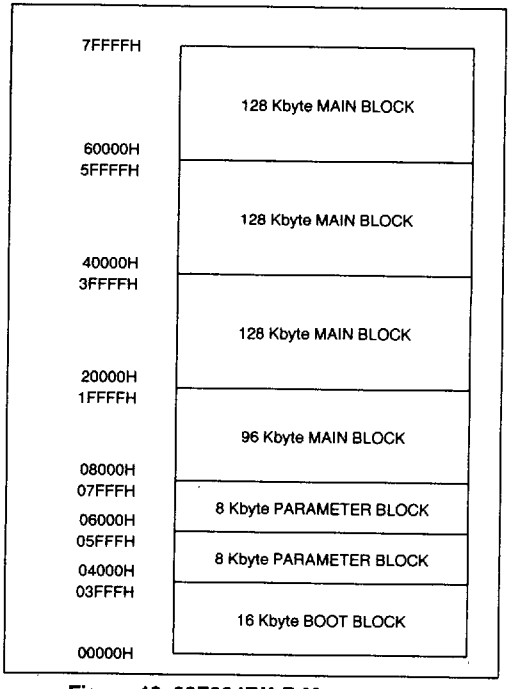

Figure 10. 28F004BX-B Memory Map

3.1.2.2 28F004BX-T Memory Map

The 28F004BX-T device has the 16 Kbyte boot block located from 7C000H to 7FFFFH to accommodate those microprocessors that boot from the top of the address map. In the 28F004BX-T the first 8 Kbyte parameter block resides in memory space from 7A000H to 7BFFFH. The second 8 Kbyte parameter block resides in memory space from 78000H to 79FFFH. The 96 Kbyte main block resides in memory space from 60000H to 77FFFH. The three 128 Kbyte main blocks reside in memory space from 40000H to 5FFFFH, 20000H to 3FFFFH and 00000H to 1FFFFH.

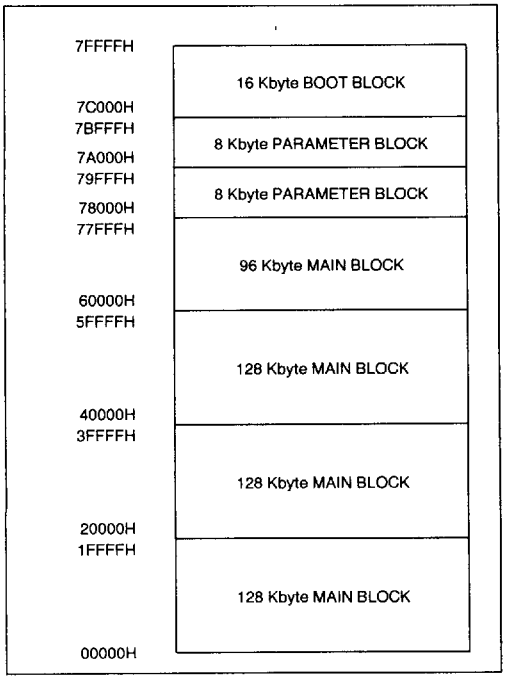

Figure 11. 28F004BX-T Memory Map

4.0 PRODUCT FAMILY PRINCIPLES OF OPERATION

Flash memory augments EPROM functionality with in-circuit electrical write and erase. The 4 Mbit flash family utilizes a Command User Interface (CUI) and internally generated and timed algorithms to simplify write and erase operations.

The CUI allows for 100% TTL-level control inputs, fixed power supplies during erasure and programming, and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 4 Mbit boot block flash family will only successfully execute the following commands: Read Array, Read Status Register, Clear Status Register and Intelligent Identifier mode. The device provides standard EPROM read, standby and output disable operations. Manufacturer Identification and Device Identification data can be accessed through the CUI or through the standard EPROM A_9 high voltage access (V_{ID}) for PROM programming equipment.

The same EPROM read, standby and output disable functions are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} allows write and erase of the device. All functions associated with altering memory contents: write and erase, Intelligent Identifier read and Read Status are accessed via the CUI.

The purpose of the Write State Machine (WSM) is to completely automate the write and erasure of the device. The WSM will begin operation upon receipt of a signal from the CUI and will report status back through a Status Register. The CUI will handle the $\overline{WE}$ interface to the data and address latches, as well as system software requests for status while the WSM is in operation.

4.1 28F400BX Bus Operations

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

Table 1. Bus Operations for WORD-WIDE Mode ($\overline{BYTE}$ = V_{IH})

Mode	Notes	$\overline{PWD}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_9	A_0	V_{PP}	DQ_{0-15}
Read	1, 2, 3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	High Z
Deep Power-Down	9	V_{IL}	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	0089H
Intelligent Identifier (Device)	4, 5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	4470H 4471H
Write	6, 7, 8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	D_{IN}

Table 2. Bus Operations for BYTE-WIDE Mode (BYTE = V_{IL})

Mode	Notes	$\overline{PWD}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_9	A_0	A_{-1}	V_{PP}	DQ_{0-7}	DQ_{8-14}
Read	1, 2, 3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	X	D_{OUT}	High Z
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	High Z	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	X	High Z	High Z
Deep Power-Down	9	V_{IL}	X	X	X	X	X	X	X	High Z	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	X	89H	High Z
Intelligent Identifier (Device)	4, 5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	X	70H 71H	High Z
Write	6, 7, 8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	X	D_{IN}	High Z

NOTES:
1. Refer to DC Characteristics.
2. X can be V_L, V_{IH} for control pins and addresses, V_{PPL} or V_{PPH} for V_{PP}.
3. See DC Characteristics for V_{PPL}, V_{PPH}, V_{HH}, V_{ID} voltages.
4. Manufacturer and Device codes may also be accessed via a CUI write sequence. A_1–A_{17} = X.
5. Device ID = 4470H for 28F400BX-T and 4471H for 28F400BX-B.
6. Refer to Table 4 for valid D_{IN} during a write operation.
7. Command writes for Block Erase or Word/Byte Write are only executed when V_{PP} = V_{PPH}.
8. To write or erase the boot block, hold $\overline{PWD}$ at V_{HH}.
9. $\overline{PWD}$ must be at GND ±0.2V to meet the 1.2 µA maximum deep power-down current.

4.2 28F004BX Bus Operations

Table 3. Bus Operations

Mode	Notes	$\overline{PWD}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_9	A_0	V_{PP}	DQ_{0-7}
Read	1, 2, 3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	X	High Z
Deep Power-Down	9	V_{IL}	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr)	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	89H
Intelligent Identifier (Device)	4, 5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	78H 79H
Write	6, 7, 8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	D_{IN}

NOTES:
1. Refer to DC Characteristics.
2. X can be V_{IL} or V_{IH} for control pins and addresses, V_{PPL} or V_{PPH} for V_{PP}.
3. See DC Characteristics for V_{PPL}, V_{PPH}, V_{HH}, V_{ID} voltages.
4. Manufacturer and Device codes may also be accessed via a CUI write sequence. A_1–A_{18} = X.
5. Device ID = 78H for 28F004BX-T and 79H for 28F004BX-B.
6. Refer to Table 4 for valid D_{IN} during a write operation.
7. Command writes for Block erase or byte program are only executed when V_{PP} = V_{PPH}.
6. Program or erase the Boot block by holding $\overline{PWD}$ at V_{HH}.
9. $\overline{PWD}$ must be at GND ±0.2V to meet the 1.2 µA maximum deep power-down current.

3

4.3 Read Operations

The 4 Mbit boot block flash family has three user read modes; Array, Intelligent Identifier, and Status Register. Status Register read mode will be discussed in detail in the "Write Operations" section.

During power-up conditions (V_{CC} supply ramping), it takes a maximum of 600 ns from when V_{CC} is at 4.5V minimum to valid data on the outputs.

4.3.1 READ ARRAY

If the memory is not in the Read Array mode, it is necessary to write the appropriate read mode command to the CUI. The 4 Mbit boot block flash family has three control functions, all of which must be logically active, to obtain data at the outputs. Chip-Enable $\overline{CE}$ is the device selection control. Power-Down $\overline{PWD}$ is the device power control. Output-Enable $\overline{OE}$ is the DATA INPUT/OUTPUT (DQ[0:15] or DQ[0:7]) direction control and when active is used to drive data from the selected memory on to the I/O bus.

4.3.1.1 Output Control

With $\overline{OE}$ at logic-high level (V_{IH}), the output from the device is disabled and data input/output pins (DQ[0:15] or DQ[0:7] are tri-stated. Data input is then controlled by $\overline{WE}$.

4.3.1.2 Input Control

With $\overline{WE}$ at logic-high level (V_{IH}), input to the device is disabled. Data Input/Output pins (DQ[0:15] or DQ[0:7]) are controlled by $\overline{OE}$.

4.3.2 INTELLIGENT IDENTIFIERS

28F400BX PRODUCTS

The manufacturer and device codes are read via the CUI or by taking the A_9 pin to 12V. Writing 90H to the CUI places the device into Intelligent Identifier read mode. A read of location 00000H outputs the manufacturer's identification code, 0089H, and location 00001H outputs the device code; 4470H for 28F400BX-T, 4471H for 28F400BX-B. When $\overline{BYTE}$ is at a logic low only the lower byte of the above signatures is read and DQ_{15}/A_{-1} is a "don't care" during Intelligent Identifier mode. A read array command must be written to the memory to return to the read array mode.

28F004BX PRODUCTS

The manufacturer and device codes are also read via the CUI or by taking the A_9 pin to 12V. Writing 90H to the CUI places the device into Intelligent Identifier read mode. A read of location 00000H outputs the manufacturer's identification code, 89H, and location 00001H outputs the device code; 78H for 28F004BX-T, 79H for 28F004BX-B.

4.4 Write Operations

Commands are written to the CUI using standard microprocessor write timings. The CUI serves as the interface between the microprocessor and the internal chip operation. The CUI can decipher Read Array, Read Intelligent Identifier, Read Status Register, Clear Status Register, Erase and Program commands. In the event of a read command, the CUI simply points the read path at either the array, the Intelligent Identifier, or the status register depending on the specific read command given. For a program or erase cycle, the CUI informs the write state machine that a write or erase has been requested. During a program cycle, the Write State Machine will control the program sequences and the CUI will only respond to status reads. During an erase cycle, the CUI will respond to status reads and erase suspend. After the Write State Machine has completed its task, it will allow the CUI to respond to its full command set. The CUI will stay in the current command state until the microprocessor issues another command.

The CUI will successfully initiate an erase or write operation only when V_{PP} is within its voltage range. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable, available only when memory updates are desired. The system designer can also choose to "hard-wire" V_{PP} to 12V. The 4 Mbit boot block flash family is designed to accommodate—either design practice. It is recommended that $\overline{PWD}$ be tied to logical Reset for data protection during unstable CPU reset function as described in the "Product Family Overview" section.

4.4.1 BOOT BLOCK WRITE OPERATIONS

In the case of Boot Block modifications (write and erase), $\overline{PWD}$ is set to V_{HH} = 12V typically, in addition to V_{PP} at high voltage.

However, if $\overline{PWD}$ is not at V_{HH} when a program or erase operation of the boot block is attempted, the corresponding status register bit (Bit 4 for Program and Bit 5 for Erase, refer to Table 5 for Status Register Definitions) is set to indicate the failure to complete the operation.

4.4.2 COMMAND USER INTERFACE (CUI)

The Command User Interface (CUI) serves as the interface to the microprocessor. The CUI points the read/write path to the appropriate circuit block as described in the previous section. After the WSM has completed its task, it will set the WSM Status bit to a "1", which will also allow the CUI to respond to its full command set. Note that after the WSM has returned control to the CUI, the CUI will remain in its current state.

4.4.2.1 Command Set

Command Codes	Device Mode
00	Invalid/Reserved
10	Alternate Program Setup
20	Erase Setup
40	Program Setup
50	Clear Status Register
70	Read Status Register
90	Intelligent Identifier
B0	Erase Suspend
D0	Erase Resume/Erase Confirm
FF	Read Array

4.4.2.2 Command Function Descriptions

Device operations are selected by writing specific commands into the CUI. Table 4 defines the 4 Mbit boot block flash family commands.

Table 4. Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
		8	Operation	Address	Data	Operation	Address	Data
Read Array	1	1	Write	X	FFH			
Intelligent Identifier	3	2, 4	Write	X	90H	Read	IA	IID
Read Status Register	2	3	Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Erase Setup/Erase Confirm	2	5	Write	BA	20H	Write	BA	D0H
Word/Byte Write Setup/Write	2	6, 7	Write	WA	40H	Write	WA	WD
Erase Suspend/Erase Resume	2		Write	X	B0H	Write	X	D0H
Alternate Word/Byte Write Setup/Write	2	6, 7	Write	WA	10H	Write	WA	WD

NOTES:
1. Bus operations are defined in Tables 1, 2, 3.
2. IA = Identifier Address: 00H for manufacturer code, 01H for device code.
3. SRD = Data read from Status Register.
4. IID = Intelligent Identifier Data.
Following the Intelligent Identifier Command, two read operations access manufacturer and device codes.
5. BA = Address within the block being erased.
6. WA = Address to be written.
WD = Data to be written at location WD.
7. Either 40H or 10H commands is valid.
8. When writing commands to the device, the upper data bus [DQ_8–DQ_{15}] = X (28F400BX-only) which is either V_{CC} or V_{SS} to avoid burning additional current.

3

Invalid/Reserved

These are unassigned commands. It is not recommended that the customer use any command other than the valid commands specified above. Intel reserves the right to redefine these codes for future functions.

Read Array (FFH)

This single write command points the read path at the array. If the host CPU performs a $\overline{CE}/\overline{OE}$ controlled read immediately following a two-write sequence that started the WSM, then the device will output status register contents. If the Read Array command is given after Erase Setup the device is reset to read the array. A two Read Array command sequence (FFH) is required to reset to Read Array after Program Setup.

Intelligent Identifier (90H)

After this command is executed, the CUI points the output path to the Intelligent Identifier circuits. Only Intelligent Identifier values at addresses 0 and 1 can be read (only address A_0 is used in this mode, all other address inputs are ignored).

Read Status Register (70H)

This is one of the two commands that is executable while the state machine is operating. After this command is written, a read of the device will output the contents of the status register, regardless of the address presented to the device.

The device automatically enters this mode after program or erase has completed.

Clear Status Register (50H)

The WSM can only set the Program Status and Erase Status bits in the status register, it can not clear them. Two reasons exist for operating the status register in this fashion. The first is a synchronization. The WSM does not know when the host CPU has read the status register, therefore it would not know when to clear the status bits. Secondly, if the CPU is programming a string of bytes, it may be more efficient to query the status register after programming the string. Thus, if any errors exist while programming the string, the status register will return the accumulated error status.

Program Setup (40H or 10H)

This command simply sets the CUI into a state such that the next write will load the address and data registers. Either 40H or 10H can be used for Program Setup. Both commands are included to accommodate efforts to achieve an industry standard command code set.

Program

The second write after the program setup command, will latch addresses and data. Also, the CUI initiates the WSM to begin execution of the program algorithm. While the WSM finishes the algorithm, the device will output Status Register contents. Note that the WSM cannot be suspended during programming.

Erase Setup (20H)

Prepares the CUI for the Erase Confirm command. No other action is taken. If the next command is not an Erase Confirm command then the CUI will set both the Program Status and Erase Status bits of the Status Register to a "1", place the device into the Read Array state, and wait for another command.

Erase Confirm (D0H)

If the previous command was an Erase Setup command, then the CUI will enable the WSM to erase, at the same time closing the address and data latches, and respond only to the Read Status Register and Erase Suspend commands. While the WSM is executing, the device will output Status Register data when $\overline{OE}$ is toggled low. Status Register data can only be updated by toggling either $\overline{OE}$ or $\overline{CE}$ low.

Erase Suspend (B0H)

This command only has meaning while the WSM is executing an Erase operation, and therefore will only be responded to during an erase operation. After this command has been executed, the CUI will set an output that directs the WSM to suspend Erase operations, and then return to responding to only Read Status Register or to the Erase Resume commands. Once the WSM has reached the Suspend state, it will set an output into the CUI which allows the CUI to respond to the Read Array, Read Status Register, and Erase Resume commands. In this mode, the CUI will not respond to any other commands. The WSM will also set the WSM Status bit to a "1". The WSM will continue to run, idling in the SUSPEND state, regardless of the state of all input control pins, with the exclusion of $\overline{PWD}$. $\overline{PWD}$ will immediately shut down the WSM and the remainder of the chip. During a suspend operation, the data and address latches will remain closed, but the address pads are able to drive the address into the read path.

Erase Resume (D0H)

This command will cause the CUI to clear the Suspend state and set the WSM Status bit to a "0", but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions.

4.4.3 STATUS REGISTER

The 4 Mbit boot block flash family contains a status register which may be read to determine when a program or erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status command to the CUI. After writing this command, all subsequent Read operations output data from the status register until another command is written to the CUI. A Read Array command must be written to the CUI to return to the Read Array mode.

The status register bits are output on DQ[0:7] whether the device is in the byte-wide (x8) or word-wide (x16) mode for the 28F400BX. In the word-wide mode the upper byte, DQ[8:15] is set to 00H during a Read Status command. In the byte-wide mode, DQ[8:14] are tri-stated and DQ_{15}/A_{-1} retains the low order address function.

It should be noted that the contents of the status register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$ whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the status register change while reading the status register. $\overline{CE}$ or $\overline{OE}$ must be toggled with each subsequent status read, or the completion of a program or erase operation will not be evident.

The Status Register is the interface between the microprocessor and the Write State Machine (WSM). When the WSM is active, this register will indicate the status of the WSM, and will also hold the bits indicating whether or not the WSM was successful in performing the desired operation. The WSM sets status bits "Three" through "Seven" and clears bits "Six" and "Seven", but cannot clear status bits "Three" through "Five". These bits can only be cleared by the controlling CPU through the use of the Clear Status Register command.

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4.4.3.1 Status Register Bit Definition

Table 5. Status Register Definitions

WSMS	ESS	ES	PS	VPPS	R	R	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	Write State Machine Status bit must first be checked to determine byte/word program or block erase completion, before the Program or Erase Status bits are checked for success.
SR.6 = ERASE SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed	When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1". ESS bit remains set to "1" until an Erase Resume command is issued.
SR.5 = ERASE STATUS 1 = Error in Block Erasure 0 = Successful Block Erase	When this bit is set to "1". WSM has applied the maximum number of erase pulses to the block and is still unable to successfully perform an erase verify.
SR.4 = PROGRAM STATUS 1 = Error In Byte/Word Program 0 = Successful Byte/Word Program	When this bit is set to "1", WSM has attempted but failed to Program a byte or word.
SR.3 = V_{PP} STATUS 1 = V_{PP} Low Detect; Operation Abort 0 = V_{PP} OK	The V_{PP} Status bit unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates the V_{PP} level only after the byte write or block erase command sequences have been entered and informs the system if V_{PP} has not been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.
SR.2–SR.0 = RESERVED FOR FUTURE ENHANCEMENTS	These bits are reserved for future use and should be masked out when polling the Status Register.

4.4.3.2 Clearing the Status Register

Certain bits in the status register are set by the write state machine, and can only be reset by the system software. These bits can indicate various failure conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The status register may then be read to determine if an error occurred during that programming or erasure series. This adds flexibility to the way the device may be programmed or erased. To clear the status register, the Clear Status Register command is written to the CUI. Then, any other command may be issued to the CUI. Note again that before a read cycle can be initiated, a Read Array command must be written to the CUI to specify whether the read data is to come from the array, status register, or Intelligent Identifier.

4.4.4 PROGRAM MODE

Program is executed by a two-write sequence. The Program Setup command is written to the CUI followed by a second write which specifies the address and data to be programmed. The write state machine will execute a sequence of internally timed events to:

1. Program the desired bits of the addressed memory word (byte), and
2. Verify that the desired bits are sufficiently programmed.

Programming of the memory results in specific bits within a byte or word being changed to a "0".

If the user attempts to program "1"s, there will be no change of the memory cell content and no error occurs.

Similar to erasure, the status register indicates whether programming is complete. While the program sequence is executing, bit 7 of the status register is a "0". The status register can be polled by toggling either $\overline{CE}$ or $\overline{OE}$ to determine when the program sequence is complete. Only the Read Status Register command is valid while programming is active.

When programming is complete, the status bits, which indicate whether the program operation was successful, should be checked. If the programming operation was unsuccessful, Bit 4 of the status register is set to a "1" to indicate a Program Failure. If Bit 3 is set then V_{PP} was not within acceptable limits, and the WSM will not execute the programming sequence.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, it must be recognized that reads from the memory, status register, or Intelligent Identifier cannot be accomplished until the CUI is given the appropriate command. A Read Array command must first be given before memory contents can be read.

Figure 12 shows a system software flowchart for device byte programming operation. Figure 13 shows a similar flowchart for device word programming operation (28F400BX-only).

4.4.5 ERASE MODE

Erasure of a single block is initiated by writing the Erase Setup and Erase Confirm commands to the CUI, along with the addresses, A[12:17] for the 28F400BX or A[12:18] for the 28F004BX, identifying the block to be erased. These addresses are latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1".

The WSM will execute a sequence of internally timed events to:

1. Program all bits within the block
2. Verify that all bits within the block are sufficiently programmed
3. Erase all bits within the block and
4. Verify that all bits within the block are sufficiently erased

While the erase sequence is executing, Bit 7 of the status register is a "0".

When the status register indicates that erasure is complete, the status bits, which indicate whether the erase operation was successful, should be checked. If the erasure operation was unsuccessful, Bit 5 of the status register is set to a "1" to indicate an Erase Failure. If V_{PP} was not within acceptable limits after the Erase Confirm command is issued, the WSM will not execute an erase sequence; instead, Bits of the status register is set to a "1" to indicate an Erase Failure, and Bit 3 is set to a "1" to identify that V_{PP} supply voltage was not within acceptable limits.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, it must be recognized that reads from the memory array, status register, or Intelligent Identifier can not be accomplished until the CUI is given the appropriate command. A Read Array command must first be given before memory contents can be read.

Figure 14 shows a system software flowchart for Block Erase operation.

4.4.5.1 Suspending and Resuming Erase

Since an erase operation typically requires 1 to 3 seconds to complete, an Erase Suspend command is provided. This allows erase-sequence interruption in order to read data from another block of the memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the Write State Machine (WSM) pause the erase sequence at a predetermined point in the erase algorithm. The status register must be read to determine when the erase operation has been suspended.

At this point, a Read Array command can be written to the CUI in order to read data from blocks other than that which is being suspended. The only other valid command at this time is the Erase Resume command or Read Status Register operation.

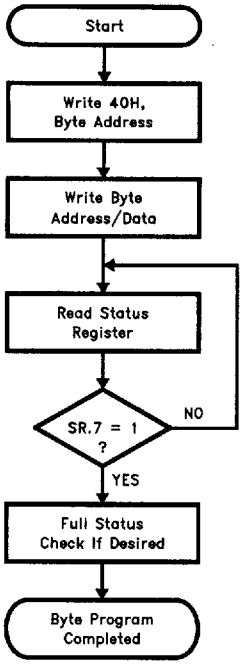
Figure 15 shows a system software flowchart detailing the operation.

During Erase Suspend mode, the chip can go into a pseudo-standby mode by taking $\overline{CE}$ to V_{IH} and the active current is now a maximum of 10 mA. If the chip is enabled while in this mode by taking $\overline{CE}$ to V_{IL}, the Erase Resume command can be issued to resume the erase operation.

Upon completion of reads from any block other than the block being erased, the Erase Resume command must be issued. When the Erase Resume command is given, the WSM will continue with the erase sequence and complete erasing the block. As with the end of erase, the status register must be read, cleared, and the next instruction issued in order to continue.

4.4.6 EXTENDED CYCLING

Intel has designed extended cycling capability into its ETOX III flash memory technology. The 4 Mbit boot block flash family is designed for 100,000 program/erase cycles on each of the seven blocks. The combination of low electric fields, clean oxide processing and minimized oxide area per memory cell subjected to the tunneling electric field, results in very high cycling capability.



290451-6

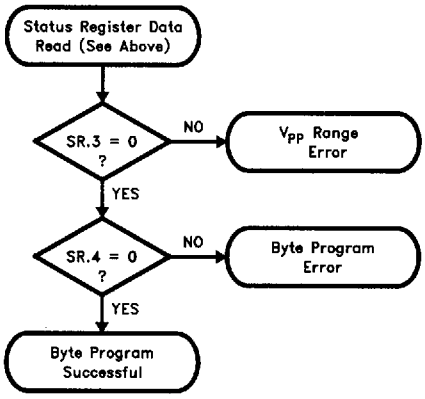
Bus Operation	Command	Comments
Write	Setup Program	Data = 40H Address = Byte to be programmed
Write	Program	Data to be programmed Address = Byte to be programmed
Read		Status Register Data. Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register
Standby		Check SR.7 1 = Ready, 0 = Busy

Repeat for subsequent bytes.

Full status check can be done after each byte or after a sequence of bytes.

Write FFH after the last byte programming operation to reset the device to Read Array Mode.

Full Status Check Procedure



290451-7

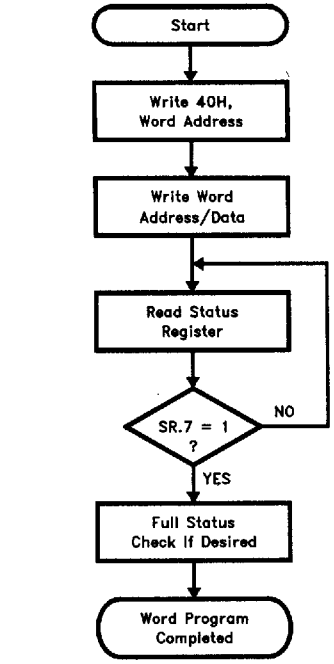
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = Byte Program Error

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the Clear Status Register Command, in cases where multiple bytes are programmed before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 12. Automated Byte Programming Flowchart



290451-8

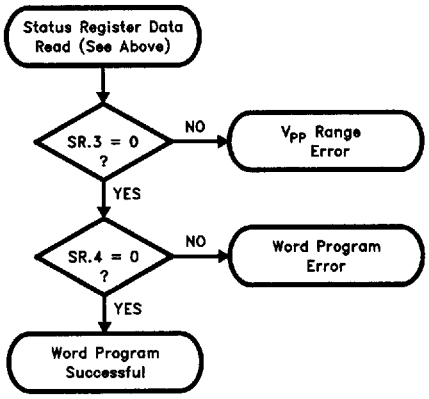
Bus Operation	Command	Comments
Write	Setup Program	Data = 40H Address = Word to be programmed
Write	Program	Data to be programmed Address = Word to be programmed
Read		Status Register Data. Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register
Standby		Check SR.7 1 = Ready, 0 = Busy

Repeat for subsequent words.

Full status check can be done after each word or after a sequence of words.

Write FFH after the last word programming operation to reset the device to Read Array Mode.

Full Status Check Procedure



290451-9

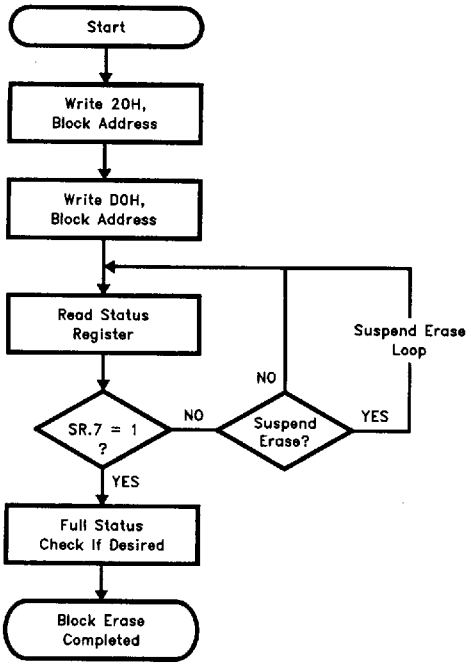
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = Word Program Error

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the Clear Status Register Command, in cases where multiple words are programmed before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 13. Automated Word Programming Flowchart



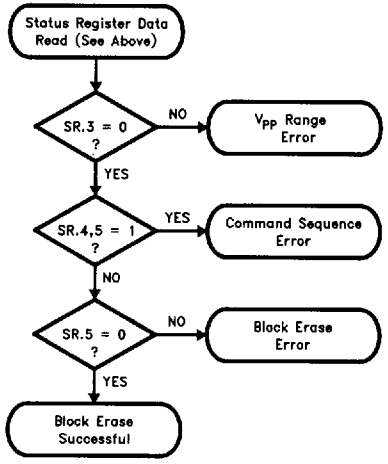
Bus Operation	Command	Comments
Write	Setup Erase	Data = 20H Address = Within block to be erased
Write	Erase	Data = D0H Address = Within block to be erased
Read		Status Register Data. Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register
Standby		Check SR.7 1 = Ready, 0 = Busy

Repeat for subsequent blocks.

Full status check can be done after each block or after a sequence of blocks.

Write FFH after the last block erase operation to reset the device to Read Array Mode.

Full Status Check Procedure



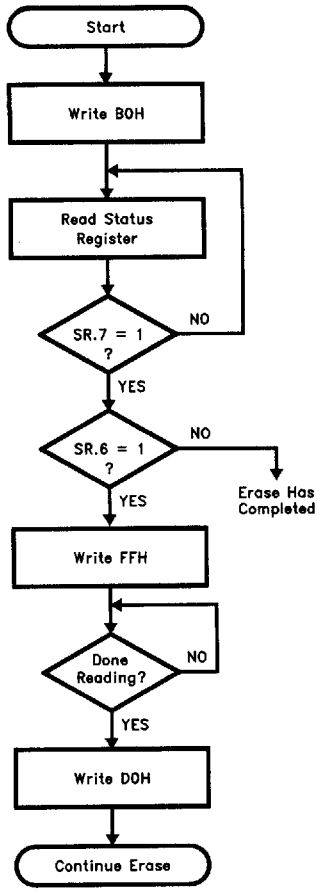
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.5 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 14. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H
Read		Status Register Data. Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register
Standby		Check SR.7 1 = Ready
Standby		Check SR.6 1 = Suspended
Write	Read Array	Data = FFH
Read		Read array data from block other than that being erased.
Write	Erase Resume	Data = D0H

Figure 15. Erase Suspend/Resume Flowchart

4.5 Power Consumption

4.5.1 ACTIVE POWER

With $\overline{CE}$ at a logic-low level and $\overline{PWD}$ at a logic-high level, the device is placed in the active mode. The device I_{CC} current is a maximum 60 mA at 10 MHz with TTL input signals.

4.5.2 AUTOMATIC POWER SAVINGS

Automatic Power Savings (APS) is a low pwer feature during active mode of operation. The 4 Mbit family of products incorporate Power Reduction Control (PRC) circuitry which basically allows the device to put itself into a low current state when it is not being accessed. After data is read from the memory array, PRC logic controls the device's power consumption by entering the APS mode where maximum I_{CC} current is 3 mA and typical I_{CC} current is 1 mA. The device stays in this static state with outputs valid until a new location is read.

4.5.3 STANDBY POWER

With $\overline{CE}$ at a logic-high level (V_{IH}), and the CUI in read mode, the memory is placed in standby mode where the maximum I_{CC} standby current is 100 μA with CMOS input signals. The standby operation disables much of the device's circuitry and substantially reduces device power consumption. The outputs (DQ[0:15] or DQ[0:7]) are placed in a high-impedance state independent of the status of the $\overline{OE}$ signal. When the 4 Mbit boot block flash family is deselected during erase or program functions, the devices will continue to perform the erase or program function and consume program or erase active power until program or erase is completed.

4.5.4 DEEP POWERDOWN

The 4 Mbit boot block flash family supports a typical I_{CC} of 0.2 µA in deep power-down mode. One of the target markets for these devices is in portable equipment where the power consumption of the machine is of prime importance. The 4 Mbit boot block flash family has a $\overline{PWD}$ pin which places the device in the deep powerdown mode. When $\overline{PWD}$ is at a logic-low (GND ±0.2V), all circuits are turned off and the device typically draws 0.2 µA of V_{CC} current.

During read modes, the $\overline{PWD}$ pin going low deselects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state, requires a minimum of 400 ns to access valid data (t_{PHQV}).

During erase or program modes, $\overline{PWD}$ low will abort either erase or program operation. The contents of the memory are no longer valid as the data has been corrupted by the $\overline{PWD}$ function. As in the read mode above, all internal circuitry is turned off to achieve the 0.2 µA current level.

$\overline{PWD}$ transitions to V_{IL} or turning power off to the device will clear the status register.

4.6 Power-up Operation

The 4 Mbit boot block flash family is designed to offer protection against accidental block erasure or programming during power transitions. Upon power-up the 4 Mbit boot block flash family is indifferent as to which power supply, V_{PP} or V_{CC}, powers-up first. Power supply sequencing is not required.

The 4 Mbit boot block flash family ensures the CUI is reset to the read mode on power-up.

In addition, on power-up the user must either drop $\overline{CE}$ low or present a new address to ensure valid data at the outputs.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides an added level of protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. Finally the device is disabled until $\overline{PWD}$ is brought to V_{IH}, regardless of the state of its control inputs. This feature provides yet another level of memory protection.

4.7 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling methods. System designers are interested in 3 supply current issues:

- Standby current levels (I_{CCS})
- Active current levels (I_{CCR})
- Transient peaks produced by falling and rising edges of $\overline{CE}$.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high frequency, low-inherent inductance capacitors should be placed as close as possible to the package leads.

4.7.1 V_{PP} TRACE ON PRINTED CIRCUIT BOARDS

Writing to flash memories while they reside in the target system, requires special consideration of the V_{PP} power supply trace by the printed circuit board designer. The V_{PP} pin supplies the flash memory cells current for programming and erasing. One should use similar trace widths and layout considerations given to the V_{CC} power supply trace. Adequate V_{PP} supply traces and decoupling will decrease spikes and overshoots.

4.7.2 V_{CC}, V_{PP} AND $\overline{PWD}$ TRANSITIONS

The CUI latches commands as issued by system software and is not altered by V_{PP} or $\overline{CE}$ transitions or WSM actions. Its state upon power-up, after exit from deep power-down mode or after V_{CC} transitions below V_{LKO} (Lockout voltage), is Read Array mode.

After any word/byte write or block erase operation is complete and even after V_{PP} transitions down to V_{PPL}, the CUI must be reset to Read Array mode via the Read Array command when accesses to the flash memory are desired.

ABSOLUTE MAXIMUM RATINGS*

Commercial Operating Temperature
During Read ..... 0°C to 70°C(1)
During Block Erase and Word/Byte Write ..... 0°C to 70°C
Temperature Under Bias ..... −10°C to +80°C

Extended Operating Temperature
During Read ..... −40°C to +85°C
During Block Erase and Word/Byte Write ..... −40°C to +85°C
Temperature Under Bias ..... −40°C to +85°C

Storage Temperature ..... −65°C to +125°C

Voltage on Any Pin (except V_{CC} and V_{PP}) with Respect to GND ..... −2.0V to +7.0V(2)

Voltage on Pin $\overline{PWD}$ or Pin A_9 with Respect to GND ..... −2.0V to +13.5V(2, 3)

V_{PP} Program Voltage with Respect to GND during Block Erase and Word/Byte Write ..... −2.0V to +14.0V(2, 3)

V_{CC} Supply Voltage with Respect to GND ..... −2.0V to +7.0V(2)

Output Short Circuit Current ..... 100 mA(4)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

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NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns.
Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum DC voltage on A_9 or V_{PP} may overshoot to +14.0V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. 10% V_{CC} specifications reference the 28F400BX-60/28F004BX-60 in their standard test configuration, and the 28F400BX-80/28F004BX-80.
6. 5% V_{CC} specifications reference the 28F400BX-60/28F004BX-60 in their high speed test configuration.

OPERATING CONDITIONS

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		0	70	°C
V_{CC}	V_{CC} Supply Voltage (10%)	5	4.50	5.50	V
V_{CC}	V_{CC} Supply Voltage (5%)	6	4.75	5.25	V

DC CHARACTERISTICS

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	1			±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND

DC CHARACTERISTICS (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{CCS}	V_{CC} Standby Current	1, 3			1.5	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = \overline{PWD} = V_{IH}$
					100	µA	$V_{CC} = V_{CC}$ Max $\overline{CE} = \overline{PWD} = V_{CC} \pm 0.2V$ 28F200BX: $\overline{BYTE} = V_{CC} \pm 0.2V$ or GND
I_{CCD}	V_{CC} Deep Powerdown Current	1		0.20	1.2	µA	$\overline{PWD}$ = GND ±0.2V
I_{CCR}	V_{CC} Read Current for 28F200BX Word-Wide Mode	1, 5, 6			60	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE}$ = GND f = 10 MHz, I_{OUT} = 0 mA CMOS Inputs
					65	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 10 MHz, I_{OUT} = 0 mA TTL Inputs
I_{CCR}	V_{CC} Read Current for 28F200BX Byte-Wide Mode and 28F004BX	1, 5, 6			55	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE}$ = GND f = 10 MHz, I_{OUT} = 0 mA CMOS Inputs
					60	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 10 MHz, I_{OUT} = 0 mA TTL Inputs
I_{CCW}	V_{CC} Word Write Current	1			70	mA	Word Write in Progress
I_{CCW}	V_{CC} Byte Write Current	1			60	mA	Byte Write in Progress
I_{CCE}	V_{CC} Block Erase Current	1			30	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1, 2		5	10	mA	Block Erase Suspended, $\overline{CE} = V_{IH}$
I_{PPS}	V_{PP} Standby Current	1			±10	µA	$V_{PP} \leq V_{CC}$
I_{PPD}	V_{PP} Deep PowerDown Current	1			5.0	µA	$\overline{PWD}$ = GND ±0.2V
I_{PPR}	V_{PP} Read Current	1			200	µA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Word Write Current	1			40	mA	$V_{PP} = V_{PPH}$ Word Write in Progress
I_{PPW}	V_{PP} Byte Write Current	1			30	mA	$V_{PP} = V_{PPH}$ Byte Write in Progress
I_{PPE}	V_{PP} Block Erase Current	1			30	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1			200	µA	$V_{PP} = V_{PPH}$ Block Erase Suspended
I_{ID}	A_9 Intelligent Identifier Current	1			500	µA	$A_9 = V_{ID}$
V_{ID}	A_9 Intelligent Identifier Voltage		11.5		13.0	V	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	$V_{CC} = V_{CC}$ Min I_{OL} = 5.8 mA

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DC CHARACTERISTICS (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
V_{OH}	Output High Voltage		2.4			V	$V_{CC} = V_{CC}$ Min $I_{OH} = -2.5$ mA
V_{PPL}	V_{PP} during Normal Operations	3	0.0		6.5	V	
V_{PPH}	V_{PP} during Erase/Write Operations	7	11.4	12.0	12.6	V	
V_{PPH}	V_{PP} during Erase/Write Operations	8	10.8	12.0	13.2	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0			V	
V_{HH}	$\overline{PWD}$ Unlock Voltage		11.5		13.0	V	Boot Block Write/Erase

EXTENDED TEMPERATURE OPERATING CONDITIONS

Symbol	Parameter	Notes	Min	Max	Unit
T_A	Operating Temperature		−40	85	°C
V_{CC}	V_{CC} Supply Voltage (10%)	5	4.50	5.50	V

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DC CHARACTERISTICS: EXTENDED TEMPERATURE OPERATION

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	1			±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1, 3			1.5	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = \overline{PWD} = V_{IH}$
					100	µA	$V_{CC} = V_{CC}$ Max $\overline{CE} = \overline{PWD} = V_{CC} \pm 0.2V$ 28F400BX: $\overline{BYTE} = V_{CC} \pm 0.2V$ or GND
I_{CCD}	V_{CC} Deep Power-Down Current	1		0.20	8	µA	$\overline{PWD}$ = GND ±2V

DC CHARACTERISTICS: EXTENDED TEMPERATURE OPERATION (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{CCR}	V_{CC} Read Current for 28F400BX Word-Wide Mode	1, 5, 6			70	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = GND$ f = 10 MHz, I_{OUT} = 0 mA CMOS Inputs
					75	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 10 MHz, I_{OUT} = 0 mA TTL Inputs
I_{CCR}	V_{CC} Read Current for 28F400BX Byte-Wide Mode and 28F004BX	1, 5, 6			65	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = GND$ f = 10 MHz, I_{OUT} = 0 mA CMOS Inputs
					70	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 10 MHz, I_{OUT} = 0 mA TTL Inputs
I_{CCW}	V_{CC} Word Write Current	1			75	mA	Word Write in Progress
I_{CCW}	V_{CC} Byte Write Current	1			65	mA	Byte Write in Progress
I_{CCE}	V_{CC} Block Erase Current	1			40	mA	Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1, 2		5	10	mA	Block Erase Suspended, $\overline{CE} = V_{IH}$
I_{PPS}	V_{PP} Standby Current	1			±10	μA	$V_{PP} \leq V_{CC}$
I_{PPD}	V_{CC} Deep Power-Down Current	1			5.0	μA	$\overline{PWD} = GND \pm 0.2V$
I_{PPR}	V_{PP} Read Current	1			200	μA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Word Write Current	1			40	mA	$V_{PP} = V_{PPH}$ Word Write in Progress
I_{PPW}	V_{PP} Byte Write Current	1			40	mA	$V_{PP} = V_{PPH}$ Byte Write in Progress

DC CHARACTERISTICS: EXTENDED TEMPERATURE OPERATION (Continued)

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{PPE}	V_{PP} Block Erase Current	1			30	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1			200	µA	$V_{PP} = V_{PPH}$ Block Erase Suspended
I_{ID}	A_9 Intelligent Identifier Current	1			500	µA	$A_9 = V_{ID}$
V_{ID}	A_9 Intelligent Identifier Current		11.5		13.0	V	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	$V_{CC} = V_{CC}$ Min I_{OL} = 5.8 mA
V_{OH}	Output High Voltage		2.4			V	$V_{CC} = V_{CC}$ Min I_{OH} = −2.5 mA
V_{PPL}	V_{PP} during Normal Operations	3	0.0		6.5	V	
V_{PPH}	V_{PP} during Erase/Write Operations	7	11.4	12.0	12.6	V	
V_{PPH}	V_{PP} during Erase/Write Operations	8	10.8	12.0	13.2	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.0			V	
V_{HH}	$\overline{PWD}$ Unlock Voltage		11.5		13.0	V	Boot Block Write/Erase

CAPACITANCE[4] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	10	12	pF	$V_{OUT} = 0V$

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If the device is read while in Erase Suspend Mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block Erases and Word/Byte Writes are inhibited when $V_{PP} = V_{PPL}$ and not guaranteed in the range between V_{PPH} and V_{PPL}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to less than 1 mA typical in static operation.
6. CMOS Inputs are either V_{CC} ±0.2V or GND ±0.2V. TTL Inputs are either V_{IL} or V_{IH}.
7. V_{PP} = 12.0V ± 5% for applications requiring 100,000 block erase cycles.
8. V_{PP} = 12.0V ± 10% for applications requiring wider V_{PP} tolerances at 100 block erase cycles.
9. For the 28F004BX address pin A_{10} follows the C_{OUT} capacitance numbers.

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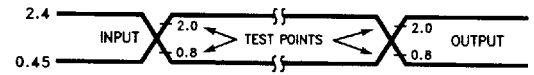
STANDARD TEST CONFIGURATION(1)

STANDARD AC INPUT/OUTPUT REFERENCE WAVEFORM



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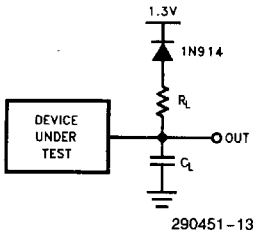
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) < 10 ns.

STANDARD AC TESTING LOAD CIRCUIT



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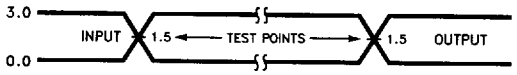
C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 KΩ

HIGH SPEED TEST CONFIGURATION(2)

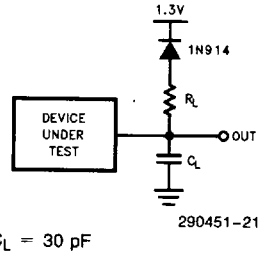
HIGH SPEED AC INPUT/OUTPUT REFERENCE WAVEFORM



290451-22

AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a logic "0". Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10 ns.

HIGH SPEED AC TESTING LOAD CIRCUIT



290451-21

C_L = 30 pF
C_L Includes Jig Capacitance
R_L = 3.3 KΩ

NOTES:
1. Testing characteristics for 28F400BX-60/28F004BX-60 in standard test configuration and 28F400BX-80/28F004BX-80.
2. Testing characteristics for 28F400BX-60/28F004BX-60 in high speed test configuration.

AC CHARACTERISTICS—Read Only Operations[1]

Versions		$V_{CC} \pm 5\%$		28F400BX-60[4] 28F004BX-60[4]						Unit
		$V_{CC} \pm 10\%$				28F400BX-60[5] 28F004BX-60[5]		28F400BX-80[5] 28F004BX-80[5]		
Symbol		Parameter	Notes	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time		60		70		80		ns
t_{AVQV}	t_{ACC}	Address to Output Delay			60		70		80	ns
t_{ELQV}	t_{CE}	$\overline{CE}$ to Output Delay	2		60		70		80	ns
t_{PHQV}	t_{PWH}	$\overline{PWD}$ High to Output Delay			300		300		300	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ to Output Delay	2		30		35		40	ns
t_{ELQX}	t_{LZ}	$\overline{CE}$ to Output Low Z	3	0		0		0		ns
t_{EHQZ}	t_{HZ}	$\overline{CE}$ High to Output High Z	3		20		25		30	ns
t_{GLQX}	t_{OLZ}	$\overline{OE}$ to Output Low Z	3	0		0		0		ns
t_{GHQZ}	t_{DF}	$\overline{OE}$ High to Output High Z	3		20		25		30	ns
	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change, Whichever is First	3	0		0		0		ns
t_{ELFL} t_{ELFH}		$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High	3		5		5		5	ns
t_{FHQV}		$\overline{BYTE}$ Switching High to Valid Output Delay	3, 6		60		70		80	ns
t_{FLQZ}		$\overline{BYTE}$ Switching Low to Output High Z	3		20		25		30	ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. See High Speed Test Configuration.
5. See Standard Test Configuration.
6. t_{FLQV}, $\overline{BYTE}$ switching low to valid output delay, will be equal to t_{AVQV}, measured from the time DQ_{15}/A_{-1} becomes valid.

3

T-46-13-26

EXTENDED TEMPERATURE OPERATION
AC CHARACTERISTICS—Read Only Operations[1]

Versions				T28F400BX-90[4, 5] T28F004BX-80		Unit
Symbol		Parameter	Notes	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time		90		ns
t_{AVQV}	t_{ACC}	Address to Output Delay			90	ns
t_{ELQV}	t_{CE}	$\overline{CE}$ to Output Delay			90	ns
t_{PHQV}	t_{PWH}	$\overline{PWD}$ High to Output Delay			300	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ to Output Delay	2		45	ns
t_{ELQX}	t_{LZ}	$\overline{CE}$ to Output Low Z		0		ns
t_{EHQZ}	t_{HZ}	$\overline{CE}$ High to Output High Z			35	ns
t_{GLQX}	t_{OLZ}	$\overline{OE}$ to Output Low Z	3	0		ns
t_{GHQZ}	t_{DF}	$\overline{OE}$ High to Output High Z	3		35	ns
	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change, Whichever is First	3	0		ns
t_{ELFL} t_{ELFH}		$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High	3		5	ns
t_{FHQV}		$\overline{BYTE}$ Switching High to Valid Output Delay	3, 5		90	ns
t_{FLQZ}		$\overline{BYTE}$ Switching Low to Output High Z	3		35	ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. See Standard Test Configuration.
5. t_{FLQV}, $\overline{BYTE}$ switching low to valid output delay, will be equal to t_{AVQV} from the time DQ_{15}/A_{-1} becomes valid.

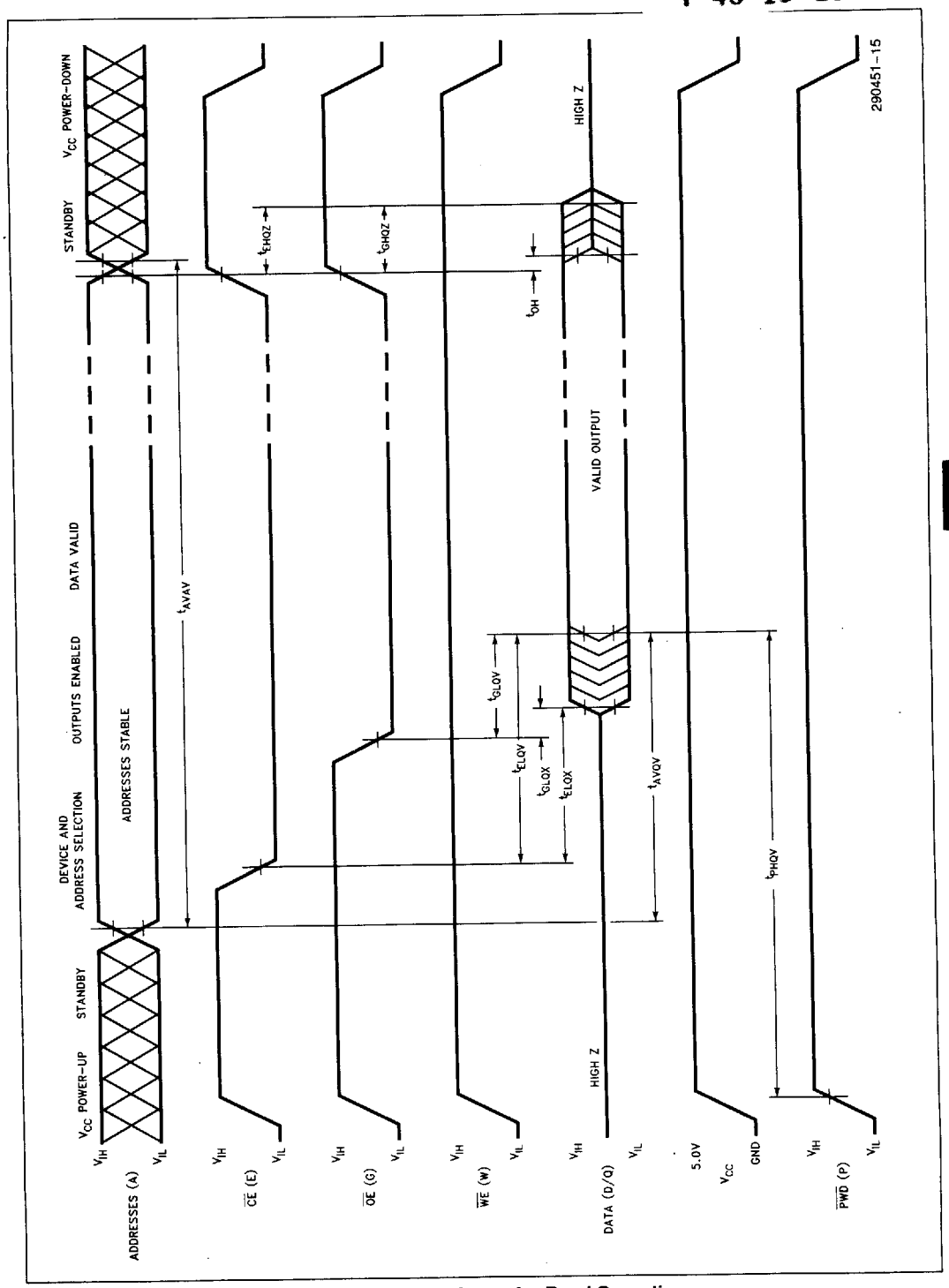


Figure 16. A.C. Waveforms for Read Operations

T-46-13-26

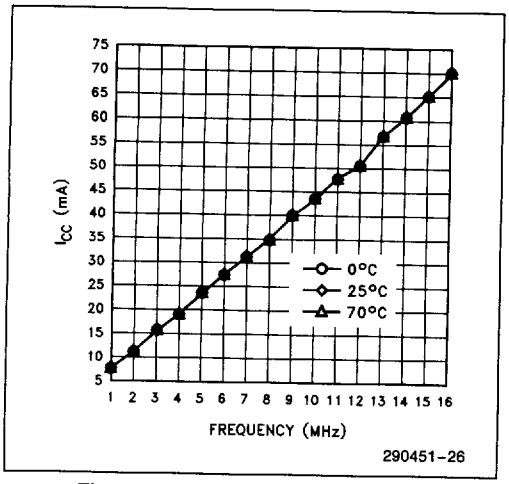


Figure 17. I_{CC} (RMS) vs Frequency (V_{CC} = 5.5V for x16 Operation

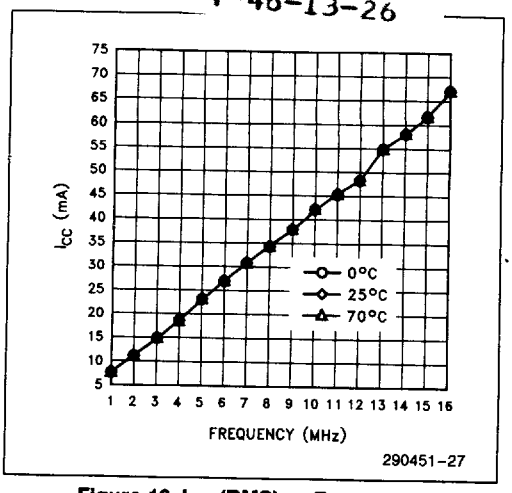


Figure 18. I_{CC} (RMS) vs Frequency (V_{CC} = 5.5V) for x8 Operation

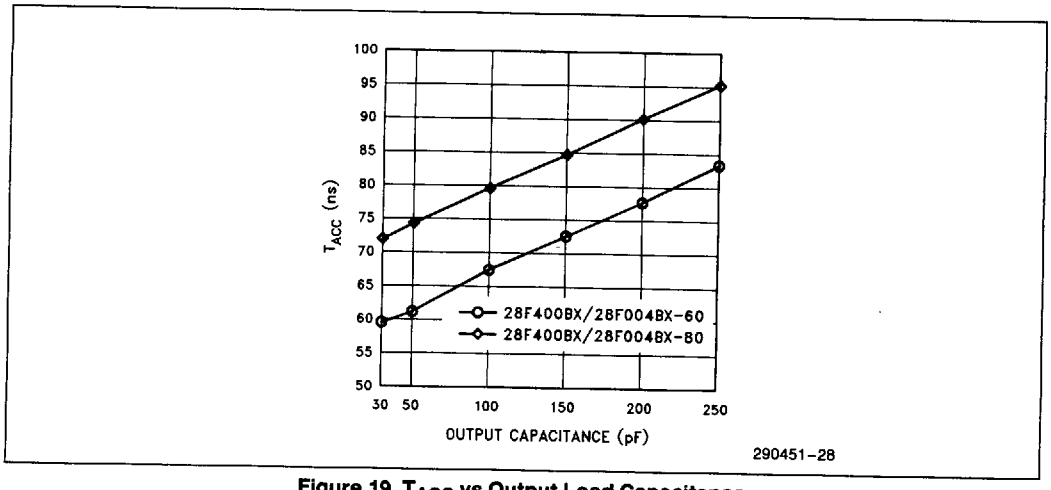


Figure 19. T_{ACC} vs Output Load Capacitance

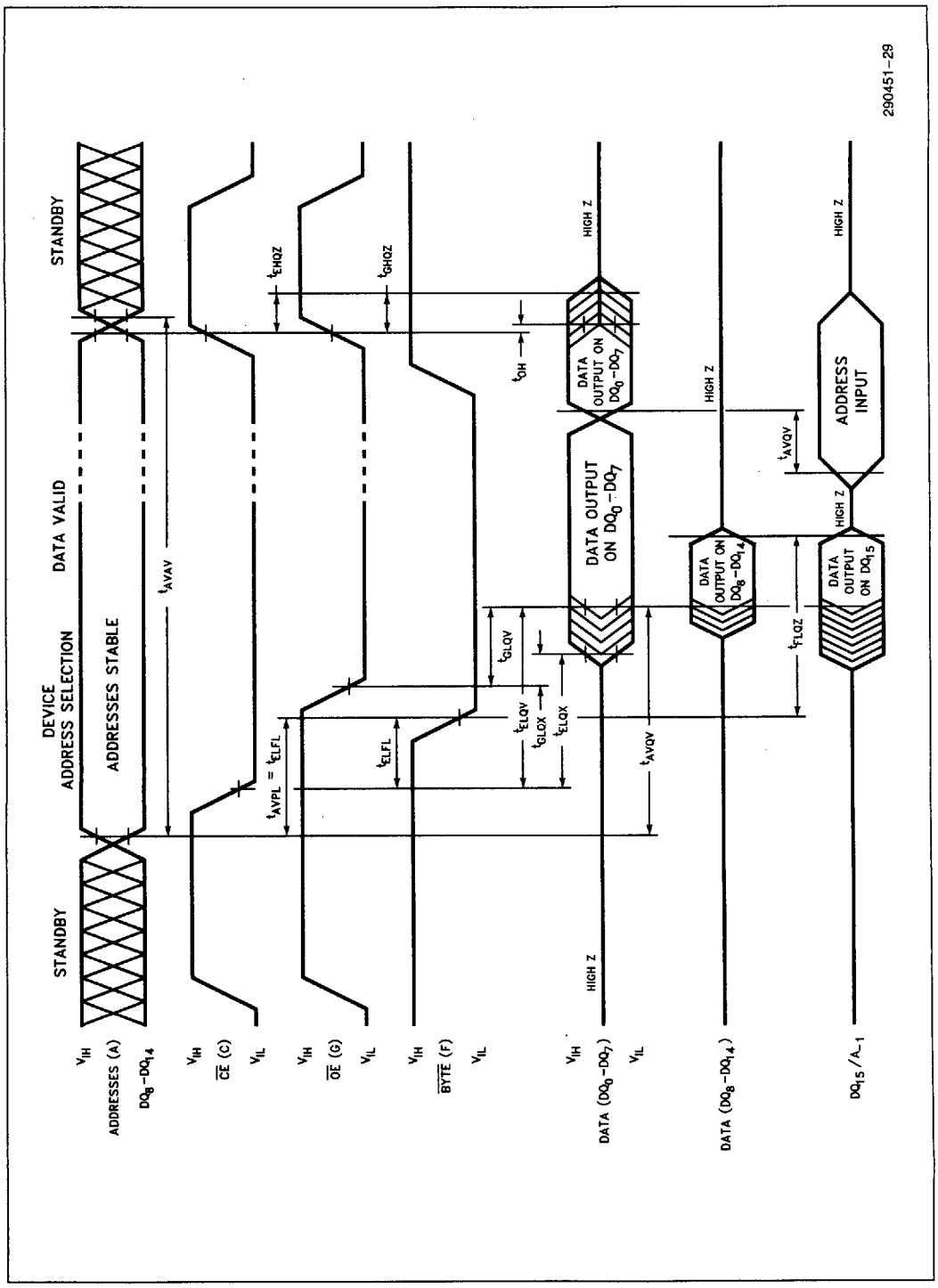


Figure 20. $\overline{BYTE}$ Timing Diagram for Both Read and Write Operations for 28F400BX

AC CHARACTERISTICS—$\overline{WE}$ Controlled Write Operations(1)

Versions		$V_{CC} \pm 5\%$		28F400BX-60(9) 28F004BX-60(9)						Unit
		$V_{CC} \pm 10\%$				28F400BX-60(10) 28F004BX-60(10)		28F400BX-80(10) 28F004BX-80(10)		
Symbol		Parameter	Notes	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		60		70		80		ns
t_{PHWL}	t_{PS}	$\overline{PWD}$ High Recovery to $\overline{WE}$ Going Low		215		215		215		ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		0		0		0		ns
t_{PHHWH}	t_{PHS}	$\overline{PWD}$ V_{HH} Setup to $\overline{WE}$ Going High	6, 8	100		100		100		ns
t_{VPWH}	t_{VPS}	V_{PP} Setup to $\overline{WE}$ Going High	5, 8	100		100		100		ns
t_{AVWH}	t_{AS}	Address Setup to $\overline{WE}$ Going High	3	50		50		50		ns
t_{DVWH}	t_{DS}	Data Setup to $\overline{WE}$ Going High	4	50		50		50		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width		50		50		50		ns
t_{WHDX}	t_{DH}	Data Hold from $\overline{WE}$ High	4	0		0		0		ns
t_{WHAX}	t_{AH}	Address Hold from $\overline{WE}$ High	3	10		10		10		ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold from $\overline{WE}$ High		10		10		10		ns
t_{WHWL}	t_{WPH}	$\overline{WE}$ Pulse Width High		10		20		30		ns
t_{WHQV1}		Duration of Word/Byte Programming Operation	2, 5	6		6		6		μs
t_{WHQV2}		Duration of Erase Operation (Boot)	2, 5, 6	0.3		0.3		0.3		s
t_{WHQV3}		Duration of Erase Operation (Parameter)	2, 5	0.3		0.3		0.3		s
t_{WHQV4}		Duration of Erase Operation (Main)	2, 5	0.6		0.6		0.6		s
t_{QWL}	t_{VPH}	V_{PP} Hold from Valid SRD	5, 8	0		0		0		ns
t_{QVPH}	t_{PHH}	$\overline{PWD}$ V_{HH} Hold from Valid SRD	6, 8	0		0		0		ns
t_{PHBR}		Boot-Block Relock Delay	7, 8		100		100		100	ns

AC CHARACTERISTICS—$\overline{WE}$ Controlled Write Operations(1) (Continued)

NOTES:
1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC characteristics during Read Mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled internally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}.
4. Refer to command definition table for valid D_{IN}.
5. Program/Erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For Boot Block Program/Erase, $\overline{PWD}$ should be held at V_{HH} until operation completes successfully.
7. Time t_{PHBR} is required for successful relocking of the Boot Block.
8. Sampled but not 100% tested.
9. See High Speed Test Configuration.
10. See Standard Test Configuration.

BLOCK ERASE AND WORD/BYTE WRITE PERFORMANCE V_{PP} = 12.0V ±5%

Parameter	Notes	28F400BX-60 28F004BX-60			28F400BX-80 28F004BX-80			Unit
		Min	Typ(1)	Max	Min	Typ(1)	Max	
Boot/Parameter Block Erase Time	2		1.0	7		1.0	7	s
Main Block Erase Time	2		2.4	14		2.4	14	s
Main Block Byte Program Time	2		1.2	4.2		1.2	4.2	s
Main Block Word Program Time	2		0.6	2.1		0.6	2.1	s

NOTES:
1. 25°C
2. Excludes System-Level Overhead.

BLOCK ERASE AND WORD/BYTE WRITE PERFORMANCE V_{PP} = 12.0V ±10%

Parameter	Notes	28F400BX-60 28F004BX-60			28F400BX-80 28F004BX-80			Unit
		Min	Typ(1)	Max	Min	Typ(1)	Max	
Boot/Parameter Block Erase Time	2		5.8	40		5.8	40	s
Main Block Erase Time	2		14	60		14	60	s
Main Block Byte Program Time	2		6.0	20		6.0	20	s
Main Block Word Program Time	2		3.0	10		3.0	10	s

NOTES:
1. 25°C
2. Excludes System-Level Overhead.

EXTENDED TEMPERATURE OPERATION
AC CHARACTERISTICS—$\overline{WE}$ Controlled Write Operations[1]

Versions[4]				T28F400BX-90[9] T28F004BX-90[9]		Unit
Symbol		Parameter	Notes	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		90		ns
t_{PHWL}	t_{PS}	$\overline{PWD}$ High Recovery to $\overline{WE}$ Going Low		210		ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		0		ns
t_{PHHWH}	t_{PHS}	$\overline{PWD}$ V_{HH} Setup to $\overline{WE}$ Going High	6, 8	100		ns
t_{VPWH}	t_{VPS}	V_{PP} Setup to $\overline{WE}$ Going High	5, 8	100		ns
t_{AVWH}	t_{AS}	Address Setup to $\overline{WE}$ Going High	3	60		ns
t_{DVWH}	t_{DS}	Data Setup to $\overline{WE}$ Going High	4	60		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width		60		ns
t_{WHDX}	t_{DH}	Data Hold from $\overline{WE}$ High	4	0		ns
t_{WHAX}	t_{AH}	Address Hold from $\overline{WE}$ High	3	10		ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold from $\overline{WE}$ High		10		ns
t_{WHWL}	t_{WPH}	$\overline{WE}$ Pulse Width High		30		ns
t_{WHQV1}		Duration of Word/Byte Programming Operation	2, 5	7		μs
t_{WHQV2}		Duration of Erase Operation (Boot)	2, 5, 6	0.4		s
t_{WHQV3}		Duration of Erase Operation (Parameter)	2, 5	0.4		s
t_{WHQV4}		Duration of Erase Operation (Main)	2, 5	0.7		s
t_{QWL}	t_{VPH}	V_{PP} Hold from Valid SRD	5, 8	0		ns
t_{QVPH}	t_{PHH}	$\overline{PWD}$ V_{HH} Hold from Valid SRD	6, 8	0		ns
t_{PHBR}		Boot-Block Relock Delay	7, 8		100	ns

EXTENDED TEMPERATURE OPERATION
AC CHARACTERISTICS—$\overline{WE}$ Controlled Write Operations[1] (Continued)

NOTES:
1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC characteristics during Read Mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled internally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}.
4. Refer to command definition table for valid D_{IN}.
5. Program/Erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For Boot Block Program/Erase, $\overline{PWD}$ should be held at V_{HH} until operation completes successfully.
7. Time t_{PHBR} is required for successful relocking of the Boot Block.
8. Sampled but not 100% tested.
9. See Standard Test Configuration.

EXTENDED TEMPERATURE OPERATION
BLOCK ERASE AND WORD/BYTE WRITE PERFORMANCE V_{PP} = 12.0V ±5%

Parameter	Notes	T28F400BX-90 T28F004BX-90			Unit
		Min	Typ[1]	Max	
Boot/Parameter Block Erase Time	2		1.5	10.5	s
Main Block Erase Time	2		3.0	18	s
Main Block Byte Program Time	2		1.4	5.0	s
Main Block Word Program Time	2		0.7	2.5	s

NOTES:
1. 25°C
2. Excludes System-Level Overhead.

3

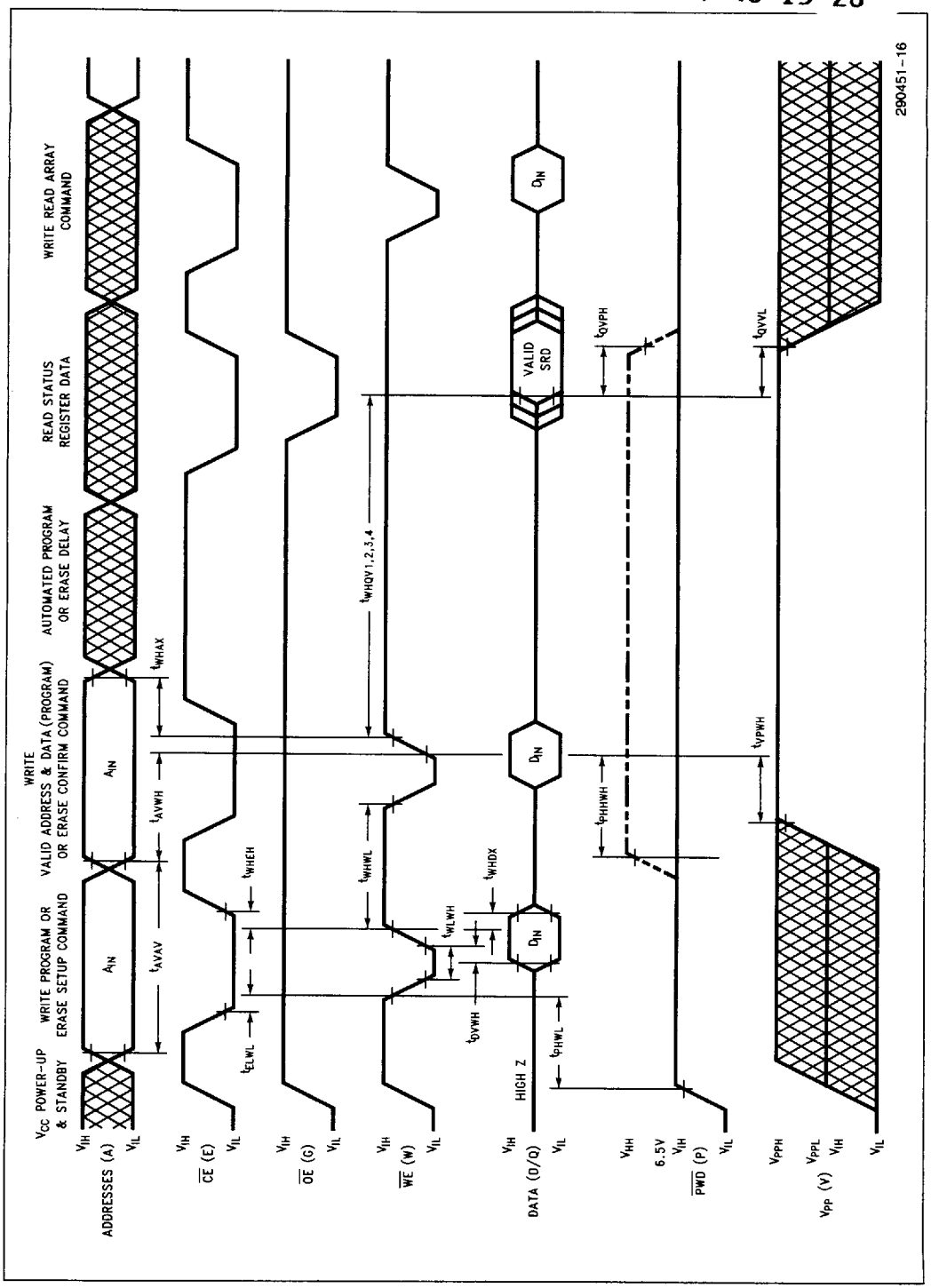


Figure 21. AC Waveforms for a Write and Erase Operations (WE-Controlled Writes)

AC CHARACTERISTICS—$\overline{CE}$-CONTROLLED WRITE OPERATIONS(1, 9)

Versions		$V_{CC} \pm 5\%$		28F400BX-60(10) 28F004BX-60(10)						Unit
		$V_{CC} \pm 10\%$				28F400BX-60(11) 28F004BX-60(11)		28F400BX-80(11) 28F004BX-80(11)		
Symbol		Parameter	Notes	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		60		70		80		ns
t_{PHEL}	t_{PS}	$\overline{PWD}$ High Recovery to $\overline{CE}$ Going Low		215		215		215		ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0		0		0		ns
t_{PHHEH}	t_{PHS}	$\overline{PWD}$ V_{HH} Setup to $\overline{CE}$ Going High	6, 8	100		100		100		ns
t_{VPEH}	t_{VPS}	V_{PP} Setup to $\overline{CE}$ Going High	5, 8	100		100		100		ns
t_{AVEH}	t_{AS}	Address Setup to $\overline{CE}$ Going High	3	50		50		50		ns
t_{DVEH}	t_{DS}	Data Setup to $\overline{CE}$ Going High	4	50		50		50		ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		50		50		50		ns
t_{EHDX}	t_{DH}	Data Hold from $\overline{CE}$ High	4	0		0		0		ns
t_{EHAX}	t_{AH}	Address Hold from $\overline{CE}$ High	3	10		10		10		ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold from $\overline{CE}$ High		10		10		10		ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		10		20		30		ns
t_{EHQV1}		Duration of Word/ Byte Programming Operation	2, 5	6		6		6		μs
t_{EHQV2}		Duration of Erase Operation (Boot)	2, 5, 6	0.3		0.3		0.3		s
t_{EHQV3}		Duration of Erase Operation (Parameter)	2, 5	0.3		0.3		0.3		s
t_{EHQV4}		Duration of Erase Operation (Main)	2, 5	0.6		0.6		0.6		s
t_{QWL}	t_{VPH}	V_{PP} Hold from Valid SRD	5, 8	0		0		0		ns
t_{QVPH}	t_{PHH}	$\overline{PWD}$ V_{HH} Hold from Valid SRD	6, 8	0		0		0		ns
t_{PHBR}		Boot-Block Relock Delay	7		100		100		100	ns

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AC CHARACTERISTICS—$\overline{CE}$-CONTROLLED WRITE OPERATIONS(1, 9) (Continued)

NOTES:
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of $\overline{CE}$ and $\overline{WE}$ in systems where $\overline{CE}$ defines the write pulse-width (within a longer $\overline{WE}$ timing waveform), all set-up, hold and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.
2, 3, 4, 5, 6, 7, 8: Refer to AC Characteristics notes for $\overline{WE}$-Controlled Write Operations.
9. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC Characteristics during Read Mode.
10. See High Speed Test Configuration.
11. See Standard Test Configuration.

EXTENDED TEMPERATURE OPERATION
AC CHARACTERISTICS—$\overline{CE}$-CONTROLLED WRITE OPERATIONS(1, 9)

Versions				T28F400BX-90(10) T28F004BX-90(10)		Unit
Symbol		Parameter	Notes	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		90		ns
t_{PHEL}	t_{PS}	$\overline{PWD}$ High Recovery to $\overline{CE}$ Going Low		210		ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0		ns
t_{PHHEH}	t_{PHS}	$\overline{PWD}$ V_{HH} Setup to $\overline{CE}$ Going High	6, 8	100		ns
t_{VPEH}	t_{VPS}	V_{PP} Setup to $\overline{CE}$ Going High	5, 8	100		ns
t_{AVEH}	t_{AS}	Address Setup to $\overline{CE}$ Going High	3	60		ns
t_{DVEH}	t_{DS}	Data Setup to $\overline{CE}$ Going High	4	60		ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		60		ns
t_{EHDX}	t_{DH}	Data Hold from $\overline{CE}$ High	4	0		ns
t_{EHAX}	t_{AH}	Address Hold from $\overline{CE}$ High	3	10		ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold from $\overline{CE}$ High		10		ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		30		ns
t_{EHQV1}		Duration of Word/Byte Programming Operation	2, 5	7		μs
t_{EHQV2}		Duration of Erase Operation (Boot)	2, 5, 6	0.4		s
t_{EHQV3}		Duration of Erase Operation (Parameter)	2, 5	0.4		s
t_{EHQV4}		Duration of Erase Operation (Main)	2, 5	0.7		s
t_{QWL}	t_{VPH}	V_{PP} Hold from Valid SRD	5, 8	0		ns
t_{QVPH}	t_{PHH}	$\overline{PWD}$ V_{HH} Hold from Valid SRD	6, 8	0		ns
t_{PHBR}		Boot-Block Relock Delay	7		100	ns

NOTES:
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of $\overline{CE}$ and $\overline{WE}$ in systems where $\overline{CE}$ defines the write pulse-width (within a longer $\overline{WE}$ timing waveform), all set-up, hold and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.
2, 3, 4, 5, 6, 7, 8: Refer to AC Characteristics for $\overline{WE}$-Controlled Write Operations.
9. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC Characteristics during Read Mode.
10. See Standard Test Configuration.

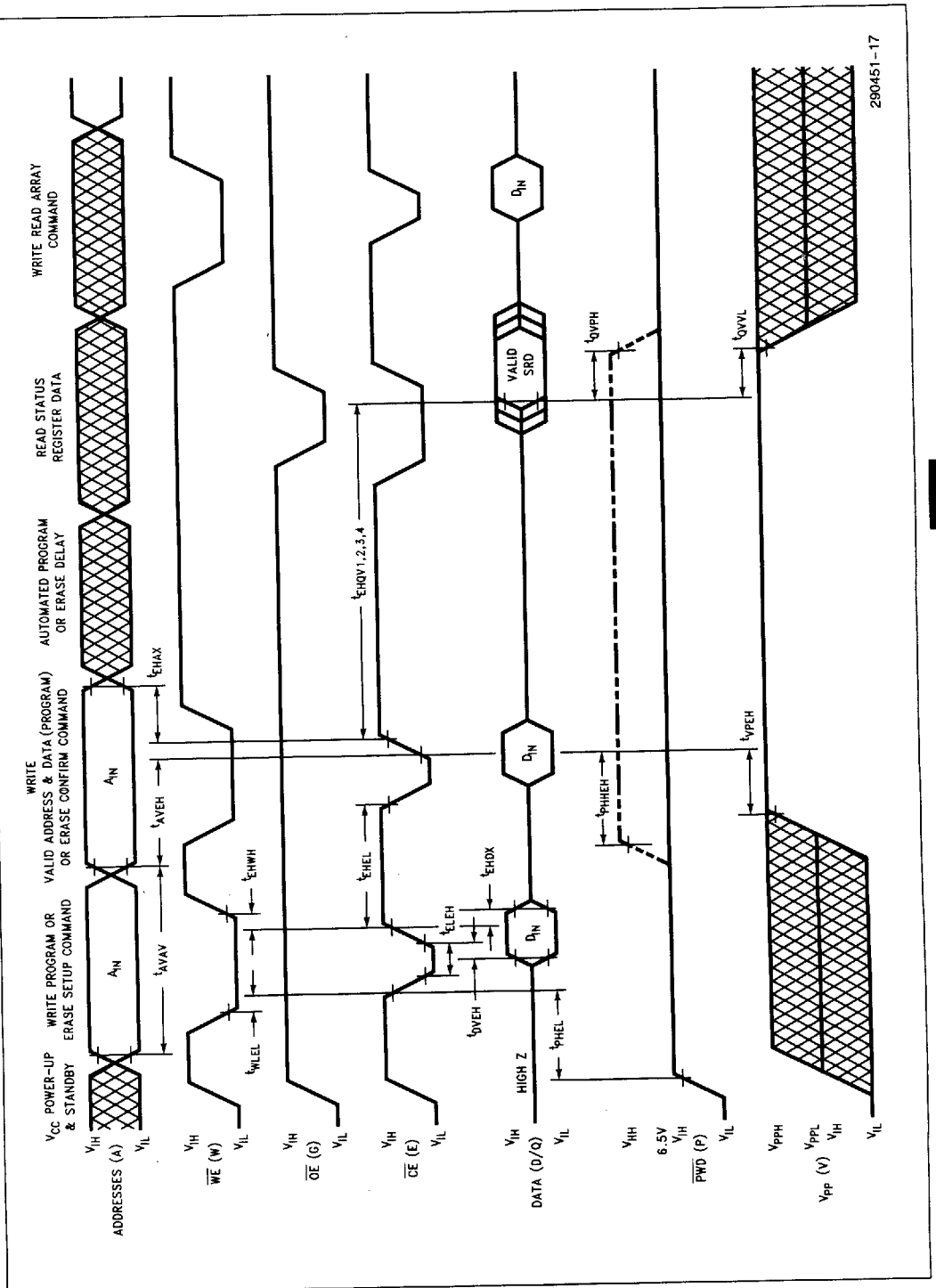
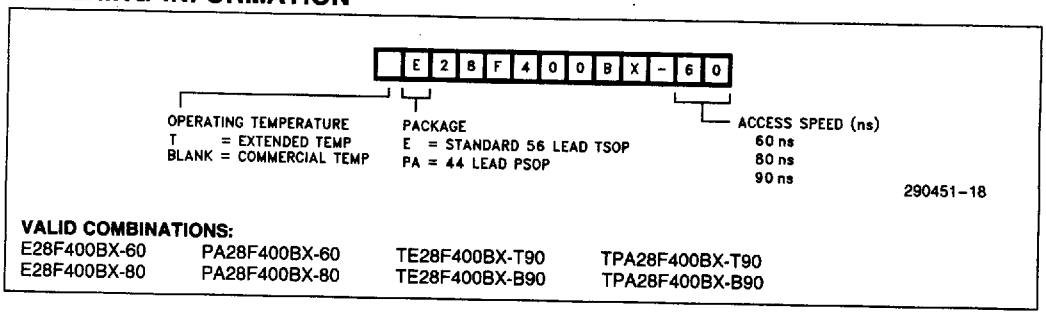


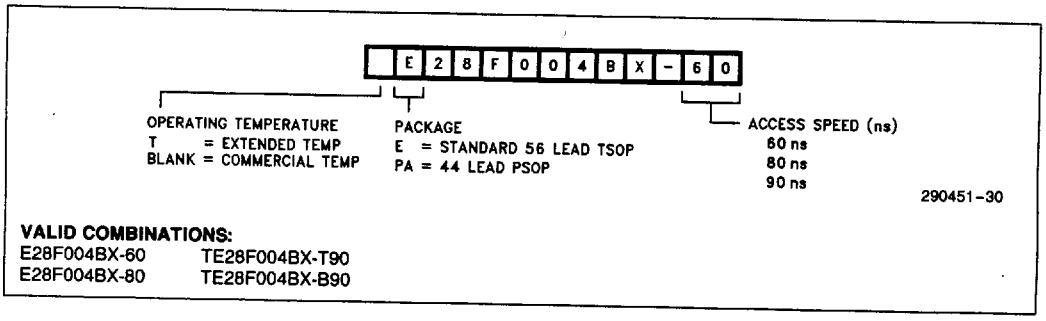
Figure 22. Alternate A.C. Waveforms for Write and Erase Operations ($\overline{CE}$-Controlled Writes)

ORDERING INFORMATION



VALID COMBINATIONS:

E28F400BX-60	PA28F400BX-60	TE28F400BX-T90	TPA28F400BX-T90
E28F400BX-80	PA28F400BX-80	TE28F400BX-B90	TPA28F400BX-B90



VALID COMBINATIONS:

E28F004BX-60	TE28F004BX-T90
E28F004BX-80	TE28F004BX-B90

ADDITIONAL INFORMATION

	Order Number
28F200BX/28F002BX Datasheet	290448
28F200BXL/28F002BXL Datasheet	290449
28F400BXL/28F004BXL Datasheet	290450
AP-363 "Extended Flash BIOS Design for Portable Computers"	292098
ER-28 "ETOX-III Flash Memory Technology"	204012
ER-29 "The Intel 2/4-MBit Boot Block Flash Memory Family"	294013

REVISION HISTORY

Number	Description
-001	Original Version
-002	Removed -70 speed bin. Integrated -70 characteristics into -60 speed bin. Added Extended Temperature characteristics. Modified $\overline{BYTE}$ Timing Diagram.