

HF/VHF power MOS transistor

BLF175

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the HF/VHF frequency range.

The transistor has a 4-lead, SOT123A flange package, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the handbook 'General' section for further information.

PIN CONFIGURATION

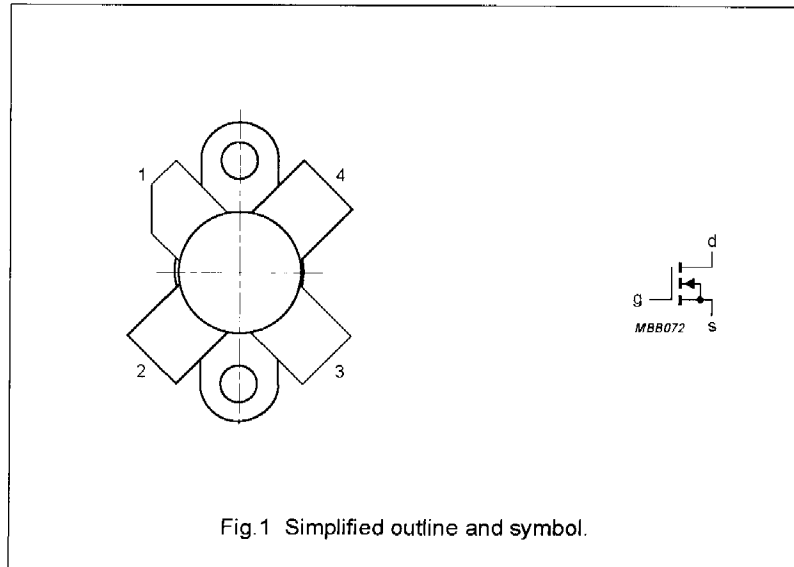


Fig.1 Simplified outline and symbol.

PINNING - SOT123A

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

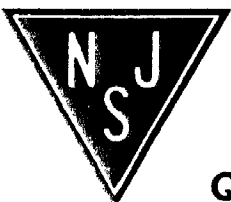
QUICK REFERENCE DATA

RF performance at $T_h = 25^\circ\text{C}$ in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)
class-A	28	50	800	8 (PEP)	>24	-	<-40
class-AB	28	50	150	30 (PEP)	typ. 24	typ. 40 ⁽¹⁾	typ. -35
CW, class-B	108	50	30	30	typ. 20	typ. 65	-

Note

1. 2-tone efficiency.



NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

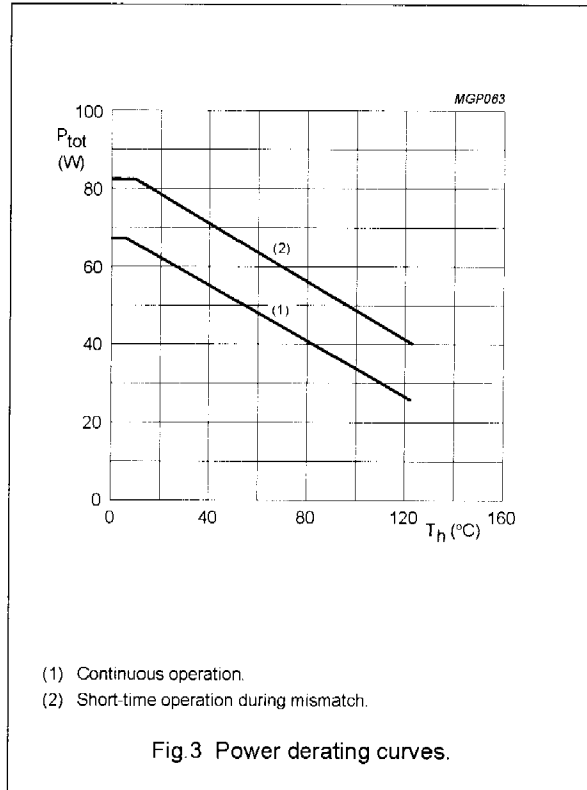
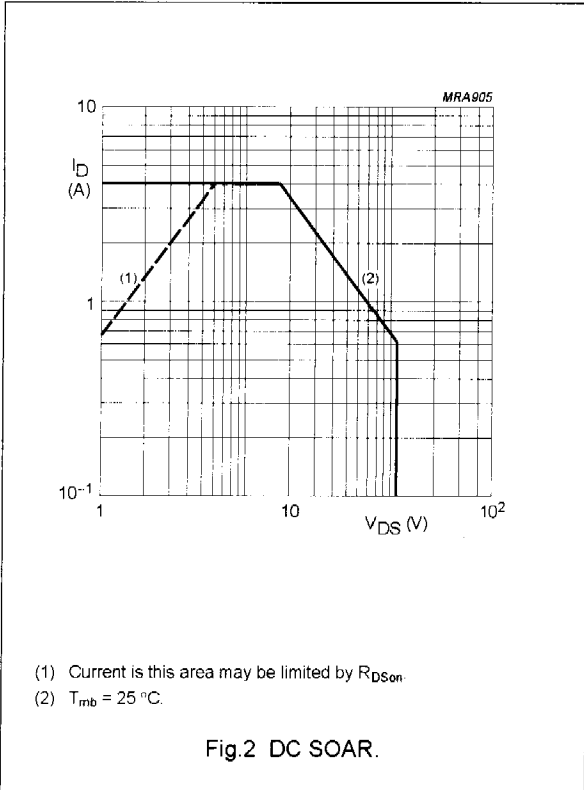
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	125	V
$\pm V_{GS}$	gate-source voltage		-	20	V
I_D	DC drain current		-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ }^\circ\text{C}$	-	68	W
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
T_J	junction temperature		-	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	$T_{mb} = 25\text{ }^\circ\text{C}; P_{tot} = 68\text{ W}$	2.6	K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	$T_{mb} = 25\text{ }^\circ\text{C}; P_{tot} = 68\text{ W}$	0.3	K/W



CHARACTERISTICST_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 100 mA; V _{GS} = 0	125	–	–	V
I _{DSS}	drain-source leakage current	V _{GS} = 0; V _{DS} = 50 V	–	–	100	μA
I _{GSS}	gate-source leakage current	±V _{GS} = 20 V; V _{DS} = 0	–	–	1	μA
V _{GStH}	gate-source threshold voltage	I _D = 10 mA; V _{DS} = 10 V	2	–	4.5	V
ΔV _{GS}	gate-source voltage difference of matched pairs	I _D = 10 mA; V _{DS} = 10 V	–	–	100	mV
g _{fs}	forward transconductance	I _D = 1 A; V _{DS} = 10 V	1.1	1.6	–	S
R _{DSon}	drain-source on-state resistance	I _D = 1 A; V _{GS} = 10 V	–	0.75	1.5	Ω
I _{DSX}	on-state drain current	V _{GS} = 10 V; V _{DS} = 10 V	–	5.5	–	A
C _{is}	input capacitance	V _{GS} = 0; V _{DS} = 50 V; f = 1 MHz	–	130	–	pF
C _{os}	output capacitance	V _{GS} = 0; V _{DS} = 50 V; f = 1 MHz	–	36	–	pF
C _{rs}	feedback capacitance	V _{GS} = 0; V _{DS} = 50 V; f = 1 MHz	–	3.7	–	pF

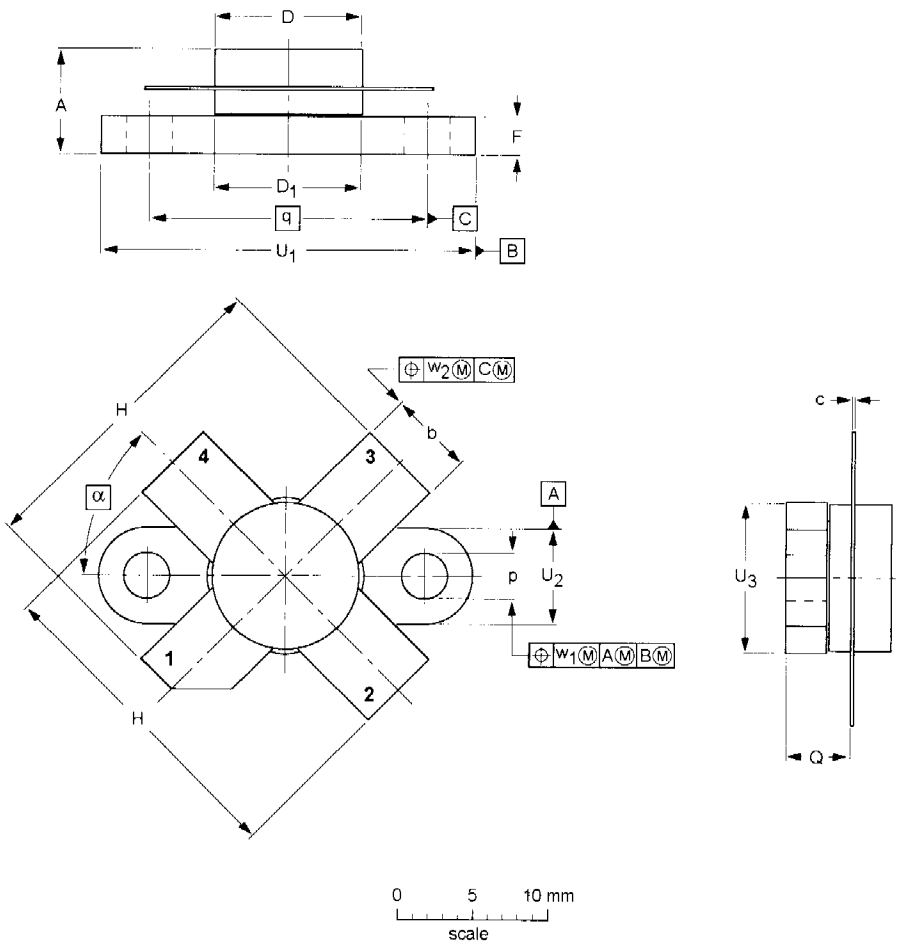
V_{GS} group indication

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads

SOT123A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	F	H	p	Q	q	U ₁	U ₂	U ₃	w ₁	w ₂	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.78 9.42	2.72 2.31	20.71 19.93	3.33 3.04	4.63 4.11	18.42	24.87 24.64	6.48 6.22	9.78 9.39	0.25	0.51	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.385 0.371	0.107 0.091	0.815 0.785	0.131 0.120	0.182 0.162	0.725	0.980 0.970	0.255 0.245	0.385 0.370	0.010	0.020	

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT123A					99-03-29