

Silicon NPN Power Transistors**2N6354****DESCRIPTION**

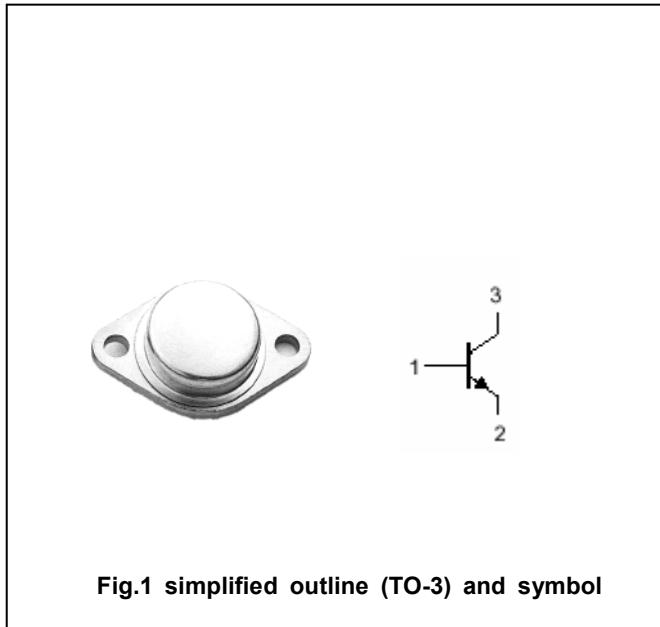
- With TO-3 package
- Excellent safe operating area
- Fast switching speed
- Low collector saturation voltage
- High power dissipation

APPLICATIONS

- For switching applications in military and industrial equipment

PINNING

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

**Absolute maximum ratings($T_a=25^\circ C$)**

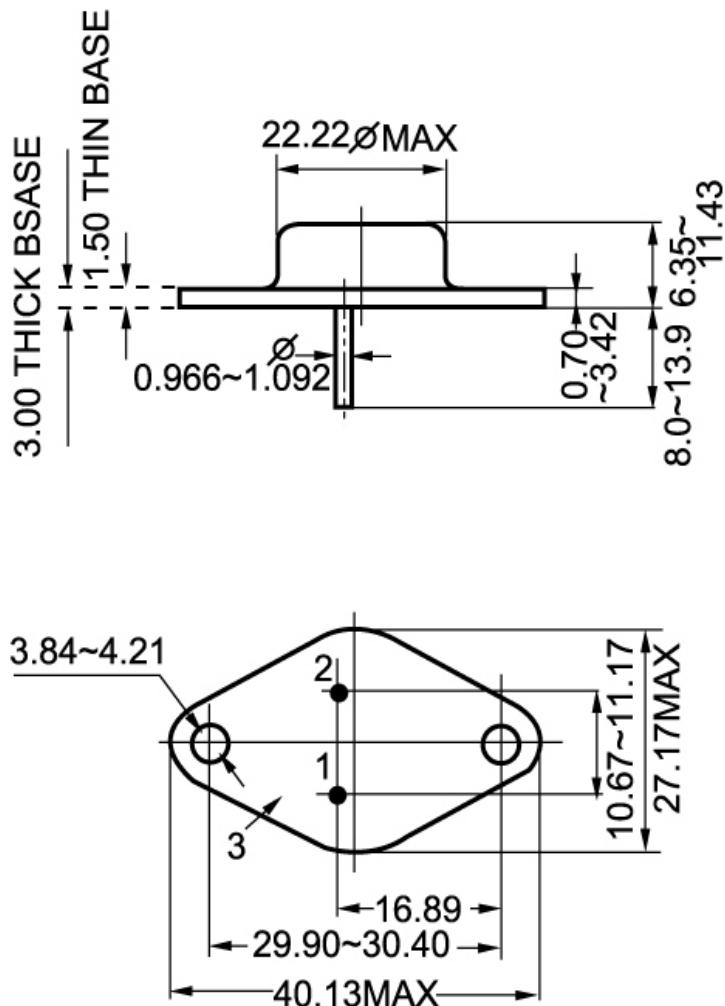
SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	150	V
V_{CEO}	Collector-emitter voltage	Open base	120	V
V_{EBO}	Emitter-base voltage	Open collector	6.5	V
I_C	Collector current		10	A
I_{CM}	Collector current-peak		12	A
I_B	Base current		5	A
P_D	Total Power Dissipation	$T_c=25^\circ C$	140	W
T_j	Junction temperature		200	$^\circ C$
T_{stg}	Storage temperature		-65~200	$^\circ C$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th j-c}$	Thermal resistance junction to case	1.25	$^\circ C/W$

Silicon NPN Power Transistors**2N6354****CHARACTERISTICS**T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =0.2A ; I _B =0	120			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =5mA ; I _C =0	6.5			V
V _{CEsat-1}	Collector-emitter saturation voltage	I _C =5A ; I _B =0.5A			0.5	V
V _{CEsat-2}	Collector-emitter saturation voltage	I _C =10A; I _B =1A			1.0	V
V _{BE sat-1}	Base-emitter saturation voltage	I _C =5A ; I _B =0.5A			1.3	V
V _{BE sat-2}	Base-emitter saturation voltage	I _C =10A; I _B =1A			2.0	V
I _{CEO}	Collector cut-off current	V _{CE} =100V; V _{BE} =0 T _C =125°C			10	mA
I _{CEV}	Collector cut-off current	V _{CE} =140V; I _B =0			10 20	mA
I _{CBO}	Collector cut-off current	V _{CB} =150V; I _E =0			5	mA
I _{EBO}	Emitter cut-off current	V _{EB} =5V; I _C =0			5	mA
h _{FE-1}	DC current gain	I _C =5A ; V _{CE} =2V	20		150	
h _{FE-2}	DC current gain	I _C =10A ; V _{CE} =2V	10		100	
C _{OB}	Output capacitance	I _E =0 ; V _{CB} =10V; f=1MHz			300	pF

Silicon NPN Power Transistors**2N6354****PACKAGE OUTLINE**Fig.2 outline dimensions (unindicated tolerance: $\pm 0.10\text{mm}$)