



ON Semiconductor®

# FDS4559

## 60V Complementary PowerTrench® MOSFET

### General Description

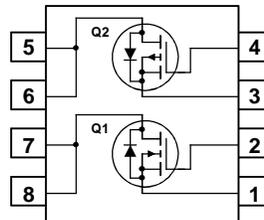
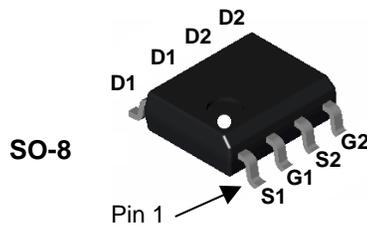
This complementary MOSFET device is produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

### Applications

- DC/DC converter
- Power management
- LCD backlight inverter

### Features

- **Q1: N-Channel**  
4.5 A, 60 V  $R_{DS(on)} = 55 \text{ m}\Omega @ V_{GS} = 10\text{V}$   
 $R_{DS(on)} = 75 \text{ m}\Omega @ V_{GS} = 4.5\text{V}$
- **Q2: P-Channel**  
-3.5 A, -60 V  $R_{DS(on)} = 105 \text{ m}\Omega @ V_{GS} = -10\text{V}$   
 $R_{DS(on)} = 135 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DSS}$	Drain-Source Voltage	60	-60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	4.5	-3.5	A
	- Pulsed	20	-20	
$P_D$	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1.2		
	(Note 1c)	1		
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175		$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4559	FDS4559	13"	12mm	2500 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

**Drain-Source Avalanche Ratings** (Note 1)

$W_{DSS}$	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30\text{ V}$ , $I_D = 4.5\text{ A}$	Q1			90	mJ
$I_{AR}$	Maximum Drain-Source Avalanche Current		Q1			4.5	A

**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$	Q1 Q2	60 -60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		58 -49		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}$ , $V_{GS} = 0\text{ V}$ $V_{DS} = -48\text{ V}$ , $V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$ $V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$	Q1 Q2	1 -1	2.2 -1.6	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		-5.5 4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4.5\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 4.5\text{ A}$ , $T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 4\text{ A}$ $V_{GS} = -10\text{ V}$ , $I_D = -3.5\text{ A}$ $V_{GS} = -10\text{ V}$ , $I_D = -3.5\text{ A}$ , $T_J = 125^\circ\text{C}$ $V_{GS} = -4.5\text{ V}$ , $I_D = -3.1\text{ A}$	Q1 Q2		42 72 55 82 130 105	55 94 75 105 190 135	m $\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$ , $V_{DS} = 5\text{ V}$ $V_{GS} = -10\text{ V}$ , $V_{DS} = -5\text{ V}$	Q1 Q2	20 -20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 4.5\text{ A}$ $V_{DS} = -5\text{ V}$ , $I_D = -3.5\text{ A}$	Q1 Q2		14 9		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 25\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$	Q1 Q2		650 759		pF
$C_{oss}$	Output Capacitance	Q1 Q2	Q1 Q2		80 90		pF
$C_{riss}$	Reverse Transfer Capacitance	$V_{DS} = -30\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$	Q1 Q2		35 39		pF

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 30\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		11 7	20 14	ns
$t_r$	Turn-On Rise Time		Q1 Q2		8 10	18 20	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -30\text{ V}$ , $I_D = -1\text{ A}$ , $V_{GS} = -10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		19 19	35 34	ns
$t_f$	Turn-Off Fall Time		Q1 Q2		6 12	15 22	ns
$Q_g$	Total Gate Charge	Q1 $V_{DS} = 30\text{ V}$ , $I_D = 4.5\text{ A}$ , $V_{GS} = 10\text{ V}$	Q1 Q2		12.5 15	18 21	nC
$Q_{gs}$	Gate-Source Charge		Q1 Q2		2.4 2.5		nC
$Q_{gd}$	Gate-Drain Charge	$V_{DS} = -30\text{ V}$ , $I_D = -3.5\text{ A}$ , $V_{GS} = -10\text{ V}$	Q1 Q2		2.6 3.0		nC

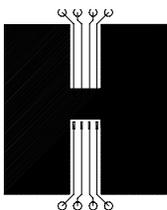
**Electrical Characteristics (continued)**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		Q1			1.3	A
			Q2			-1.3	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	Q1		0.8	1.2	V
			Q2		-0.8	-1.2	

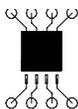
**Drain-Source Diode Characteristics and Maximum Ratings**

**Notes:**

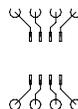
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $78^\circ\text{C/W}$  when mounted on a  $0.5\text{ in}^2$  pad of 2 oz copper



b)  $125^\circ\text{C/W}$  when mounted on a  $.02\text{ in}^2$  pad of 2 oz copper

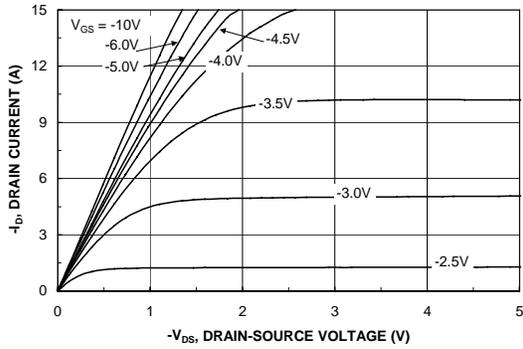


c)  $135^\circ\text{C/W}$  when mounted on a minimum pad.

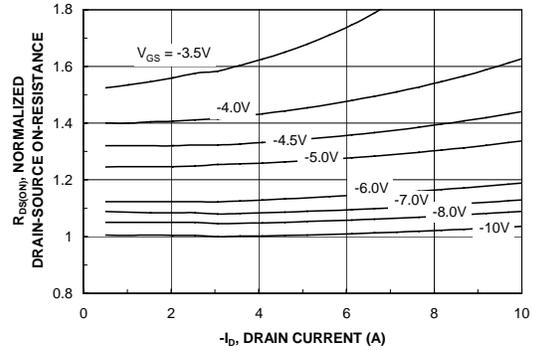
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty Cycle  $< 2.0\%$

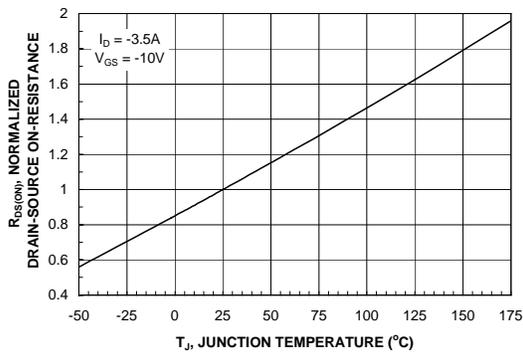
### Typical Characteristics: Q2



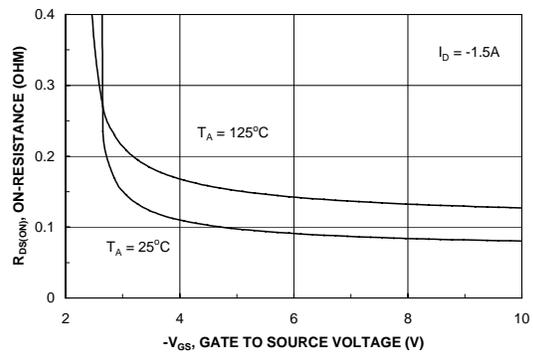
**Figure 1. On-Region Characteristics.**



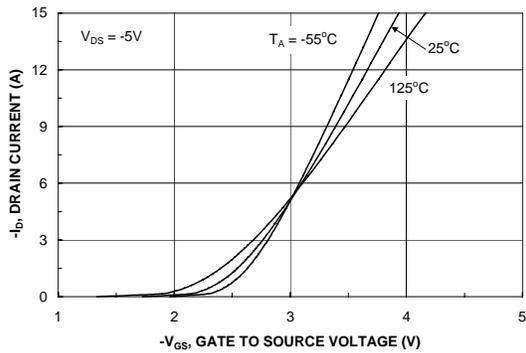
**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**



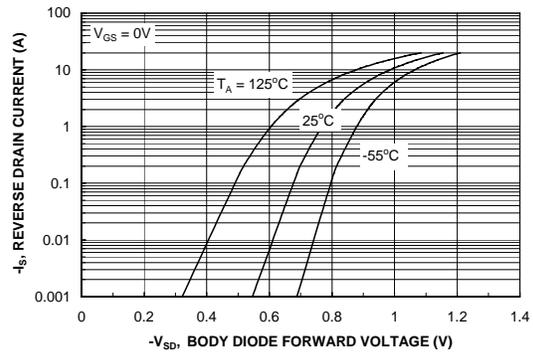
**Figure 3. On-Resistance Variation with Temperature.**



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**



**Figure 5. Transfer Characteristics.**



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

Typical Characteristics: Q2

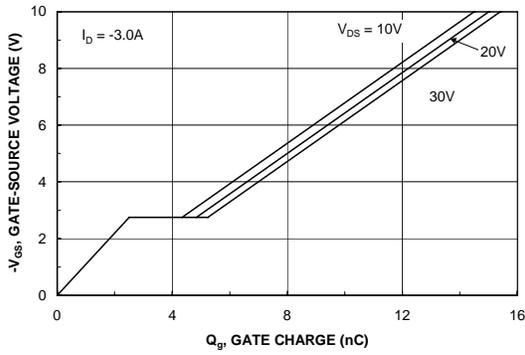


Figure 7. Gate Charge Characteristics.

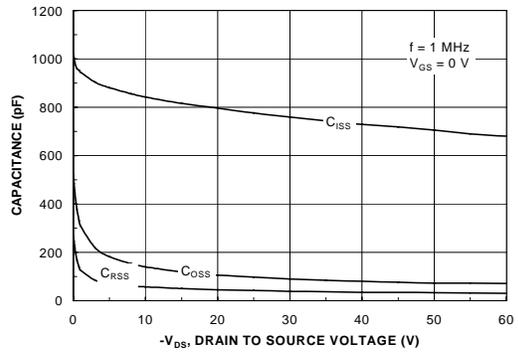


Figure 8. Capacitance Characteristics.

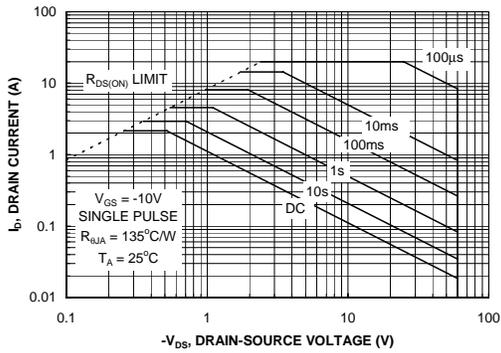


Figure 9. Maximum Safe Operating Area.

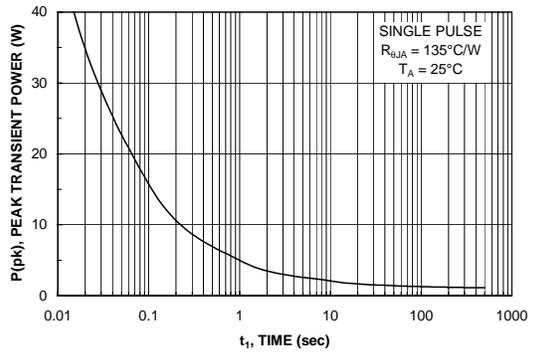


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1

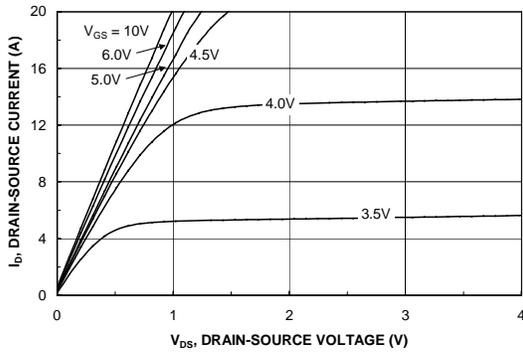


Figure 11. On-Region Characteristics.

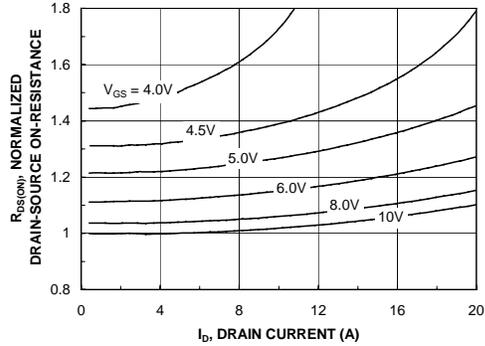


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

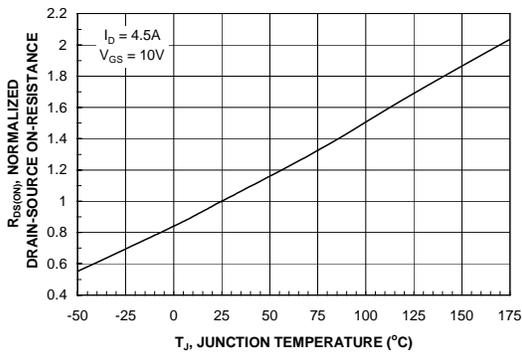


Figure 13. On-Resistance Variation with Temperature.

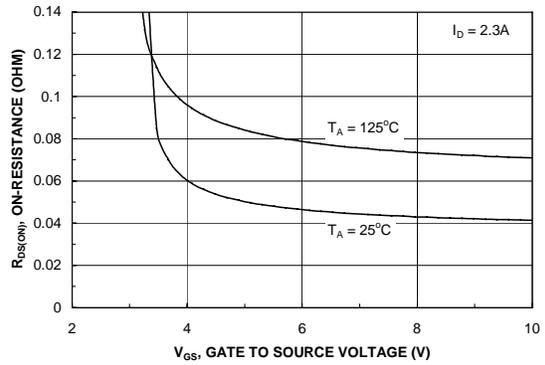


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

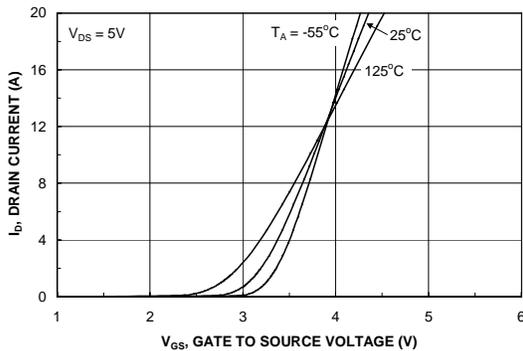


Figure 15. Transfer Characteristics.

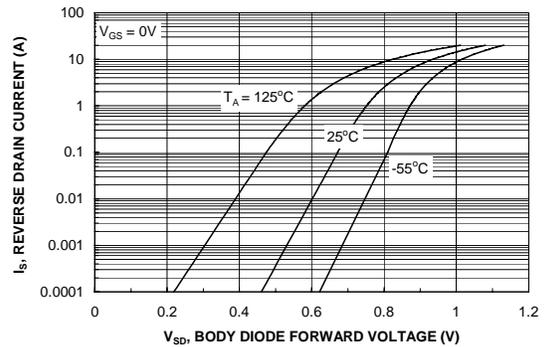


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1

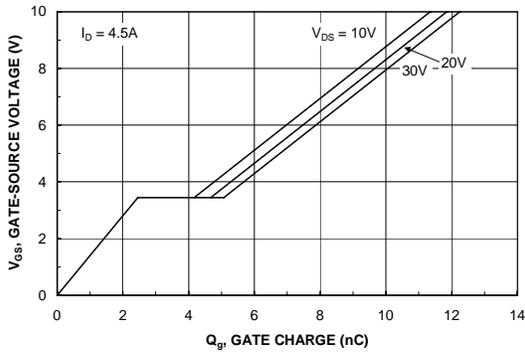


Figure 17. Gate Charge Characteristics.

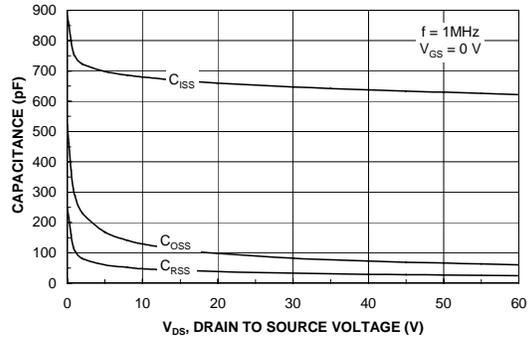


Figure 18. Capacitance Characteristics.

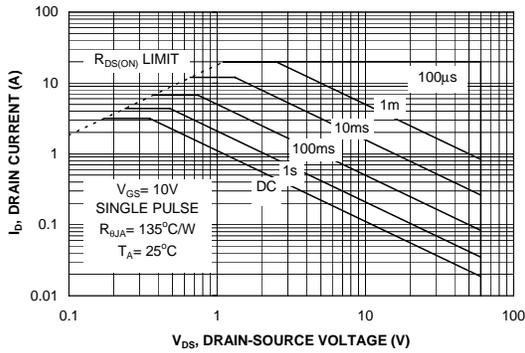


Figure 19. Maximum Safe Operating Area.

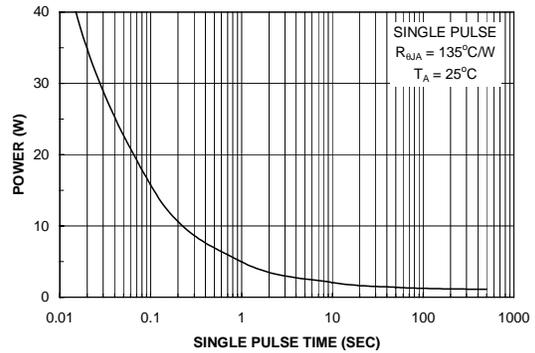


Figure 20. Single Pulse Maximum Power Dissipation.

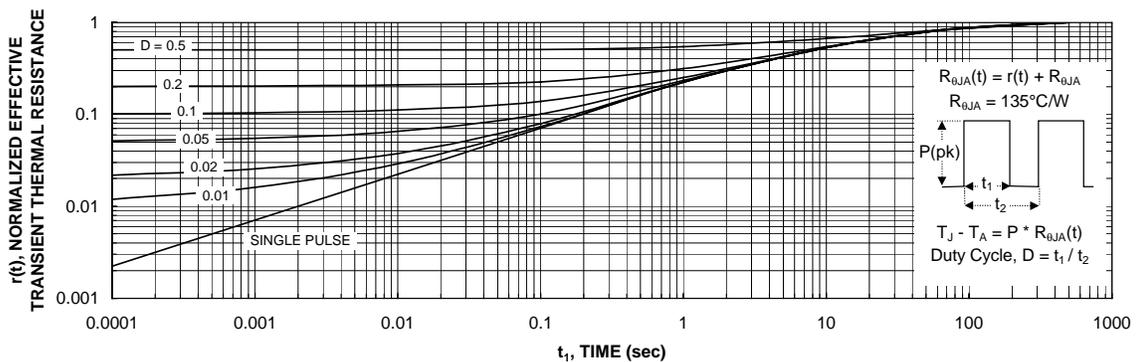


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative