PD - 94084B

International
IOR Rectifier

SMPS MOSFET

IRFB17N50L

HEXFET® Power MOSFET

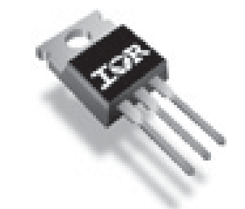
Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications

V_{DSS}	$R_{DS(on)}$ typ.	I_D
500V	**0.28Ω**	**16A**

Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.

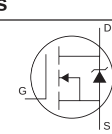


TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	16	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	11	
I_{DM}	Pulsed Drain Current ①	64	
P_D @T_C = 25°C	Power Dissipation	220	W
	Linear Derating Factor	1.8	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	10	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 screw	10	lbf.in(N.m)

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	16	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	64		
V_{SD}	Diode Forward Voltage	——	——	1.5	V	T_J = 25°C, I_S = 16A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	170	250	ns	T_J = 25°C I_F = 16A
		——	220	330		T_J = 125°C di/dt = 100A/μs ④
Q_{rr}	Reverse Recovery Charge	——	470	710	nC	T_J = 25°C
		——	810	1210		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	7.3	11	A	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

1/5/05

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.6	——	V/°C	Reference to 25°C, I_D = 1mA ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	0.28	0.32	Ω	V_{GS} = 10V, I_D = 9.9A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	——	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	50	µA	V_{DS} = 500V, V_{GS} = 0V
		——	——	2.0	mA	V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -30V
R_G	Internal Gate Resistance	——	0.77	——	Ω	f = 1MHz, open drain

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	11	——	——	S	V_{DS} = 50V, I_D = 9.9A
Q_g	Total Gate Charge	——	——	130	nC	I_D = 16A
Q_{gs}	Gate-to-Source Charge	——	——	33		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	59		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	——	21	——	ns	V_{DD} = 250V
t_r	Rise Time	——	51	——		I_D = 16A
$t_{d(off)}$	Turn-Off Delay Time	——	50	——		R_G = 7.5Ω
t_f	Fall Time	——	28	——		V_{GS} = 10V ④
C_{iss}	Input Capacitance	——	2760	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	325	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	37	——		ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	3690	——		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	84	——		V_{GS} = 0V, V_{DS} = 400V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	200	——		V_{GS} = 0V, V_{DS} = 0V to 400V ⑤

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	390	mJ
I_{AR}	Avalanche Current①	——	16	A
E_{AR}	Repetitive Avalanche Energy①	——	22	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case⑥	——	0.56	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient⑥	——	62	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 3.0mH, R_G = 25Ω, I_{AS} = 16A.

③ $I_{SD} \leq$ 16A, di/dt ≤ 520A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
C_{oss} eff.(ER) is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ R_θ is measured at T_J approximately 90°C

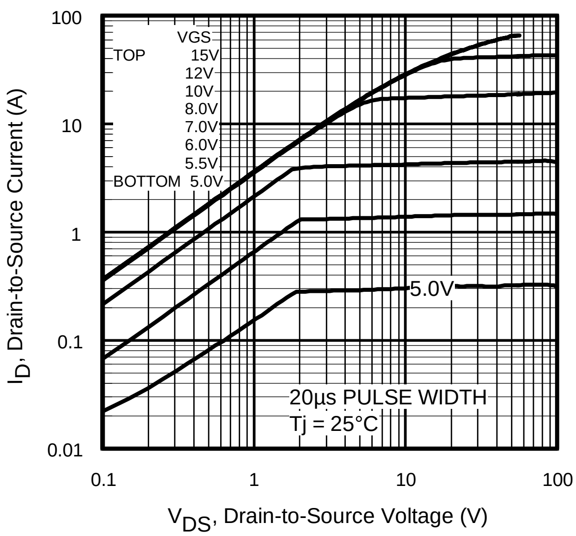


Fig 1. Typical Output Characteristics

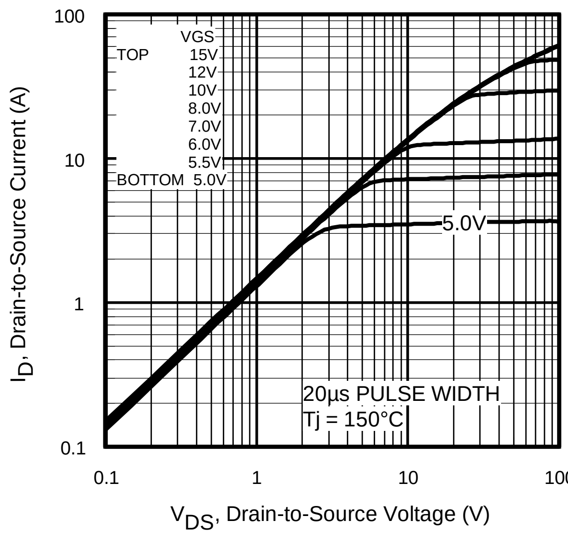


Fig 2. Typical Output Characteristics

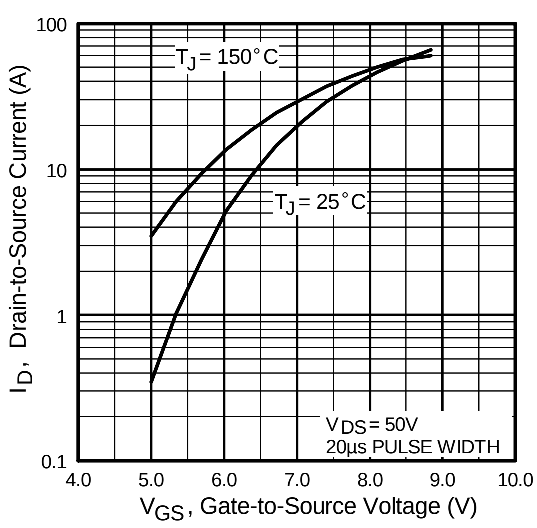


Fig 3. Typical Transfer Characteristics

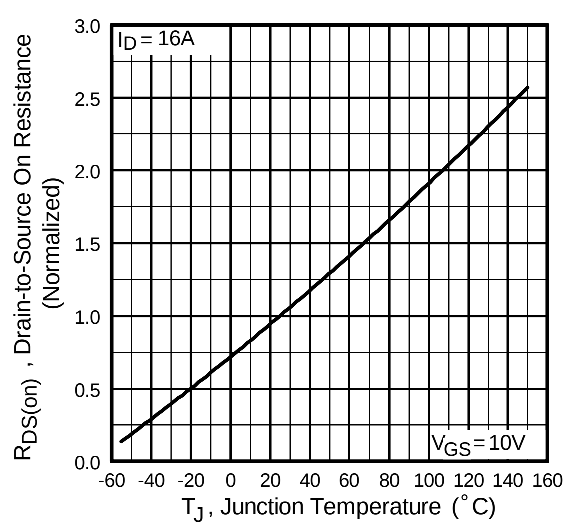


Fig 4. Normalized On-Resistance vs. Temperature

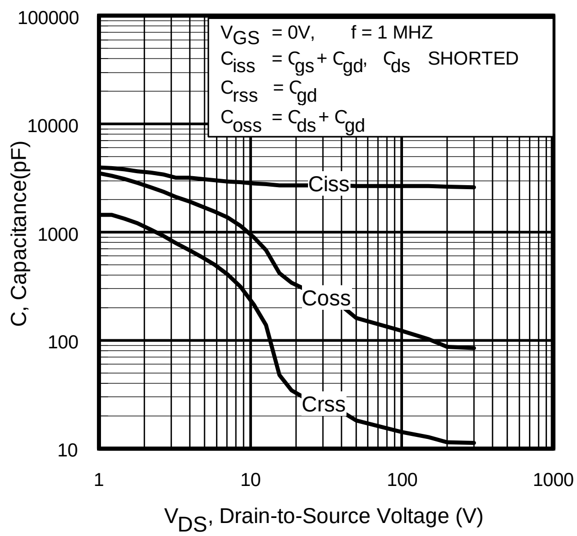


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

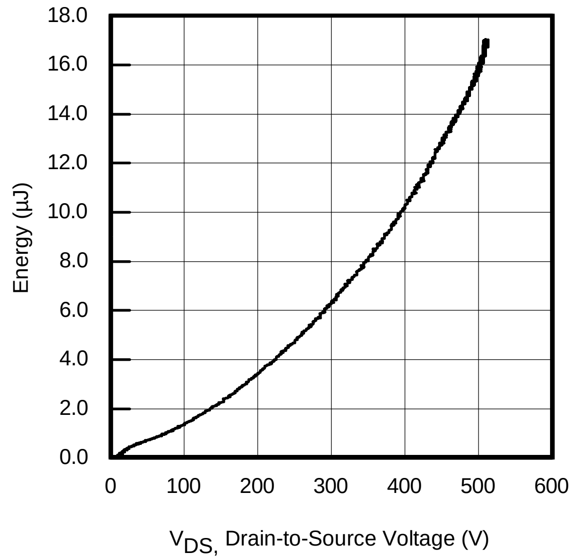


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

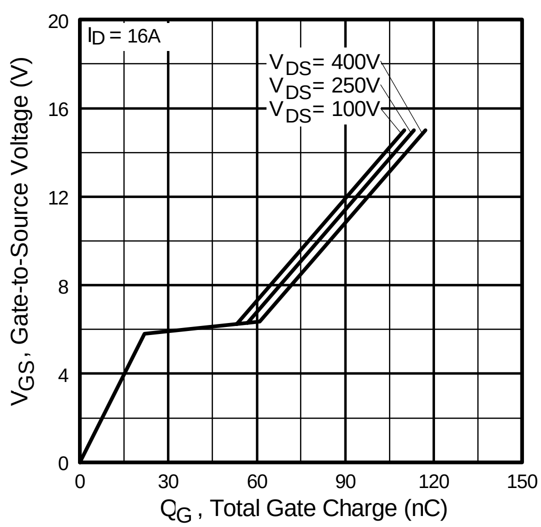


Fig 7. Typical Gate Charge vs. Gate-to-Source Voltage

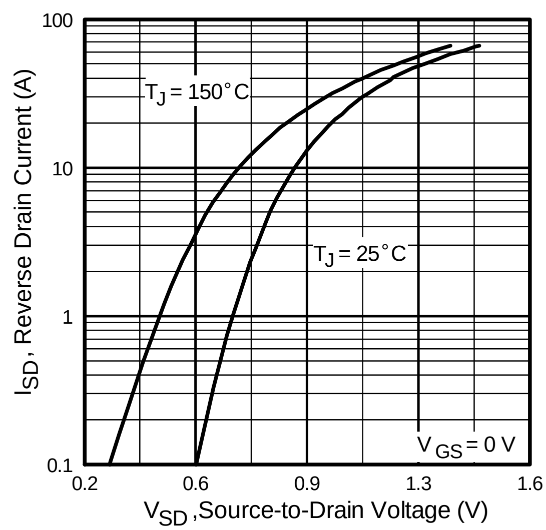


Fig 8. Typical Source-Drain Diode Forward Voltage

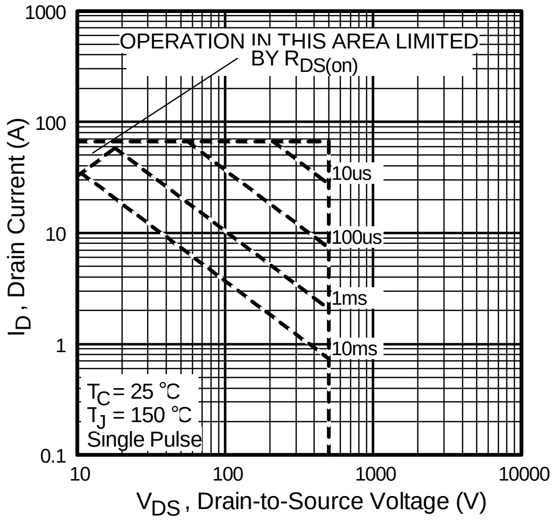


Fig 9. Maximum Safe Operating Area

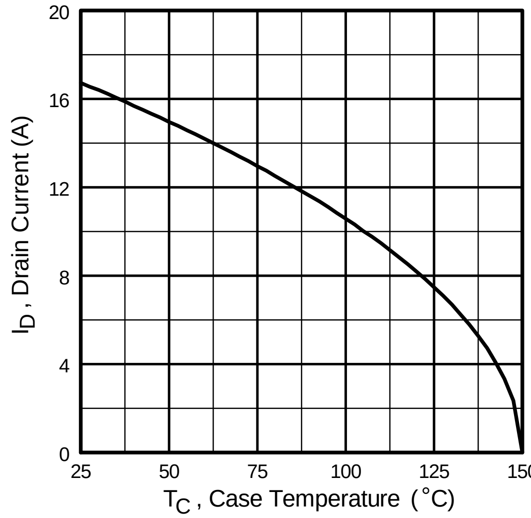


Fig 10. Maximum Drain Current vs. Case Temperature

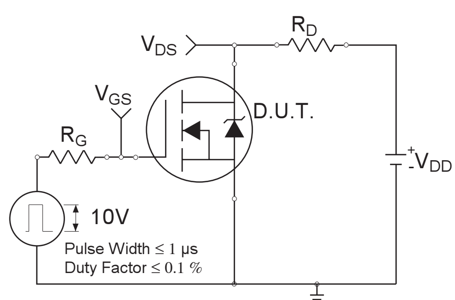


Fig 11a. Switching Time Test Circuit

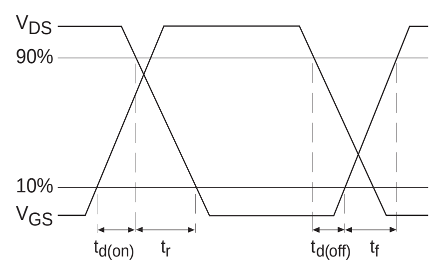


Fig 11b. Switching Time Waveforms

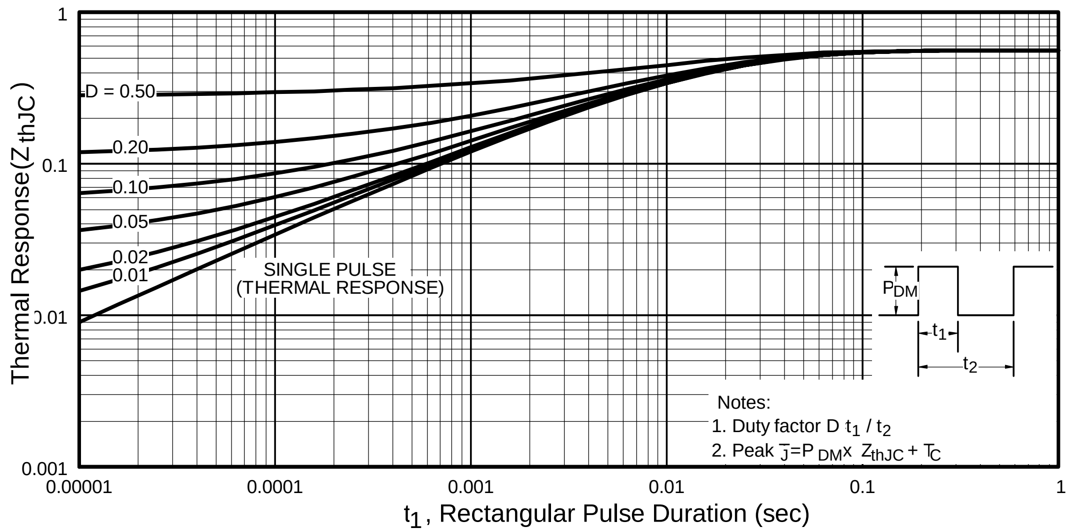


Fig 12. Maximum Effective Transient Thermal Impedance, Junction-to-

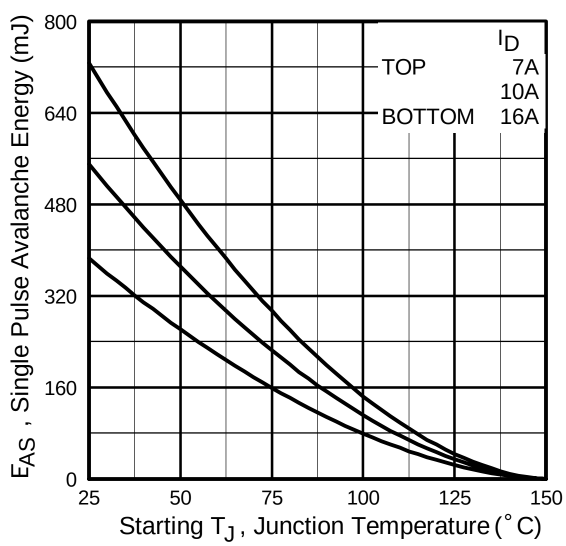


Fig 13. Maximum Avalanche Energy
vs. Drain Current

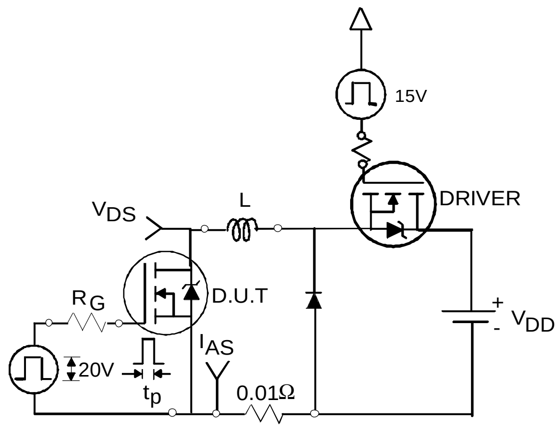


Fig 14. Unclamped Inductive Test Circuit

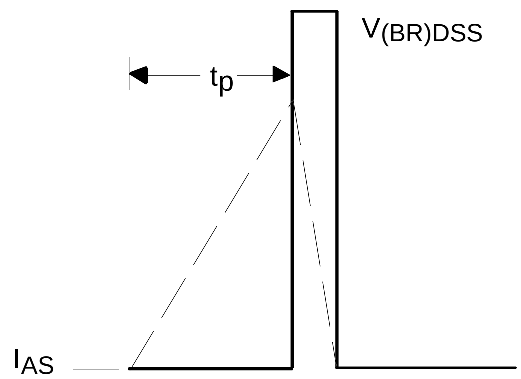


Fig 15. Unclamped Inductive Waveforms

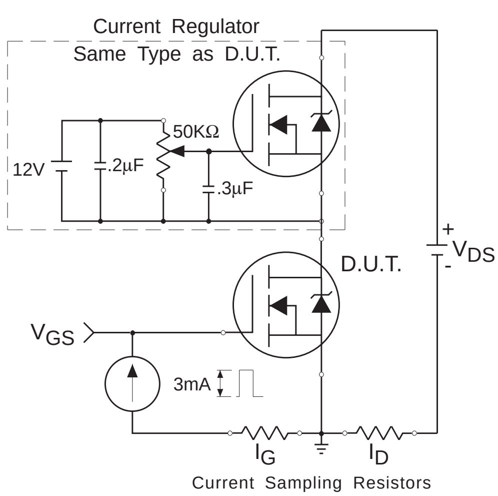


Fig 16. Gate Charge Test Circuit

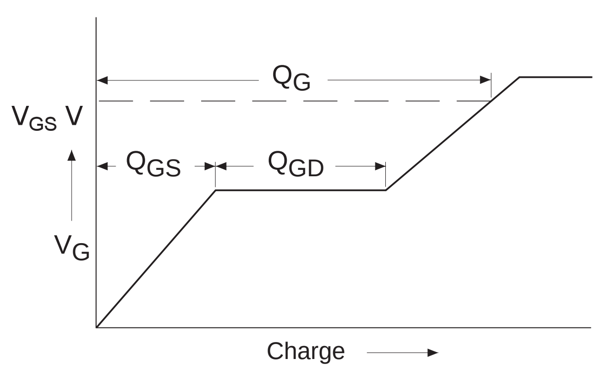
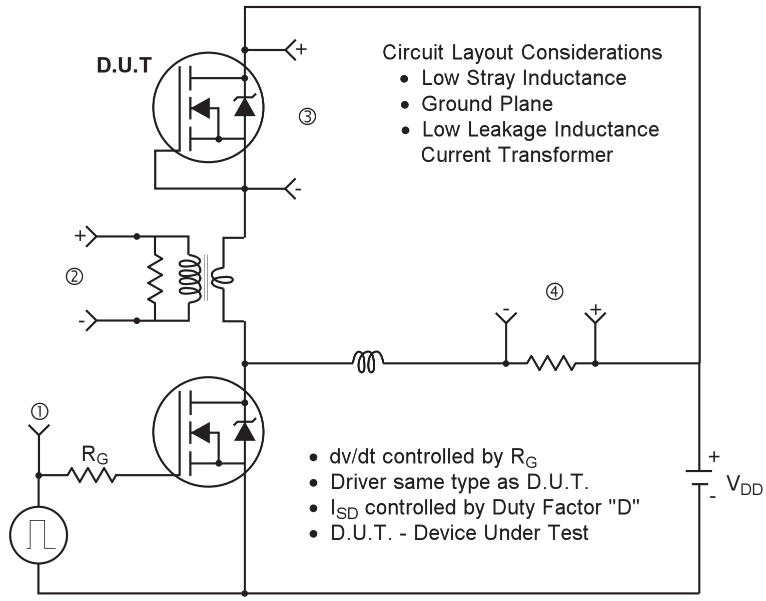
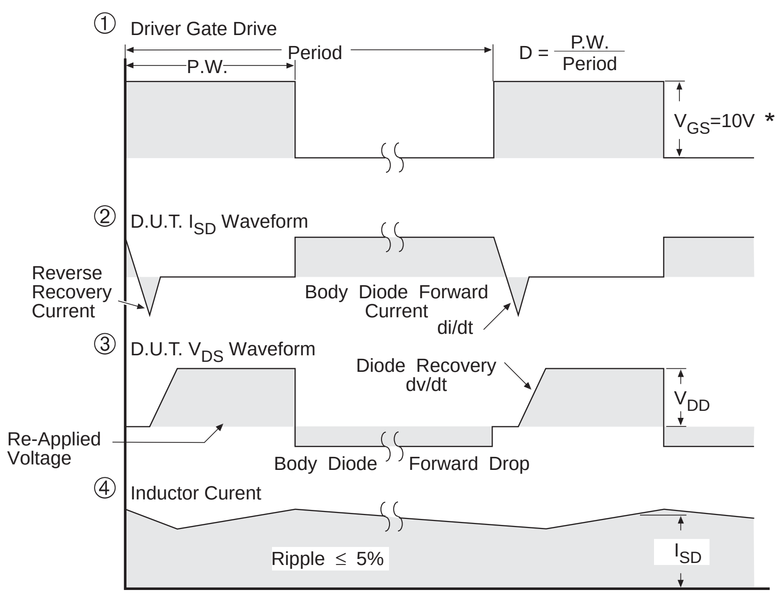


Fig 17. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



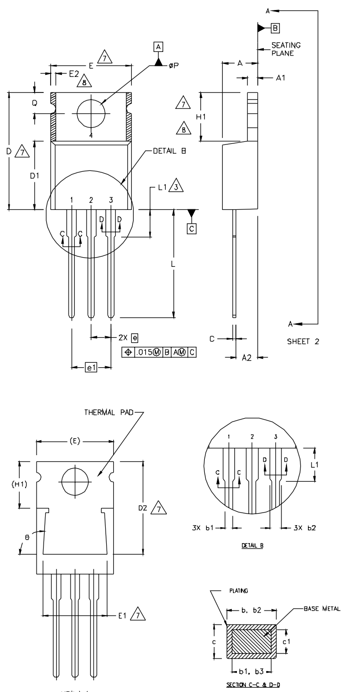


* V_{GS} = 5V for Logic Level Devices

Fig 18. For N-Channel HEXFET® Power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3. LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION : INCHES.
7. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8. DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	–	6.35	–	.250	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
ø	90°–93°		90°–93°		

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE

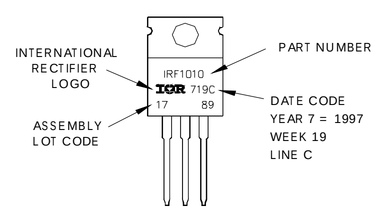
IGBTs, CoPACK
1.– GATE
2.– COLLECTOR
3.– EMITTER

DIODES
1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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