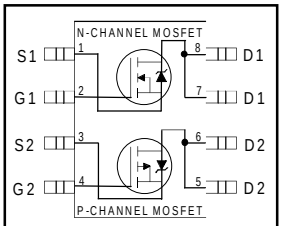
International
IOR Rectifier

PD - 94226B

# IRF7350

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Surface Mount
- Available in Tape and Reel



Top View

| | N-Ch | P-Ch |
|---|---|---|
| $V_{DSS}$ | 100V | -100V |
| $R_{DS(on)}$ | 0.21Ω | 0.48Ω |

## Description

These dual N and P channel HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET® power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in DC motor drives and load management applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques.


SO-8

## Absolute Maximum Ratings

| | Parameter | Max. | | Units |
|---|---|---|---|---|
| | | N-Channel | P-Channel | |
| $V_{DS}$ | Drain-to-Source Voltage | 100 | -100 | A |
| $I_D$ @ $T_A$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 2.1 | -1.5 | |
| $I_D$ @ $T_A$ = 70°C | Continuous Drain Current, $V_{GS}$ @ 10V | 1.7 | -1.2 | |
| $I_{DM}$ | Pulsed Drain Current ① | 8.4 | -6.0 | |
| $P_D$ @$T_A$ = 25°C | Power Dissipation | 2.0 | | W |
| | Linear Derating Factor | 0.016 | | W/°C |
| $E_{AS}$ | Single Pulse Avalanche Energy④ | 35 | 51 | mJ |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | ± 20 | V |
| dv/dt | Peak Diode Recovery dv/dt ② | 4.0 | 4.3 | V/ns |
| $T_J$, $T_{STG}$ | Junction and Storage Temperature Range | -55 to + 150 | | °C |

## Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JL}$ | Junction-to-Drain Lead | — | 20 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient ③ | — | 62.5 | |



08/09/01

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | N-Ch | 100 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| | | P-Ch | -100 | — | — | | $V_{GS}$ = 0V, $I_D$ = -250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | N-Ch | — | 0.12 | — | V/°C | Reference to 25°C, $I_D$ = 1mA |
| | | P-Ch | — | -0.11 | — | | Reference to 25°C, $I_D$ = -1mA |
| $R_{DS(ON)}$ | Static Drain-to-Source On-Resistance | N-Ch | — | — | 0.21 | Ω | $V_{GS}$ = 10V, $I_D$ = 2.1A ② |
| | | P-Ch | — | — | 0.48 | | $V_{GS}$ = -10V, $I_D$ = -1.5A ② |
| $V_{GS(th)}$ | Gate Threshold Voltage | N-Ch | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| | | P-Ch | -2.0 | — | -4.0 | | $V_{DS}$ = $V_{GS}$, $I_D$ = -250µA |
| $g_{fs}$ | Forward Transconductance | N-Ch | 2.4 | — | — | S | $V_{DS}$ = 50V, $I_D$ = 2.1A |
| | | P-Ch | 1.1 | — | — | | $V_{DS}$ = -50V, $I_D$ = -1.5A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | N-Ch | — | — | 25 | µA | $V_{DS}$ = 100V, $V_{GS}$ = 0V ② |
| | | P-Ch | — | — | -25 | | $V_{DS}$ = -100V, $V_{GS}$ = 0V ② |
| | | N-Ch | — | — | 250 | | $V_{DS}$ = 80 V, $V_{GS}$ = 0V, $T_J$ = 70°C |
| | | P-Ch | — | — | -250 | | $V_{DS}$ = -80V, $V_{GS}$ = 0V, $T_J$ = 70°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | N-P | — | — | ±100 | | $V_{GS}$ = ± 20V |
| $Q_g$ | Total Gate Charge | N-Ch | — | 19 | 28 | nC | N-Channel<br>$I_D$ = 2.1A, $V_{DS}$ = 80V, $V_{GS}$ = 10V<br><br>P-Channel<br>$I_D$ = -1.5A, $V_{DS}$ = -80V, $V_{GS}$ = -10V |
| | | P-Ch | — | 21 | 31 | | |
| $Q_{gs}$ | Gate-to-Source Charge | N-Ch | — | 3.0 | 4.5 | | |
| | | P-Ch | — | 3.4 | 5.1 | | |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | N-Ch | — | 8.8 | 13 | | |
| | | P-Ch | — | 10 | 16 | | |
| $t_{d(on)}$ | Turn-On Delay Time | N-Ch | — | 6.7 | — | ns | N-Channel<br>$V_{DD}$ = 50V, $I_D$ = 1.0A, $R_G$ = 22Ω,<br>$R_D$ = 50Ω, $V_{GS}$ = 10V ②<br><br>P-Channel<br>$V_{DD}$ = -50V, $I_D$ = -1.0A, $R_G$ = 22Ω,<br>$R_D$ = 50Ω, $V_{GS}$ = -10V |
| | | P-Ch | — | 25 | — | | |
| $t_r$ | Rise Time | N-Ch | — | 11 | — | | |
| | | P-Ch | — | 13 | — | | |
| $t_{d(off)}$ | Turn-Off Delay Time | N-Ch | — | 35 | — | | |
| | | P-Ch | — | 30 | — | | |
| $t_f$ | Fall Time | N-Ch | — | 20 | — | | |
| | | P-Ch | — | 40 | — | | |
| $C_{iss}$ | Input Capacitance | N-Ch | — | 380 | — | pF | N-Channel<br>$V_{GS}$ = 0V, $V_{DS}$ = 25V, $f$ = 1.0MHz<br><br>P-Channel<br>$V_{GS}$ = 0V, $V_{DS}$ = -25V, $f$ = 1.0MHz |
| | | P-Ch | — | 360 | — | | |
| $C_{oss}$ | Output Capacitance | N-Ch | — | 100 | — | | |
| | | P-Ch | — | 110 | — | | |
| $C_{rss}$ | Reverse Transfer Capacitance | N-Ch | — | 54 | — | | |
| | | P-Ch | — | 65 | — | | |

## Source-Drain Ratings and Characteristics

| | Parameter | | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | N-Ch | — | — | 1.8 | A | |
| | | P-Ch | — | — | -1.4 | | |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | N-Ch | — | — | 8.4 | | |
| | | P-Ch | — | — | -6.0 | | |
| $V_{SD}$ | Diode Forward Voltage | N-Ch | — | — | 1.3 | V | $T_J$ = 25°C, $I_S$ = 1.8A, $V_{GS}$ = 0V ② |
| | | P-Ch | — | — | -1.6 | | $T_J$ = 25°C, $I_S$ = -1.4A, $V_{GS}$ = 0V ② |
| $t_{rr}$ | Reverse Recovery Time | N-Ch | — | 72 | 110 | ns | N-Channel<br>$T_J$ = 25°C, $I_F$ = 1.8A, di/dt = 100A/µs<br>P-Channel ②<br>$T_J$ = 25°C, $I_F$ = -1.4A, di/dt = -100A/µs |
| | | P-Ch | — | 77 | 120 | | |
| $Q_{rr}$ | Reverse Recovery Charge | N-Ch | — | 205 | 310 | nC | |
| | | P-Ch | — | 240 | 360 | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 400µs; duty cycle ≤ 2%.

③ Surface mounted on 1 in square Cu board

④ N channel: Starting $T_J$ = 25°C, L = 4.0mH, $R_G$ = 25Ω, $I_{AS}$ = 4.2A
P channel: Starting $T_J$ = 25°C, L = 11mH, $R_G$ = 25Ω, $I_{AS}$ = -3.0A

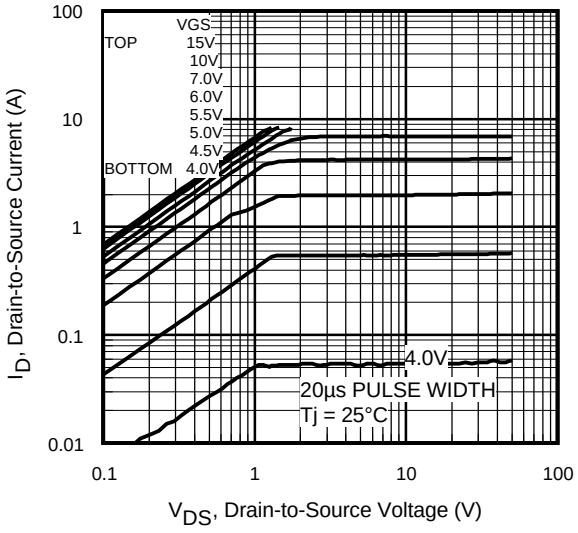



**Fig 1.** Typical Output Characteristics

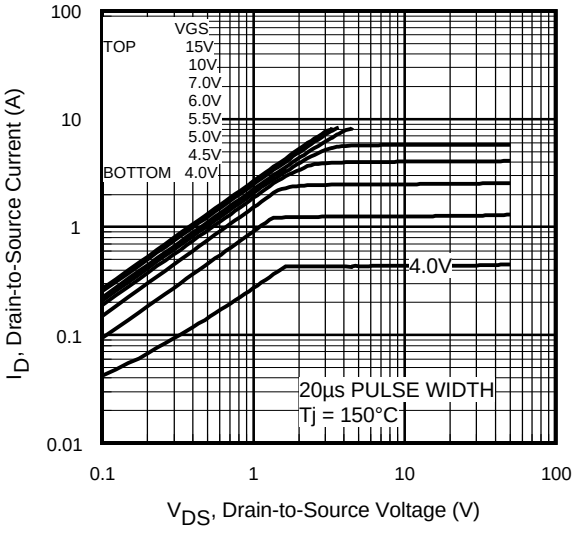



**Fig 2.** Typical Output Characteristics

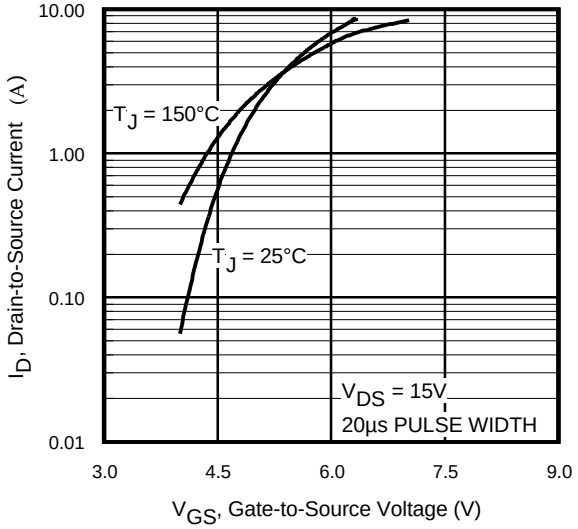



**Fig 3.** Typical Transfer Characteristics

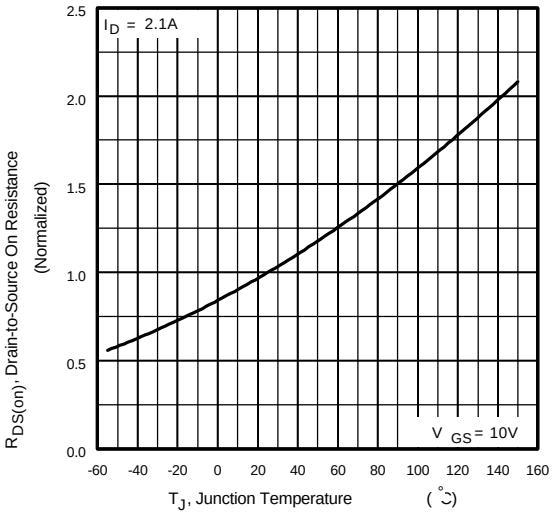



**Fig 4.** Normalized On-Resistance Vs. Temperature

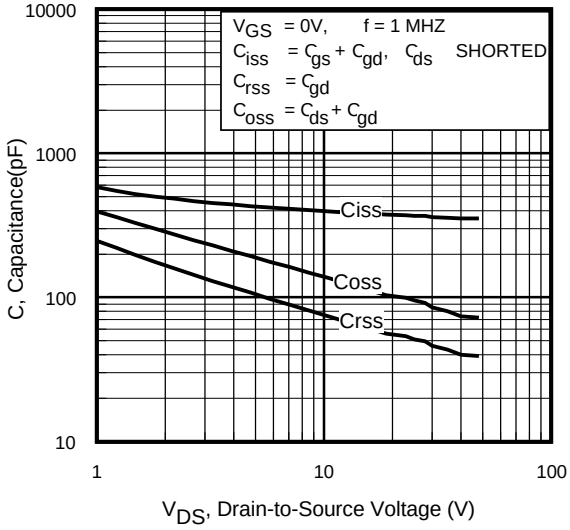



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

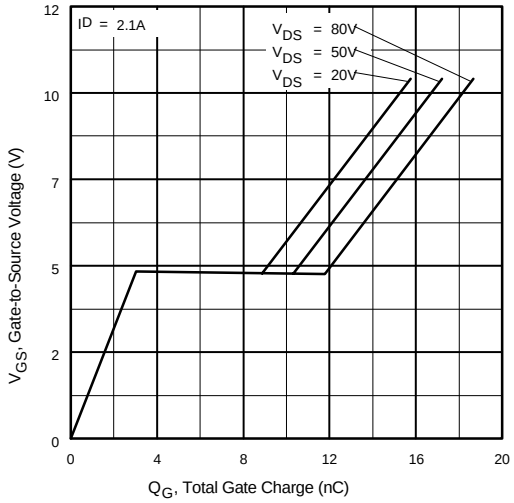



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

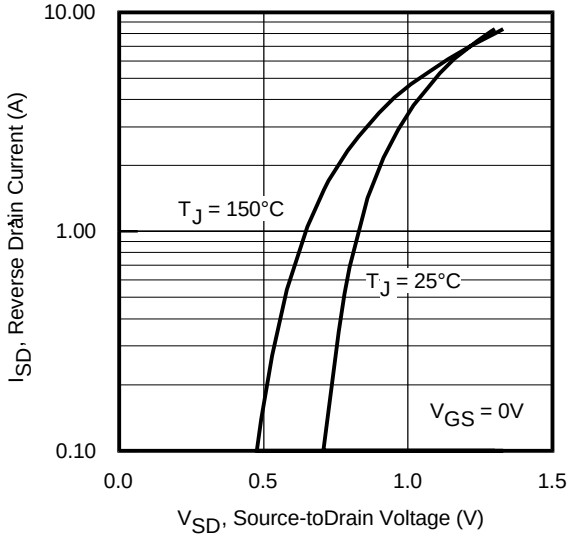



**Fig 7.** Typical Source-Drain Diode Forward Voltage

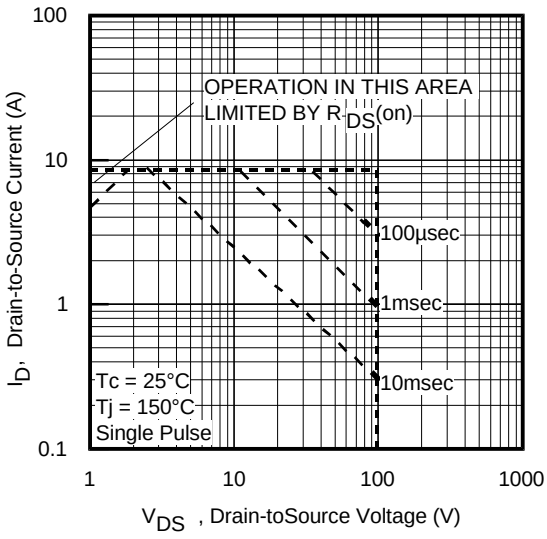



**Fig 8.** Maximum Safe Operating Area

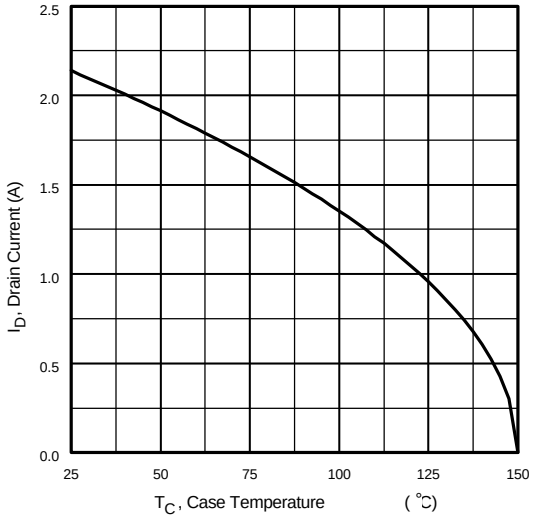



**Fig 9.** Maximum Drain Current Vs. Case Temperature

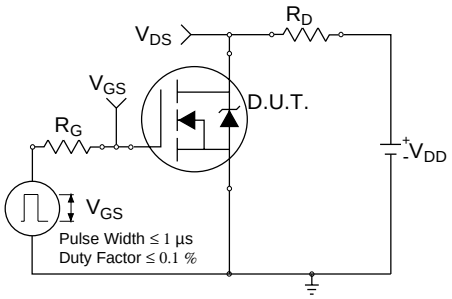



**Fig 10a.** Switching Time Test Circuit

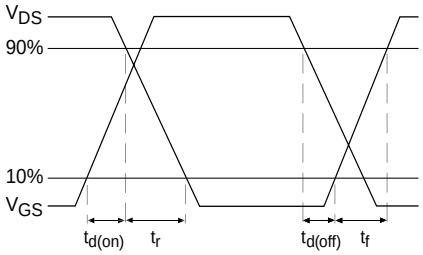



**Fig 10b.** Switching Time Waveforms

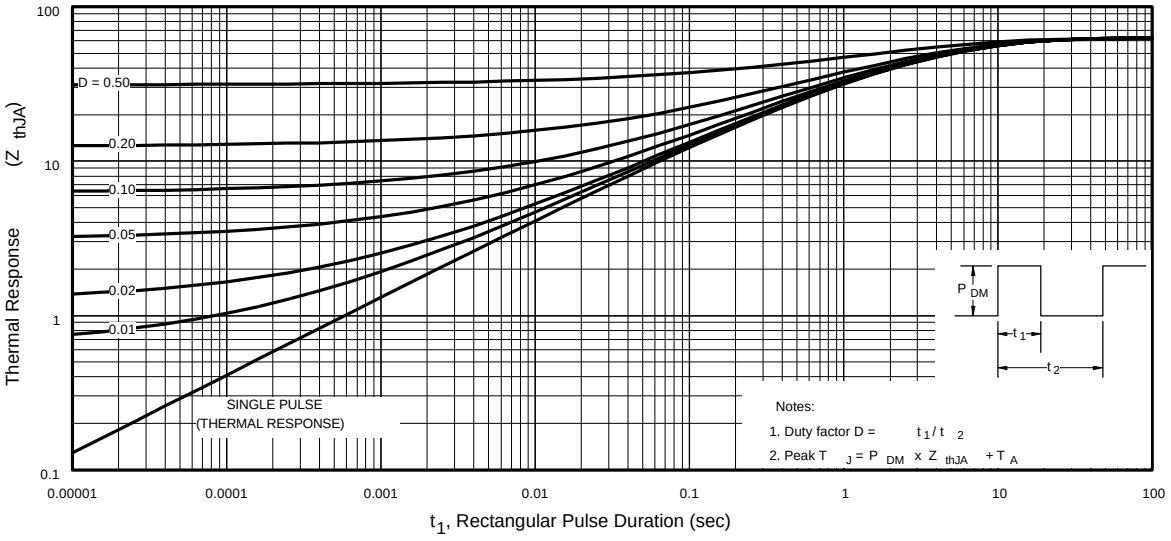



**Fig 11.** Typical Effective Transient Thermal Impedance, Junction-to-Ambient

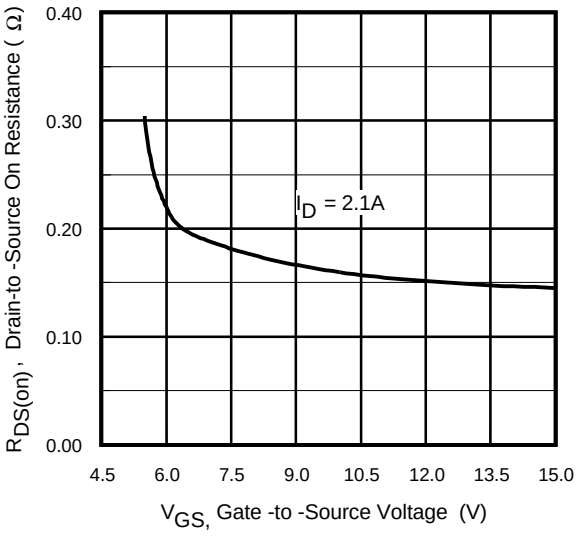



**Fig 12.** Typical On-Resistance Vs. Gate Voltage

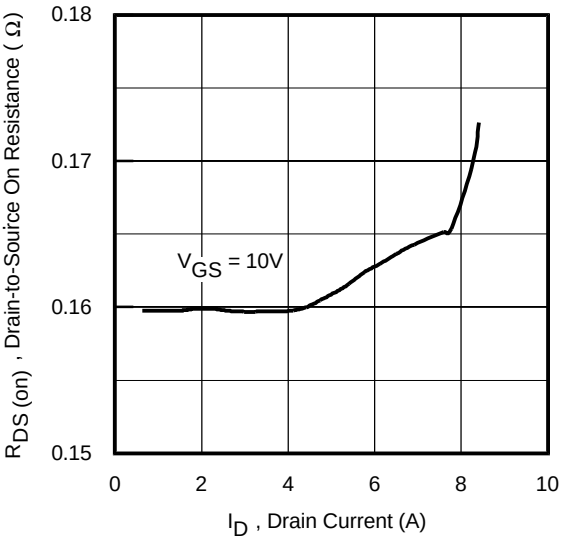



**Fig 13.** Typical On-Resistance Vs. Drain Current

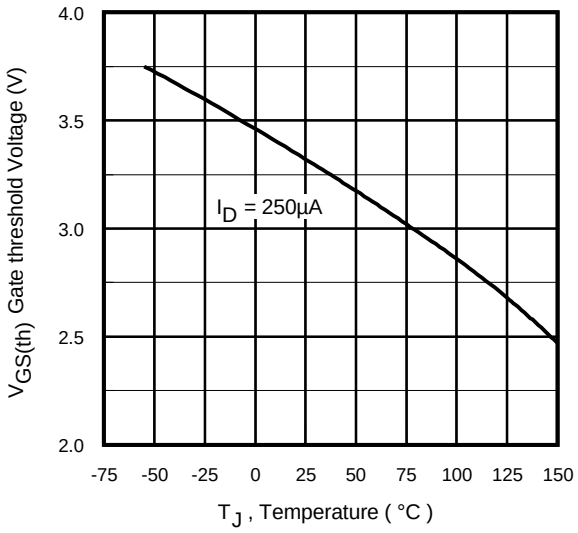



**Fig 14.** Typical Threshold Voltage Vs. Junction Temperature

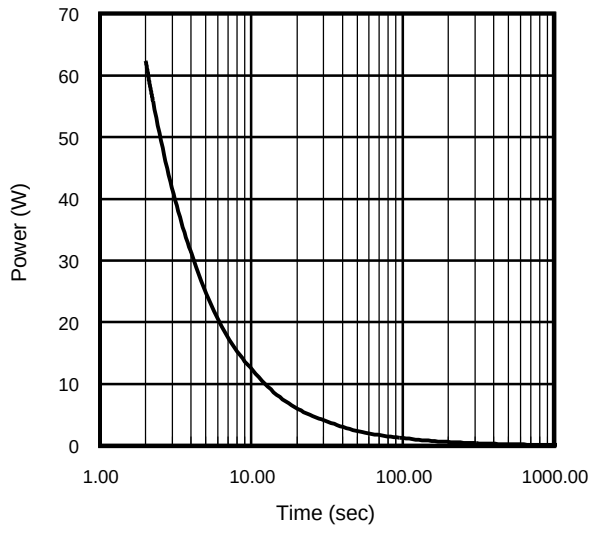



**Fig 15.** Typical Power Vs. Time

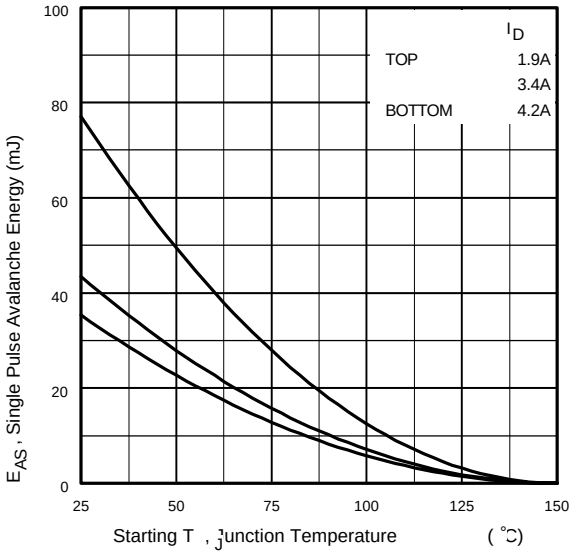



**Fig 16a.** Maximum Avalanche Energy Vs. Drain Current

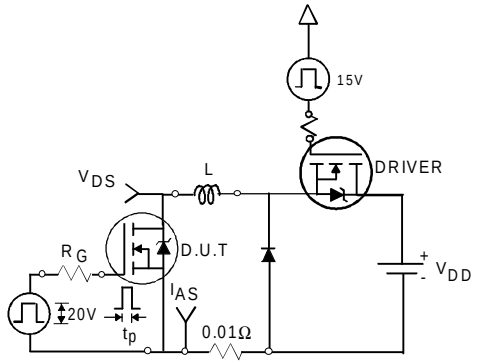



**Fig 16c.** Unclamped Inductive Test Circuit

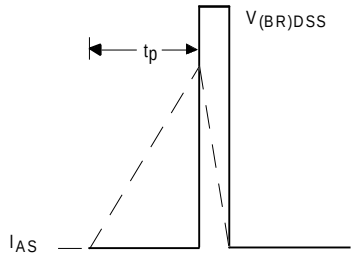



**Fig 16d.** Unclamped Inductive Waveforms

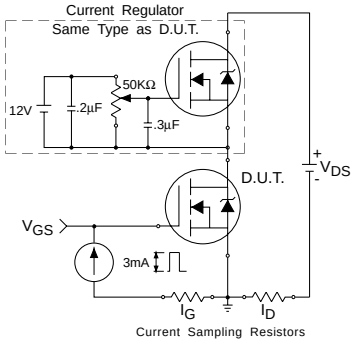



**Fig 17.** Gate Charge Test Circuit

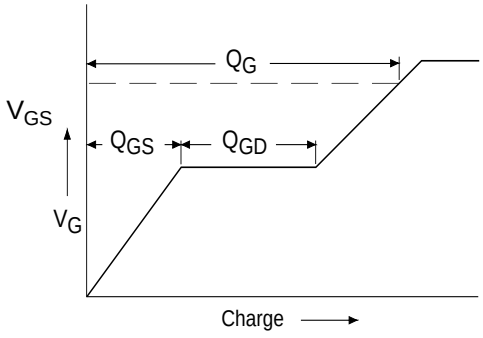



**Fig 18.** Basic Gate Charge Waveform

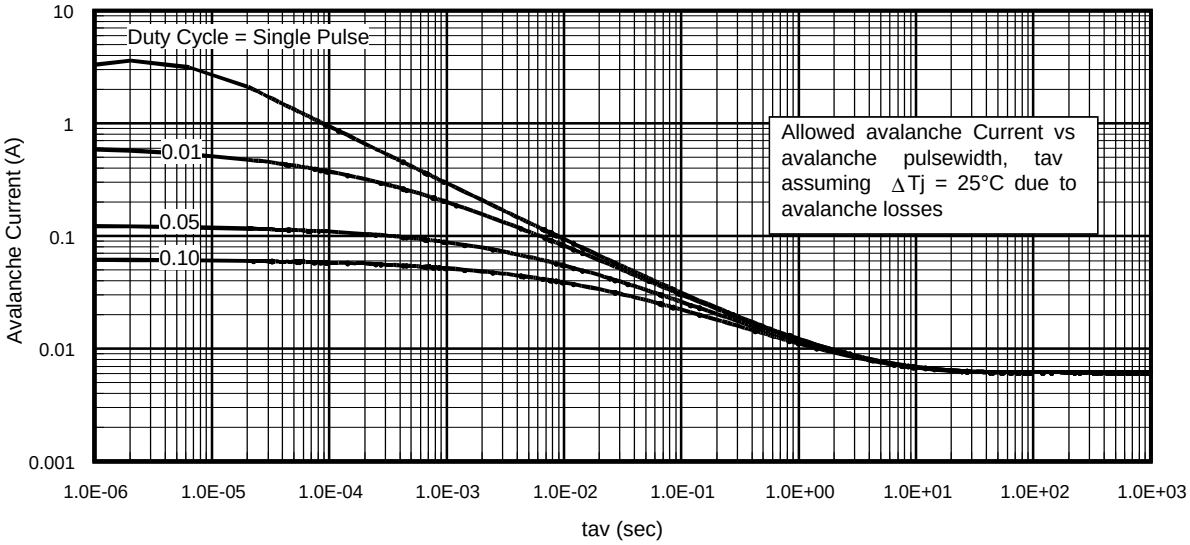



**Fig 19.** Typical Avalanche Current Vs.Pulsewidth

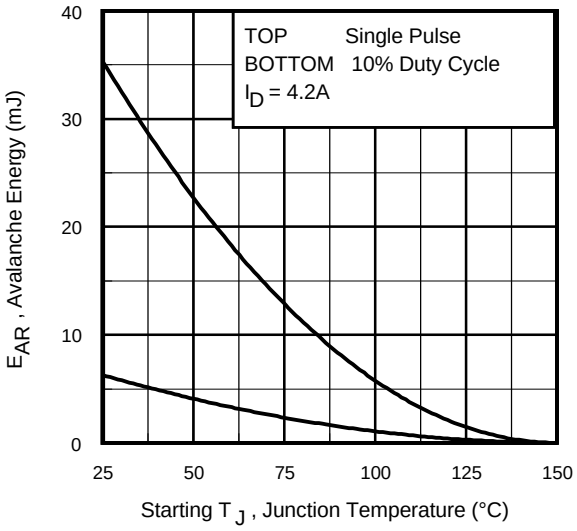



**Fig 20.** Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 15, 16).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

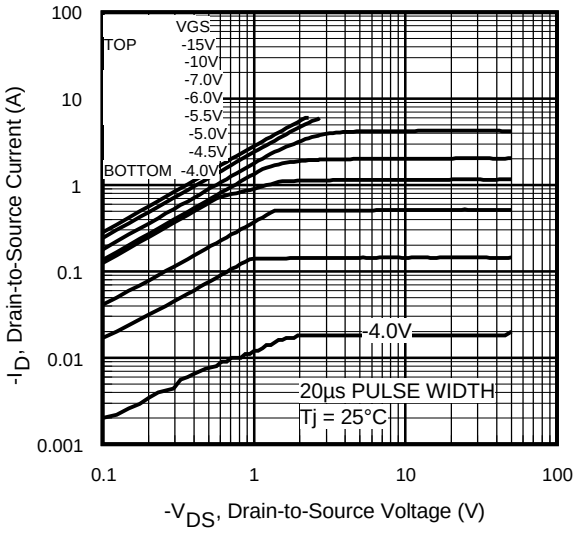



**Fig 21.** Typical Output Characteristics

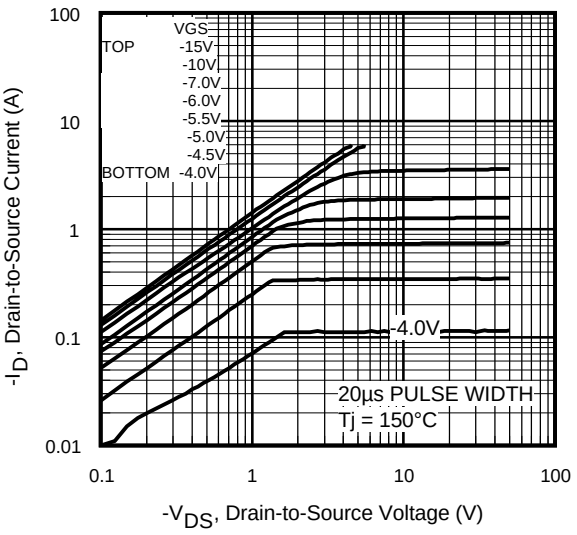



**Fig 22.** Typical Output Characteristics

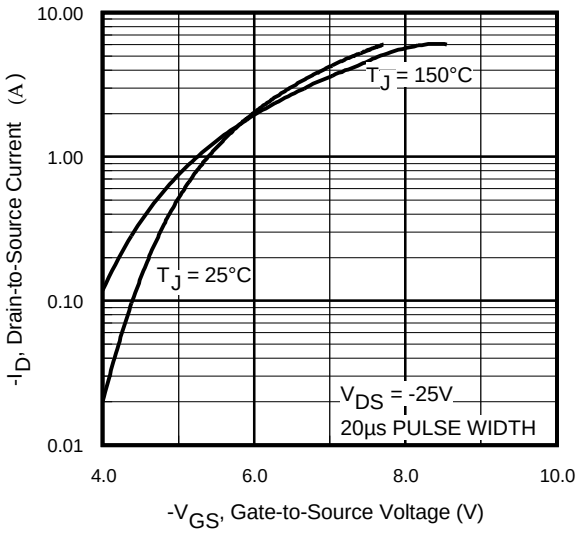



**Fig 23.** Typical Transfer Characteristics

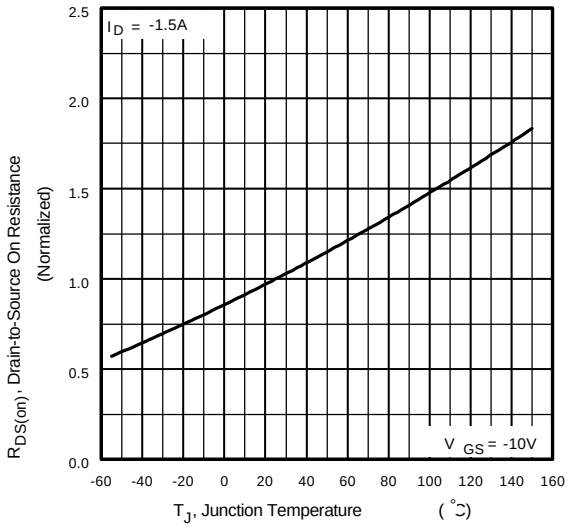



**Fig 24.** Normalized On-Resistance Vs. Temperature

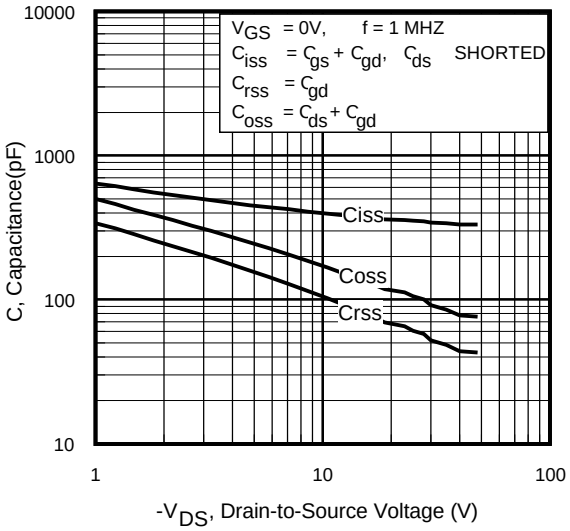



**Fig 25.** Typical Capacitance Vs. Drain-to-Source Voltage

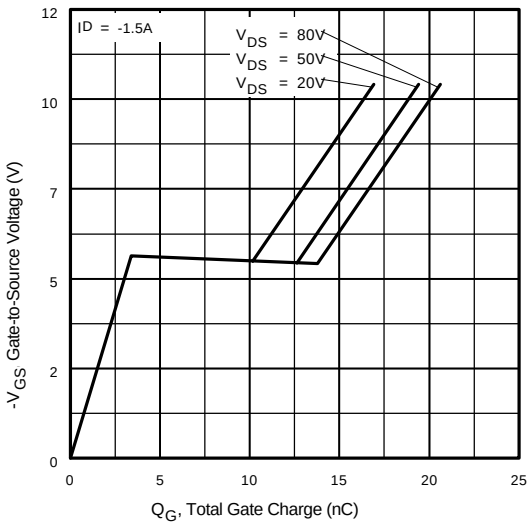



**Fig 26.** Typical Gate Charge Vs. Gate-to-Source Voltage

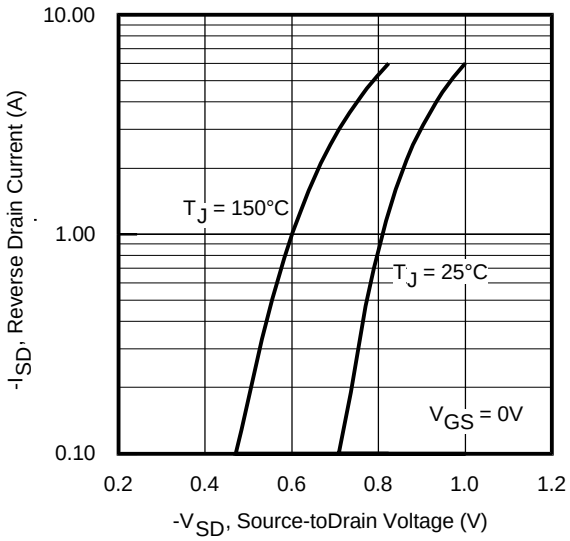



**Fig 27.** Typical Source-Drain Diode Forward Voltage

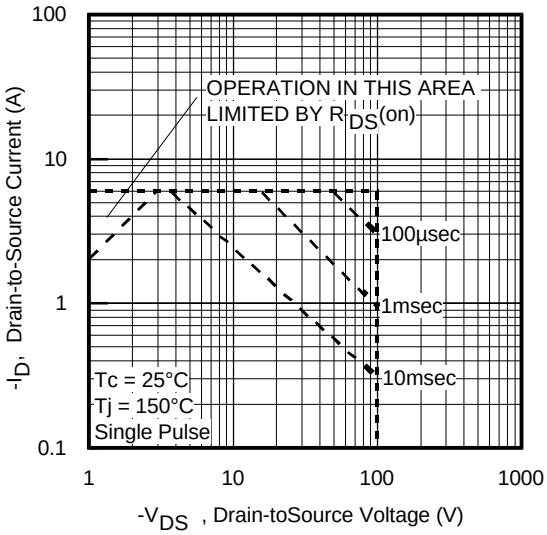



**Fig 28.** Maximum Safe Operating Area

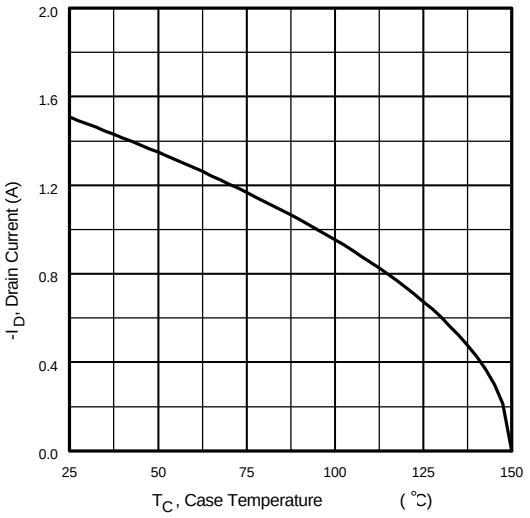



**Fig 29.** Maximum Drain Current Vs. Case Temperature

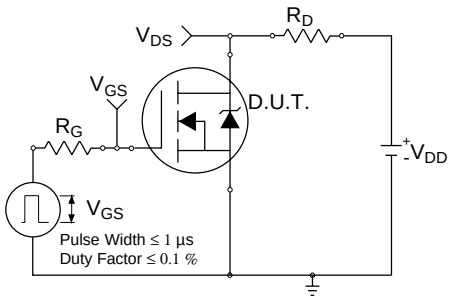



**Fig 10a.** Switching Time Test Circuit

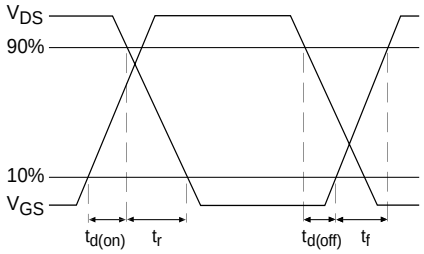



**Fig 10b.** Switching Time Waveforms

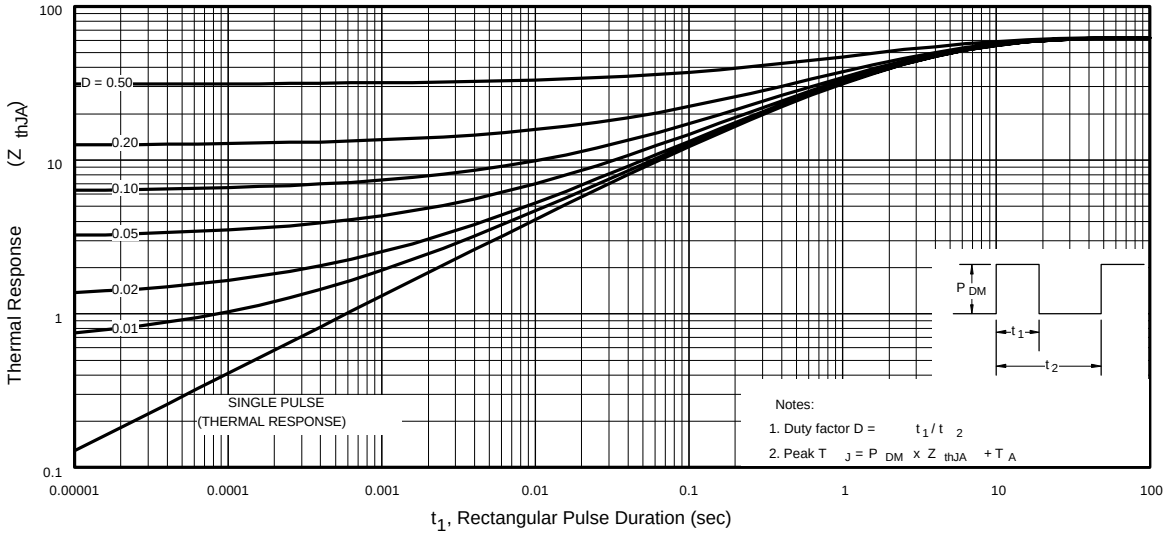



**Fig 30.** Typical Effective Transient Thermal Impedance, Junction-to-Ambient

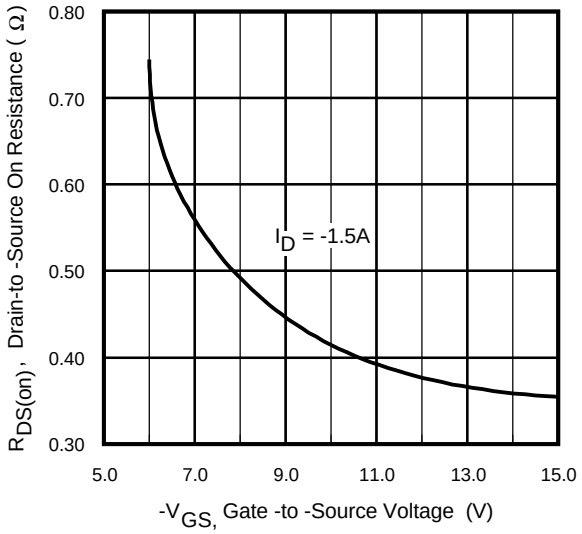



**Fig 31.** Typical On-Resistance Vs. Gate Voltage

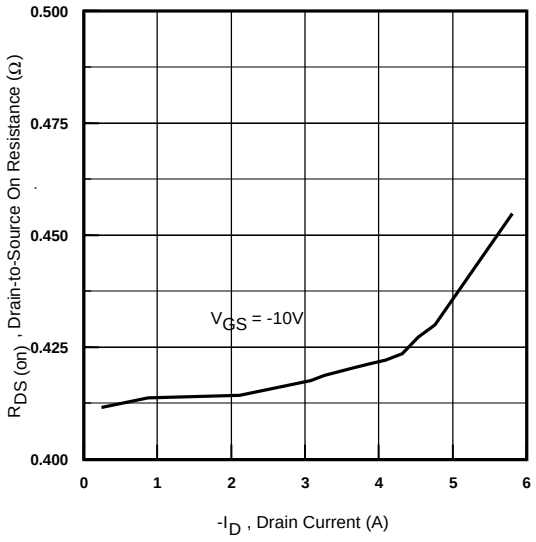



**Fig 32.** Typical On-Resistance Vs. Drain Current

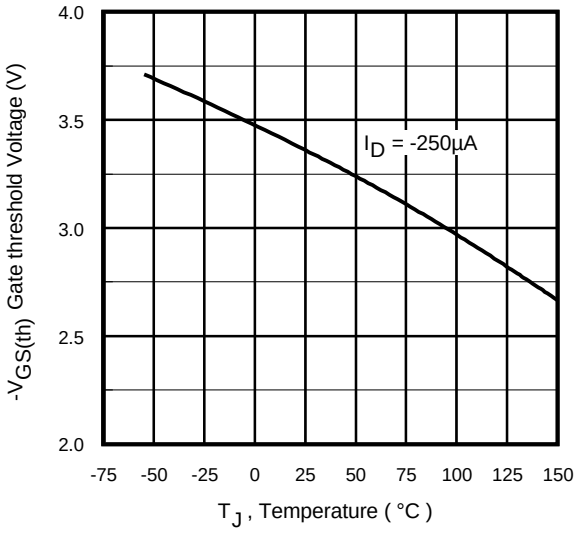



**Fig 33.** Typical Threshold Voltage Vs. Junction Temperature

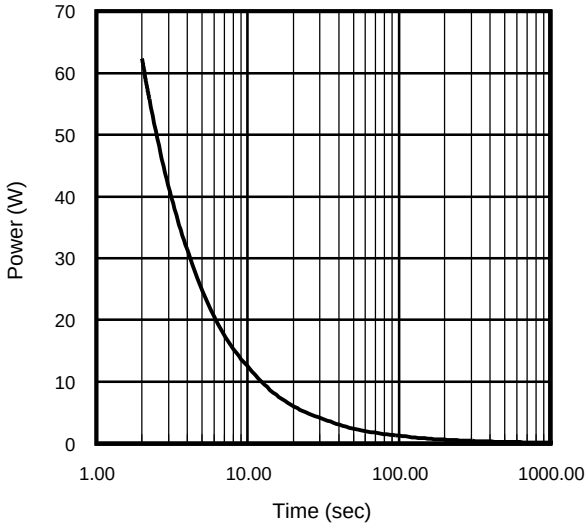



**Fig 34.** Typical Power Vs. Time

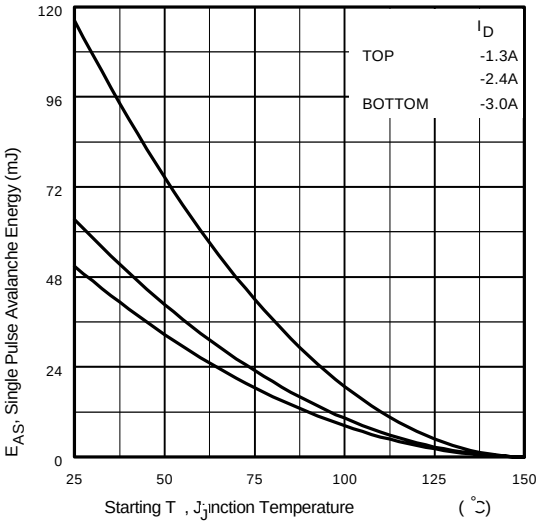



**Fig 35a.** Maximum Avalanche Energy Vs. Drain Current

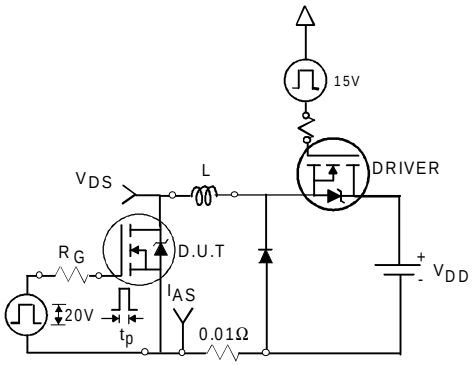



**Fig 35c.** Unclamped Inductive Test Circuit

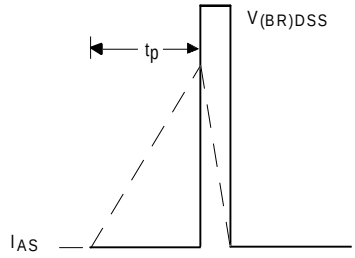



**Fig 35d.** Unclamped Inductive Waveforms

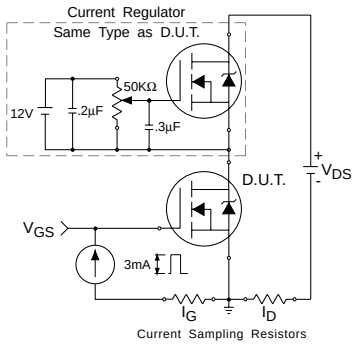



**Fig 36.** Gate Charge Test Circuit

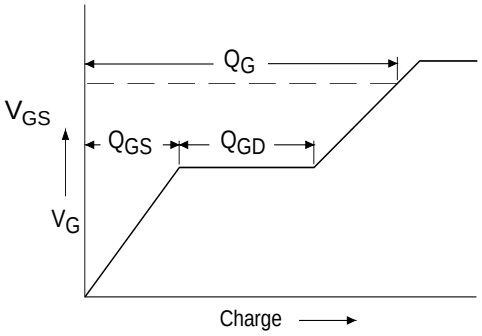



**Fig 37.** Basic Gate Charge Waveform

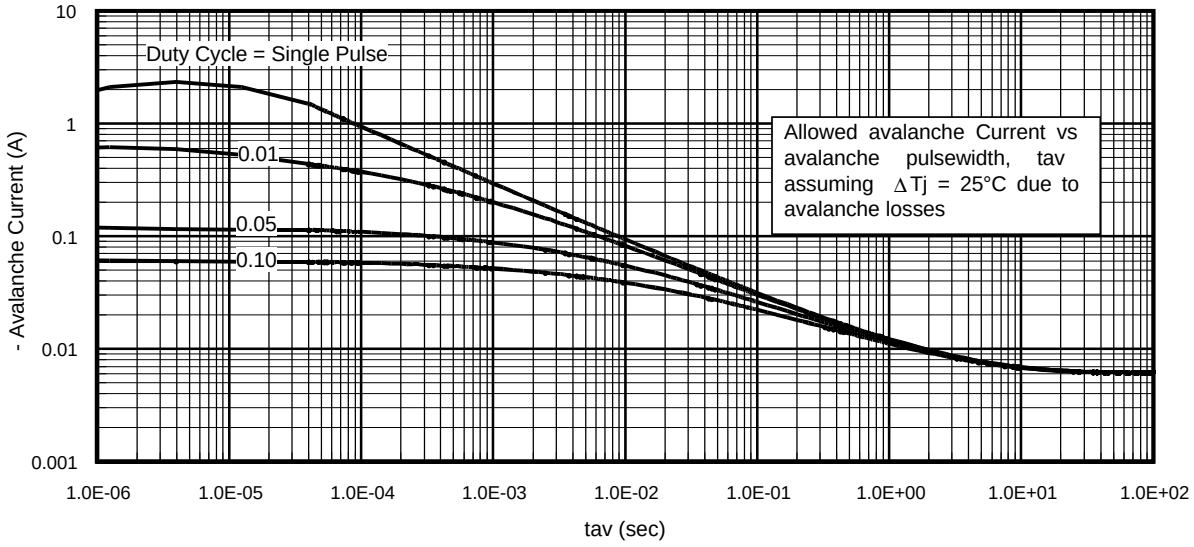



**Fig 38.** Typical Avalanche Current Vs.Pulsewidth

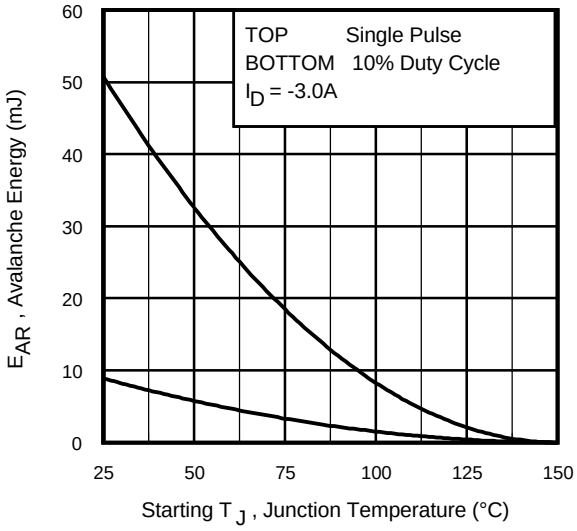


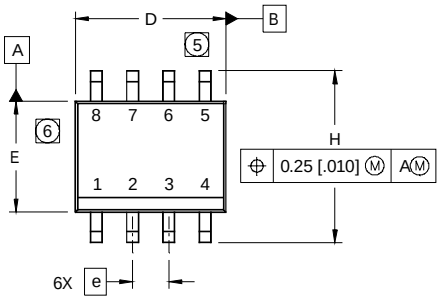

**Fig 39.** Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)**

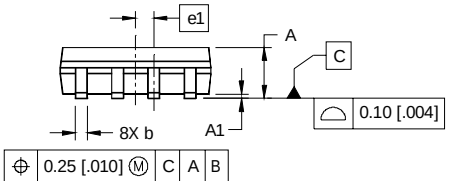
1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 15, 16).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

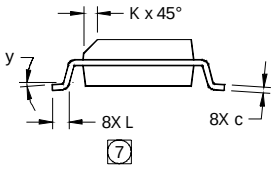
$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

## SO-8 Package Details



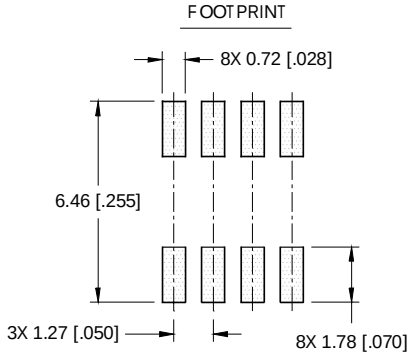

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e 1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |



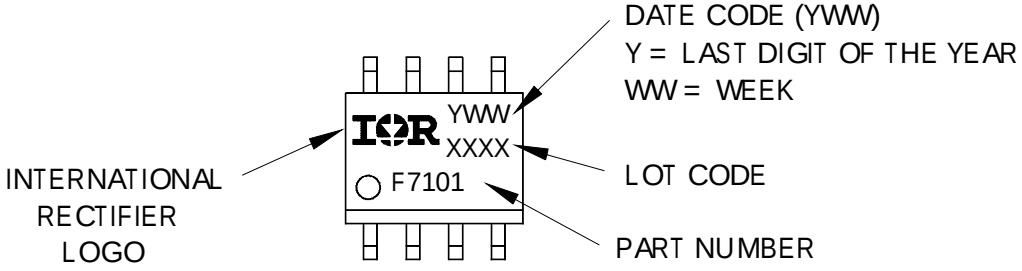

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

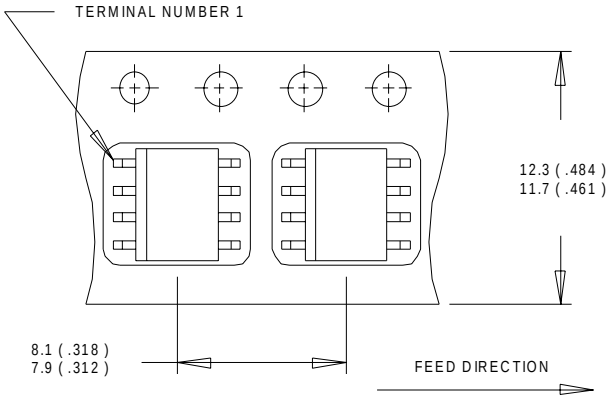



## SO-8 Part Marking

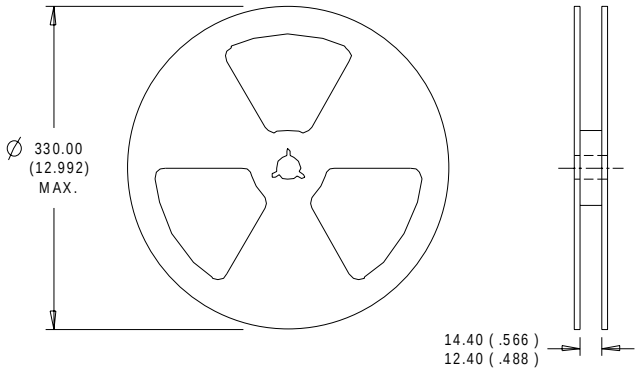
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



## SO-8 Tape and Reel




NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.




NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
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