ANALOG DEVICES

CMOS 10- & 12-Bit Monolithic Multiplying D/A Converters

AD7520/AD7521

1.1 Scope.

This specification covers the detail requirements for a 10- and a 12-bit monolithic CMOS multiplying digital-to-analog converters.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number
–1	AD7520SQ/883B
	AD7521SQ/883B
–2	AD7520TQ/883B
	AD7521TQ/883B
–3	AD7520UQ/883B
	AD7521UQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-16 – AD7520
Q-18 – AD7521

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted)

V_{DD} to GND	+17V
V_{REF} to GND	±25V
Digital Input Voltage Range	V_{DD} to GND
Output Voltage (Pins 1 and 2)	−100mV to V_{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Digital Input Voltage Range	V_{DD} to GND
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-16 or Q-18
θ_{JA} = 120°C/W for Q-16 or Q-18

AD7520/AD7521 SPECIFICATIONS

AD7520 Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1] V_{DD} = +15V	Units
Resolution	RES	−1, 2, 3	10					Bits
Relative Accuracy	RA	−1	2	2	2			± LSB max
		−2	1	2	1	1		
		−3	1/2	2	1/2	1/2		
Nonlinearity Tempco	TC_{NL}	−1, 2, 3	2					± ppm/°C max
Gain Tempco	TC_{AE}	−1, 2, 3	20					± ppm/°C max
Output Leakage Current								
Pin 1	I_{OUT1}	−1, 2, 3	200	200	200		Digital Inputs = V_{IL}.	± nA max
Pin 2	I_{OUT2}	−1, 2, 3	200	200	200		Digital Inputs = V_{IH}.	± nA max
Output Current Settling Time[2]	t_{SL}	−1, 2, 3	500				To ± 1/2LSB. All Digital Inputs V_{IL} to V_{IH} and V_{IH} to V_{IL}.	ns max
Feedthrough Error[2,3]	FT	−1, 2, 3	30				V_{REF} = 20V p-p, 100kHz, All Digital Input = V_{IL}.	mV p-p max
Reference Input Resistance	R_{IN}	−1, 2, 3	5	5	5			kΩ min
			20	20	20		Measured at Pin 15.	kΩ max
Digital Input High Voltage	V_{IH}	−1, 2, 3	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	−1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	−1, 2, 3	1.0					± μA max
Output Capacitance								
Pin 1	C_{OUT1}	−1, 2, 3	120				All Digital Inputs V_{IH}.	pF max
Pin 2	C_{OUT2}	−1, 2, 3	37				All Digital Inputs V_{IH}.	pF max
Pin 1	C_{OUT1}	−1, 2, 3	37				All Digital Inputs V_{IL}.	pF max
Pin 2	C_{OUT2}	−1, 2, 3	120				All Digital Inputs V_{IL}.	pF max
Supply Current from V_{DD}	I_{DD}	−1, 2, 3	2	2	2		All Digital Inputs V_{IL} or V_{IH}.	mA max

NOTES
[1]V_{REF} = +10V, unless otherwise stated.
[2]These design limits are +25°C only.
[3]Feedthrough error can be further minimized by connecting the metal lid to ground.

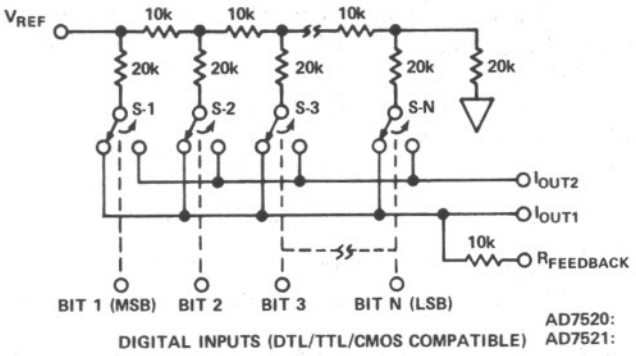
Table 1.

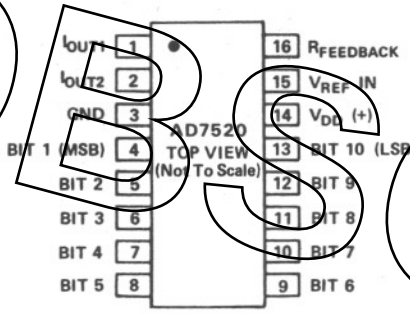
AD7521 Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1] V_{DD} = +15V	Units
Resolution	RES	–1, 2, 3	12					Bits
Relative Accuracy	RA	–1	8	8	8			± LSB max
		–2	4	8	4	4		
		–3	2	8	2	2		
Nonlinearity Tempco	TC_{NL}	–1, 2, 3	2					± ppm/°C max
Gain Tempco	TC_{AE}	–1, 2, 3	20					± ppm/°C max
Output Leakage Current								
Pin 1	I_{OUT1}	–1, 2, 3	200	200	200		Digital Inputs = V_{IL}.	± nA max
Pin 2	I_{OUT2}	–1, 2, 3	200	200	200		Digital Inputs = V_{IH}.	± nA max
Output Current Settling Time[2]	t_{SL}	–1, 2, 3	500				To ± 1/2LSB. All Digital Inputs V_{IL} to V_{IH} and V_{IH} to V_{IL}.	ns max
Feedthrough Error[2,3]	FT	–1, 2, 3	30				V_{REF} = 20V p-p, 100kHz, All Digital Input = V_{IL}.	mV p-p max
Reference Input Resistance	R_{IN}	–1, 2, 3	5 20	5 20	5 20		Measured at Pin 17.	kΩ min kΩ max
Digital Input High Voltage	V_{IH}	–1, 2, 3	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	–1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	–1, 2, 3	1.0					± µA max
Output Capacitance								
Pin 1	C_{OUT1}	–1, 2, 3	120				All Digital Inputs V_{IH}.	pF max
Pin 2	C_{OUT2}	–1, 2, 3	37				All Digital Inputs V_{IH}.	pF max
Pin 1	C_{OUT1}	–1, 2, 3	37				All Digital Inputs V_{IL}.	pF max
Pin 2	C_{OUT2}	–1, 2, 3	120				All Digital Inputs V_{IL}.	pF max
Supply Current from V_{DD}	I_{DD}	–1, 2, 3	2	2	2		All Digital Inputs V_{IL} or V_{IH}.	mA max

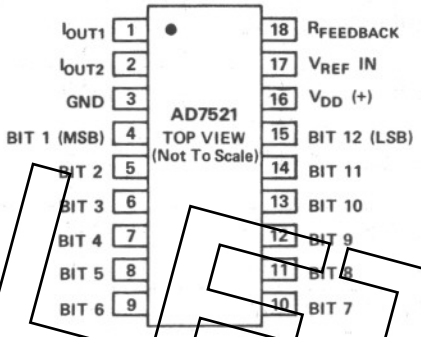
NOTES
[1]V_{REF} = +10V, unless otherwise stated.
[2]These design limits are +25°C only.
[3]Feedthrough error can be further minimized by connecting the metal lid to ground.

Table 2.

3.2.1 Functional Block Diagram and Terminal Assignments.







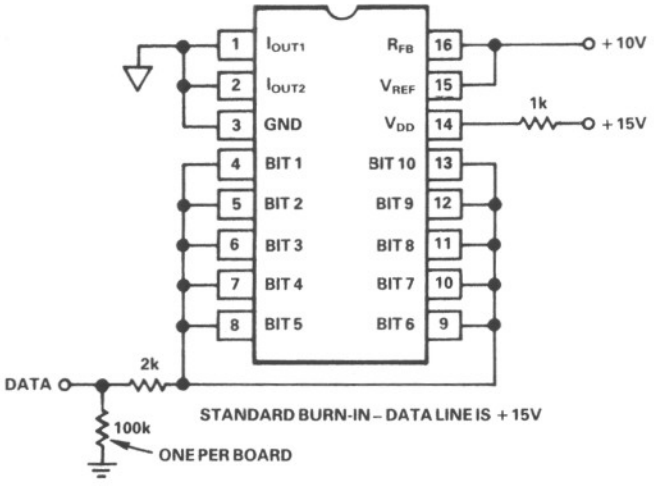
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

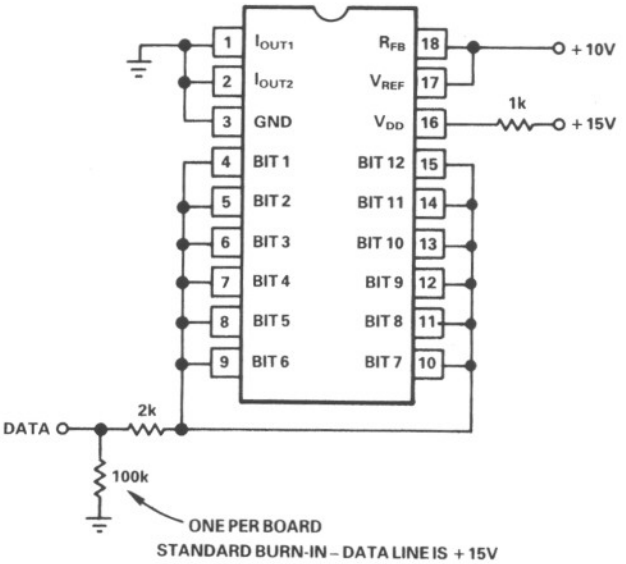
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

AD7520



AD7521



REV. B

CMOS 10- & 12-Bit Monolithic Multiplying D/A Converters

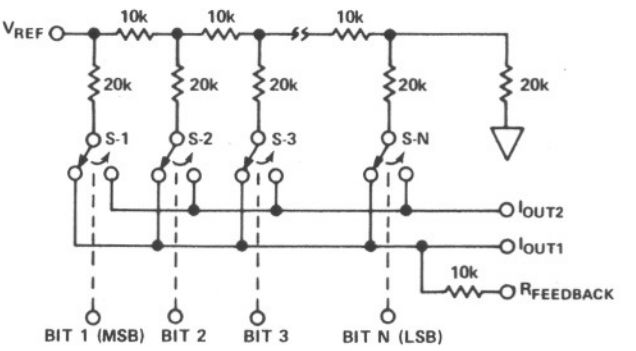
AD7520, AD7521

FEATURES

- AD7520: 10-Bit Resolution
- AD7521: 12-Bit Resolution
- End Point Linearity: 8-, 9- and 10-Bit
- Nonlinearity Tempco: 2ppm of FSR/°C
- Low Power Dissipation: 20mW
- Current Settling Time: 500ns
- Feedthrough Error: 1/2LSB @ 100kHz
- TTL/DTL/CMOS Compatible

Note: AD7533 is recommended for new 10-bit designs. AD7541A or AD7545 is recommended for new 12-bit designs.

AD7520, AD7521 FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

AD7520: N=10
AD7521: N=12
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

GENERAL DESCRIPTION

The AD7520 (AD7521) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The devices use advanced CMOS and thin film technologies providing up to 10-bit accuracy with TTL/DTL/CMOS compatibility.

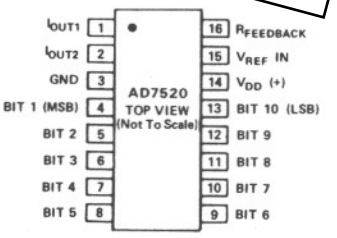
The AD7520 (AD7521) operates from +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical AD7520 (AD7521) applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

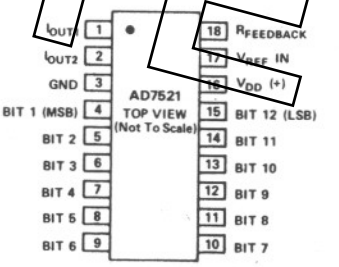
ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7521JN	AD7520JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7521KN	AD7520KD AD7521KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7521LN	AD7520LD AD7521LD	AD7520UD AD7521UD

PIN CONFIGURATIONS



16-PIN DIP



18-PIN DIP

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP Package
AD7520: (D16B)
AD7521: (D18B)

Suffix N: Plastic DIP Package
AD7520 (N16B)
AD7521 (N18B)

[1] See Section 19 for package outline information.

SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER	AD7520	AD7521	TEST CONDITIONS
DC ACCURACY[1]			
Resolution	10 Bits	12 Bits	
Relative Accuracy (See Figure 5)			
	J, 0.2% of FSR max (8 Bit)	*	S,T,U: over −55°C to +125°C
	S, 0.2% of FSR max (8 Bit)	*	$-10V \leq V_{REF} \leq +10V$
	K, 0.1% of FSR max (9 Bit)	*	
	T, 0.1% of FSR max (9 Bit)	*	
	L, 0.05% of FSR max (10 Bit)	*	
	U, 0.05% of FSR max (10 Bit)	*	
Nonlinearity Tempco	2ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Gain Error[2]	0.3% of FSR typ	*	$-10V \leq V_{REF} \leq +10V$
Gain Error Tempco[2]	10ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Output Leakage Current (either output)	200nA max	*	Over specified temperature range
Power Supply Rejection (See Figure 6)	50ppm of FSR/% typ	*	
AC ACCURACY			To 0.05% of FSR
Output Current Settling Time (See Figure 10)	500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error (See Figure 9)[4]	10mV p-p max		V_{REF} = 20V p-p, 100kHz
		*	All digital inputs low
REFERENCE INPUT			
Input Resistance[3]	5kΩ min	*	
	10kΩ typ	*	
	20kΩ max	*	
ANALOG OUTPUT			
Output Capacitance (I_{OUT1}) (See Figure 8)	120pF typ	*	All digital inputs high
Output Capacitance (I_{OUT2}) (See Figure 8)	37pF typ	*	All digital inputs high
Output Capacitance (I_{OUT1}) (See Figure 8)	37pF typ	*	All digital inputs low
Output Capacitance (I_{OUT2}) (See Figure 8)	120pF typ	*	All digital inputs low
Output Noise (both outputs) (See Figure 7)	Equivalent to 10kΩ typ Johnson noise	*	
DIGITAL INPUTS[5]			
Low State Threshold	0.8V max	*	Over specified temperature range
High State Threshold	2.4V min	*	Over specified temperature range
Input Current (low to high state)	1μA typ	*	Over specified temperature range
Input Coding	Binary	*	See Tables I & II under Applications
POWER REQUIREMENTS			
Power Supply Voltage Range	+5V to +15V	*	
I_{DD}	5nA typ	*	All digital inputs at GND
	2mA max	*	All digital inputs high or low
Total Dissipation (Including ladder)	20mW typ	*	

NOTES
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] Using the internal $R_{FEEDBACK}$
[3] Ladder and feedback resistor tempco is approximately −150ppm/°C.
[4] To minimize feedthrough with the ceramic package, the user must ground the metal lid. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.
[5] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . −100mV to V_{DD}
Power Dissipation (package)
  up to +75°C 450mW
  derates above +75°C by . . . . . 6mW/°C
Operating Temperature
  JN, KN, LN Versions . . . . . 0 to +70°C
  JD, KD, LD Versions . . . . . −25°C to +85°C
  SD, TD, UD Versions . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V unless otherwise noted

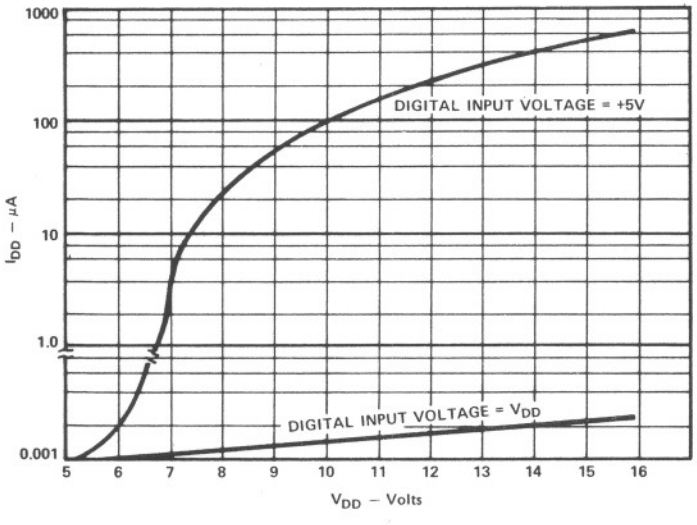


Figure 1. Supply Current vs. Supply Voltage

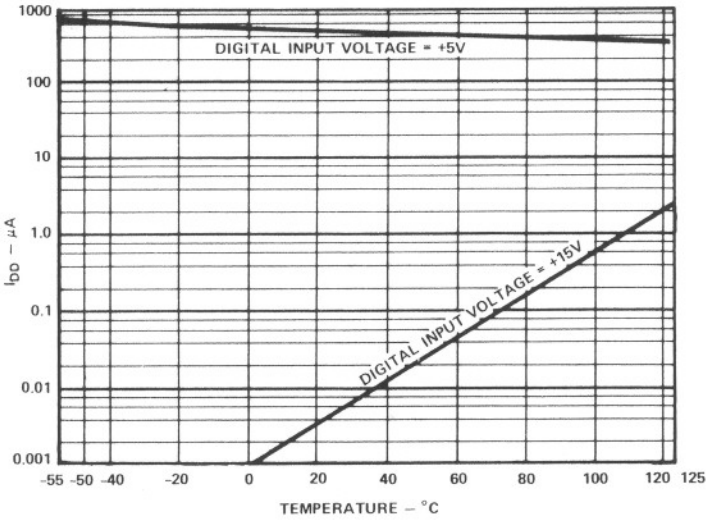


Figure 2. Supply Current vs. Temperature

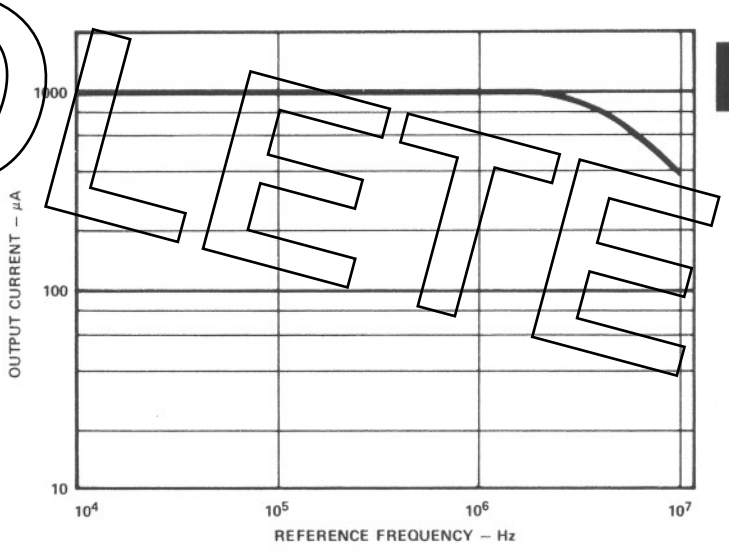


Figure 3. Output Current Bandwidth

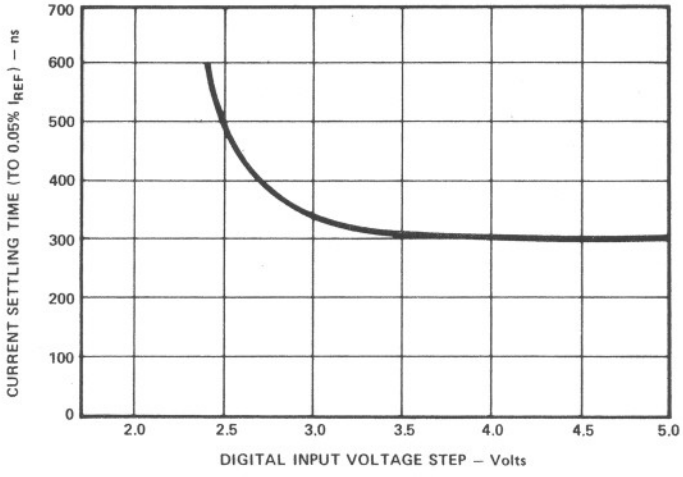


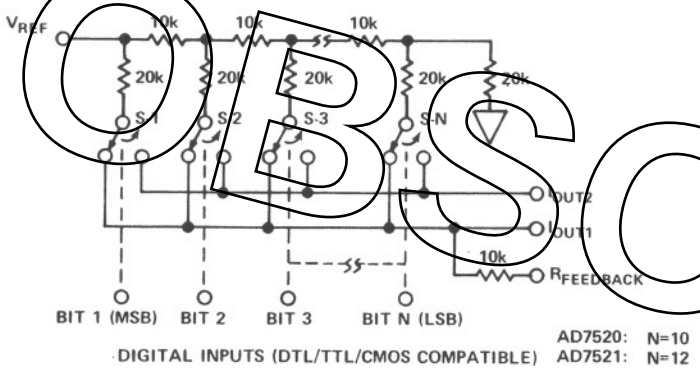
Figure 4. Output Current Settling Time vs. Digital Input Voltage

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7521), a 10-bit (12-bit) multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten (twelve) CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 11. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.



(Switches shown for Inputs "High")

Figure 11. AD7520 (AD7521) Functional Diagram

One of the CMOS current switches is shown in Figure 12. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch-1 of Figure 12 was designed for an "ON" resistance of 20 ohms, switch-2 of 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

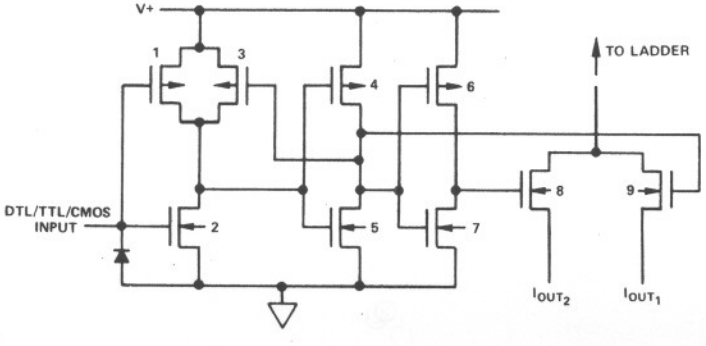


Figure 12. CMOS Switch

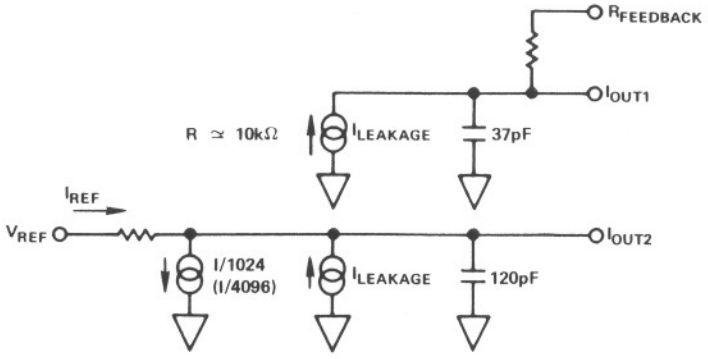


Figure 13. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 13 and 14. In Figure 13 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}\left(\frac{I}{4096}\right)$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 37pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 14 is similar to Figure 13; however, the "ON" switches are now on terminal I_{OUT1}, hence the 120pF at that terminal.

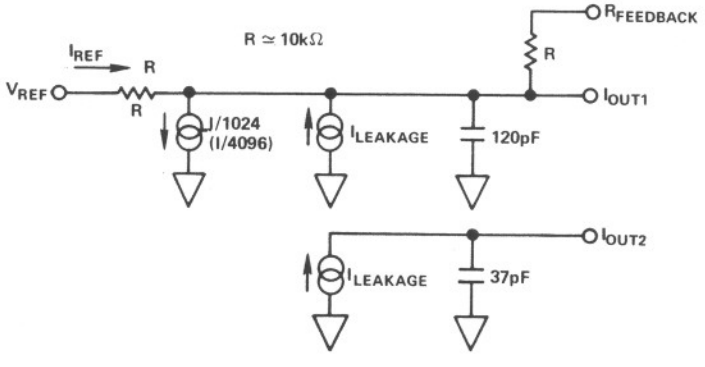


Figure 14. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs High

TEST CIRCUITS

Note: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7521.

DC PARAMETERS

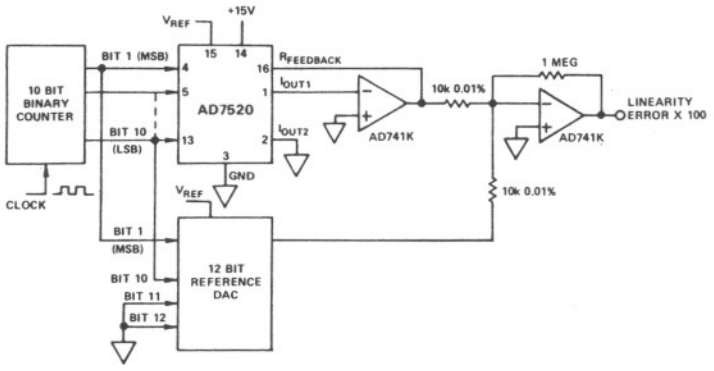


Figure 5. Relative Accuracy

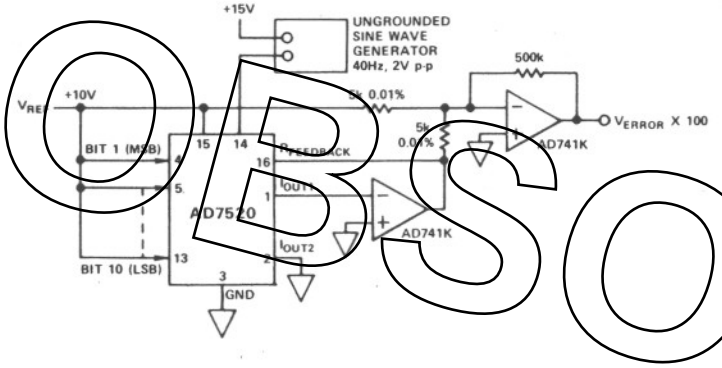


Figure 6. Power Supply Rejection

AC PARAMETERS

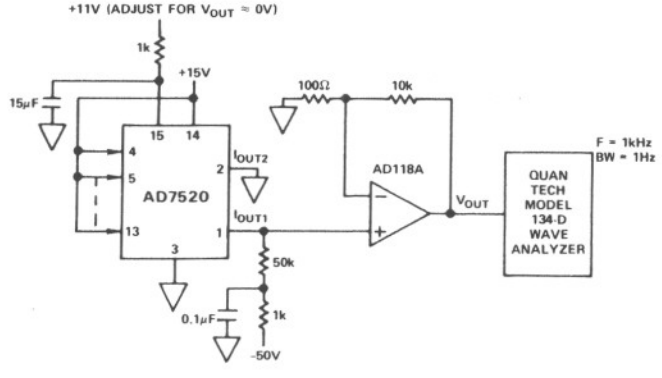


Figure 7. Noise

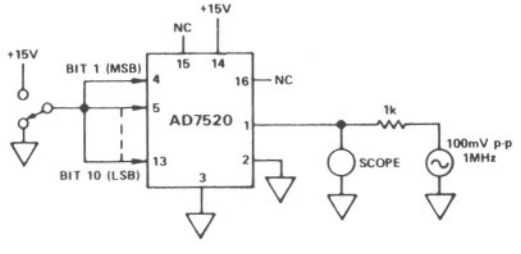


Figure 8. Output Capacitance

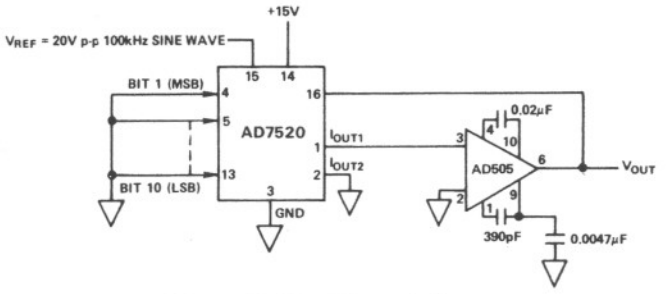


Figure 9. Feedthrough Error

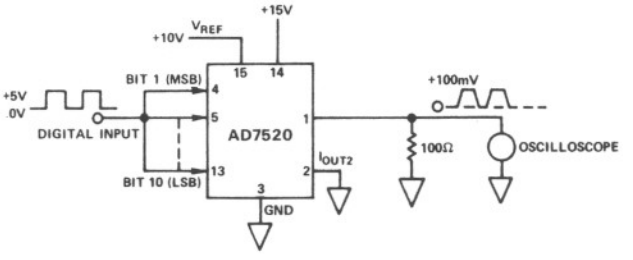


Figure 10. Output Current Settling Time

TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

APPLICATIONS

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 15 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table I. Protection Schottky shown in Figure 15 is not required when using TRIFET output amplifiers such as the AD542 or AD544.

R1 provides full scale trim capability [i.e.—load the DAC register to 11 1111 1111, adjsut R1 for $V_{OUT} = -V_{REF}(1 - 2^{-10})$]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at I_{OUT1}).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ).

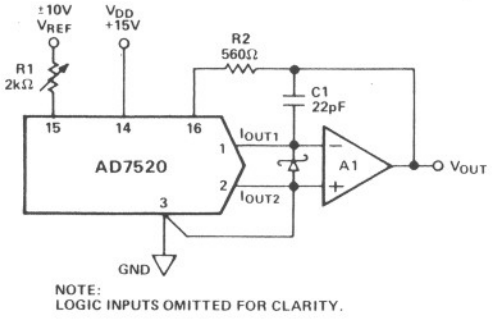


Figure 15. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table I. Code Table — Unipolar Binary Operation

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 16 and Table II illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) or an ac reference the circuit provides offset binary operation. Protection Schottky shown in Figure 16 is not required when using TRIFET output amplifiers such as the AD542 or AD544.

With the DAC register loaded to 10 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. Ci phase compensation (10pF to 25pF) may be required for stability.

Offset Adjustment

1. Make V_{REF} approximately +10V.
2. Tie all digital inputs to +15V (Logic "1").
3. Adjust amplifier #2 offset trimpot for 0V ±1mV at amplifier #2 output.
4. Tie MSB (Bit 1) to +15V, all other bits to ground.
5. Adjust amplifier #1 offset trimpot for 0V ±1mV at V_{OUT}.

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

Table II. Code Table — Bipolar (Offset Binary) Operation

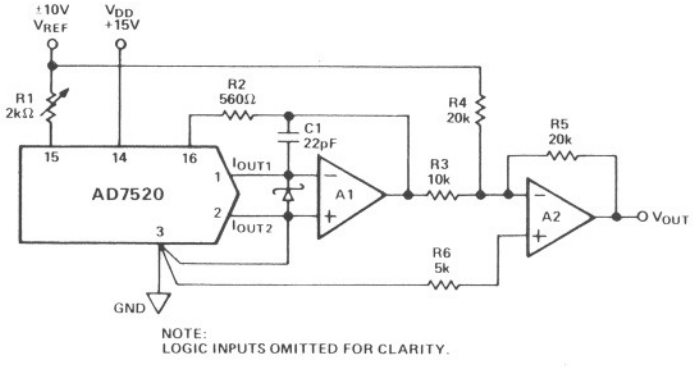


Figure 16. Bipolar Operation (4-Quadrant Multiplication)

10-BIT AND SIGN MULTIPLYING DAC

Figure 17 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 10-bit resolution in each quadrant. The 10 magnitude bits provide digitally controlled attenuation of the reference while the sign bit provides polarity control. The AD7512 is a fully protected CMOS change-over switch. Mismatch between R4 and R5 introduces a gain error. Table III shows the Code Table for the circuit of Figure 17.

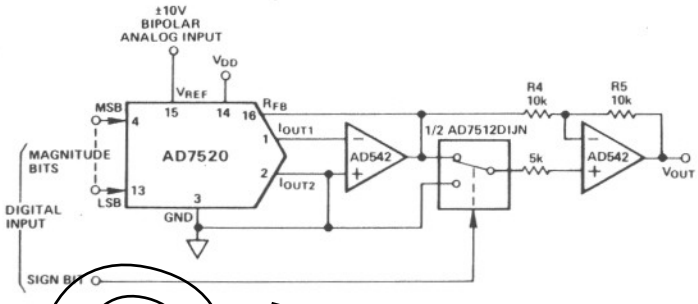


Figure 17. 10-Bit and Sign Multiplying DAC

Sign Bit	Binary Numbers in DAC Register	Analog Output
0	11 1111 1111	$+V_{IN} \cdot 1-2^{-10}$
0	00 0000 0000	0 Volts
1	00 0000 0000	0 Volts
1	11 1111 1111	$-V_{IN} \cdot 1-2^{-10}$

Table III. 10-Bit Plus Sign Magnitude Table

DIGITALLY PROGRAMMABLE LIMIT DETECTOR

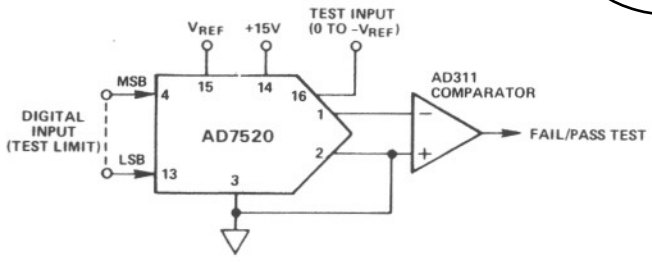


Figure 18. Programmable Limit Detector

The circuit of Figure 18 shows how the AD7520 is used to implement a programmable limit detector. If the test input does not meet the test limit set by the digital input, then the pass/fail output will indicate a fail.

VOLTAGE MODE OPERATION

The AD7520 can also be used in the voltage-switching mode and the circuit of Figure 19 shows how the DAC can be connected for voltage switching by reversing the roles of the reference input and I_{OUT1}. It is a single supply application with the DAC and the CMOS operational amplifier both powered from a single +15V supply. With a single supply operational amplifier, offset is difficult to remove completely; therefore, some offset may have to be tolerated usually amounting to less than one-half LSB at 3.5V reference. The voltage switching mode permits only a single polarity of input (positive with respect to common).

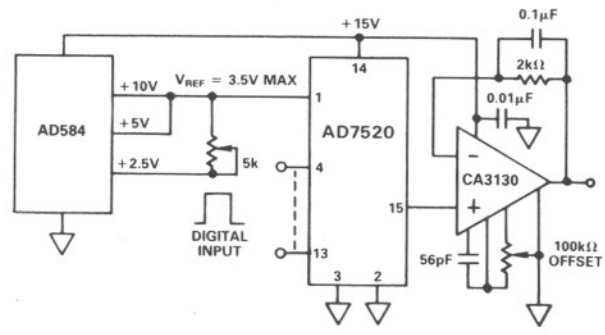


Figure 19. Single Supply Voltage Mode Operation

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_0 = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 20, the transfer function becomes

$$V_0 = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit 10) ON, the gain is 1024. With all bits ON, the gain is 1 (±1 LSB).

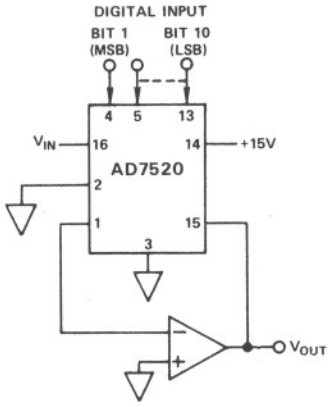


Figure 20. Analog/Digital Divider