National Semiconductor

May 1996

DAC1020/DAC1021/DAC1022 10-Bit Binary Multiplying D/A Converter DAC1220/DAC1222 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1020 and the DAC1220 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.0002%/°C linearity error temperature coefficient maximum). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference. All inputs are protected from damage due to static discharge by diode clamps to V^+ and ground.

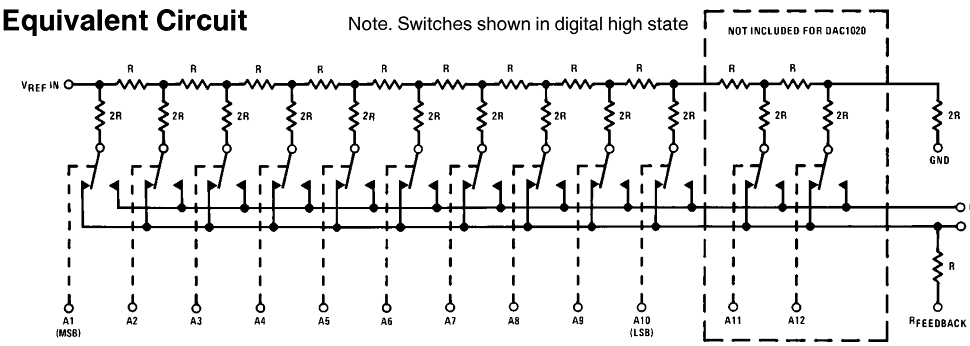
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity guaranteed over temperature (note 1 of electrical characteristics). The DAC1020, DAC1021 and DAC1022 are direct replacements for the 10-bit resolution AD7520 and AD7530 and equivalent to the AD7533 family. The DAC1220 and DAC1222 are direct replacements for the 12-bit resolution AD7521 and AD7531 family.

Features

- Linearity specified with zero and full-scale adjust only
- Non-linearity guaranteed over temperature
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq 25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—500 ns typ
- Low feedthrough error—½ LSB @100 kHz typ

Equivalent Circuit

Note. Switches shown in digital high state



TL/H/5689–1

Ordering Information

10-BIT D/A CONVERTERS

Temperature Range		0°C to 70°C			−40°C to 85°C
Non-Linearity	0.05%	DAC1020LCN	AD7520LN,AD7530LN	DAC1020LCV	DAC1020LIV
	0.10%	DAC1021LCN	AD7520KN,AD7530KN		
	0.20%	DAC1022LCN	AD7520JN,AD7530JN		
Package Outline		N16A		V20A	

12-BIT D/A CONVERTERS

Temperature Range		0°C to 70°C		−40°C to +85°C	
Non-Linearity	0.05%	DAC1220LCN	AD7521LN,AD7531LN	DAC1220LCJ	AD7521LD,AD7531LD
	0.20%	DAC1222LCN	AD7521JN,AD7531JN	DAC1222LCJ	AD7521JD,AD7531JD
Package Outline		N18A		J18A	

Note. Devices may be ordered by either part number.

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
ESD Susceptibility (Note 4)	800V

Operating Ratings

	Min	Max	Units
Temperature (T_A)			
DAC1020LIV, DAC1220LCJ, DAC1222LCJ	−40	+85	°C
DAC1020LCN, DAC1020LCV, DAC1021LCN	0	+70	°C
DAC1022LCN, DAC1220LCN	0	+70	°C
DAC1222LCN	0	+70	°C

Electrical Characteristics (V^+ = 15V, V_{REF} = 10.000V, T_A = 25°C unless otherwise specified)

Parameter	Conditions	DAC1020, DAC1021, DAC1022			DAC1220, DAC1222			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		10			12			Bits
Linearity Error	$T_{MIN} < T_A < T_{MAX}$, $-10V < V_{REF} < +10V$, (Note 1) End Point Adjustment Only (See Linearity Error in Definition of Terms)							
10-Bit Parts	DAC1020, DAC1220			0.05			0.05	% FSR
9-Bit Parts	DAC1021			0.10			0.10	% FSR
8-Bit Parts	DAC1022, DAC1222			0.20			0.20	% FSR
Linearity Error Tempco	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)			0.0002			0.0002	% FS/°C
Full-Scale Error	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)		0.3	1.0		0.3	1.0	% FS
Full-Scale Error Tempco	$T_{MIN} < T_A < T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current	$T_{MIN} \le T_A \le T_{MAX}$							
$I_{OUT\ 1}$	All Digital Inputs Low			200			200	nA
$I_{OUT\ 2}$	All Digital Inputs High			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \le V^+ \le 16V$, (Note 2), *(Figure 2)*		0.005			0.005		% FS/V
V_{REF} Input Resistance		10	15	20	10	15	20	kΩ
Full-Scale Current Settling Time	R_L = 100Ω from 0 to 99. 95% FS All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low,			10			10	mVp-p
	V_{REF} = 20 Vp-p @ 100 kHz							
	J Package (Note 4)		6	9		6	9	mVp-p
	N Package		2	5		2	5	mVp-p
Output Capacitance								
$I_{OUT\ 1}$	All Digital Inputs Low		40			40		pF
	All Digital Inputs High		200			200		pF
$I_{OUT\ 2}$	All Digital Inputs Low		200			200		pF
	All Digital Inputs High		40			40		pF

Electrical Characteristics ($V^+ = 15V$, $V_{REF} = 10.000V$, $T_A = 25°C$ unless otherwise specified) (Continued)

Parameter	Conditions	DAC1020, DAC1021, DAC1022			DAC1220, DAC1222			Units
		Min	Typ	Max	Min	Typ	Max	
Digital Input	*(Figure 1)*							
Low Threshold	$T_{MIN} < T_A < T_{MAX}$			0.8			0.8	V
High Threshold	$T_{MIN} < T_A < T_{MAX}$	2.4			2.4			V
Digital Input Current	$T_{MIN} \le T_A \le T_{MAX}$							
	Digital Input High		1	100		1	100	μA
	Digital Input Low		−50	−200		−50	−200	μA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range	*(Figures 1 and 2)*	5		15	5		15	V

Note 1: $V_{REF} = \pm 10V$ and $V_{REF} = \pm 1V$. A linearity error temperature coefficient of 0.0002% FS for a 45°C rise only guarantees 0.009% maximum change in linearity error. For instance, if the linearity error at 25°C is 0.045% FS it could increase to 0.054% at 70°C and the DAC will be no longer a 10-bit part. Note, however, that the linearity error is specified over the device full temperature range which is a more stringent specification since *it includes* the linearity error temperature coefficient.

Note 2: Using internal feedback resistor as shown in *Figure 3*.

Note 3: Both $I_{OUT\,1}$ and $I_{OUT\,2}$ must go to ground or the virtual ground of an operational amplifier. If $V_{REF} = 10V$, every millivolt offset between $I_{OUT\,1}$ or $I_{OUT\,2}$, 0.005% linearity error will be introduced.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 6: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temepature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the J18 package when board mounted is 85°C/W. For the N18 package, θ_{JA} is 120°C/W, for the N16 this number is 125°C/W, and for the V20 this number is 95°C/W.

Typical Performance Characteristics

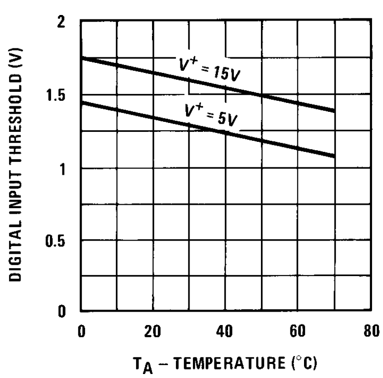


FIGURE 1. Digital Input Threshold vs Ambient Temperature

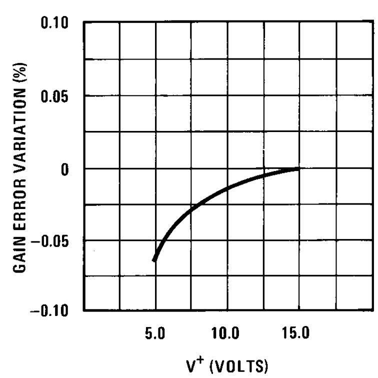


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FIGURE 2. Gain Error Variation vs V^+

Typical Applications

The following applications are also valid for 12-bit systems using the DAC1220 and 2 additional digital inputs.

Operational Amplifier Bias Current (*Figure 3*)

The op amp bias current, I_b, flows through the 15k internal feedback resistor. BI-FET op amps have low I_b and, therefore, the 15k $\times$ I_b error they introduce is negligible; they are strongly recommended for the DAC1020 applications.

V_{OS} Considerations

The output impedance, R_{OUT}, of the DAC is modulated by the digital input code which causes a modulation of the operational amplifier output offset. It is therefore recommended to adjust the op amp V_{OS}. R_{OUT} is $\sim$15k if more than 4 digital inputs are high; R_{OUT} is $\sim$45k if a single digital input is high, and R_{OUT} approaches infinity if all inputs are low.

Operational Amplifier V_{OS} Adjust (*Figure 3*)

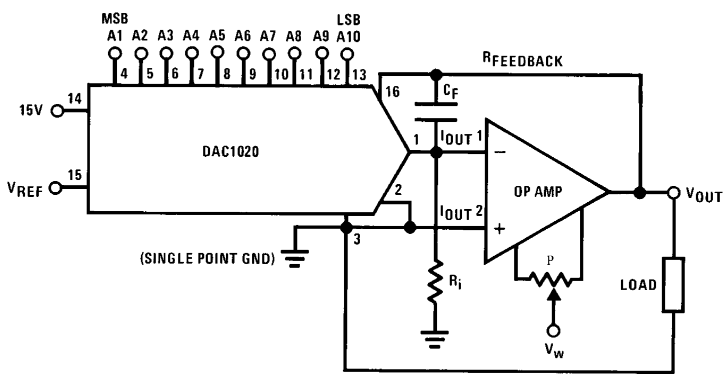
Connect all digital inputs, A1–A10, to ground and adjust the potentiometer to bring the op amp V_{OUT} pin to within $\pm$1 mV from ground potential. If V_{REF} is less than 10V, a finer V_{OS} adjustment is required. It is helpful to increase the resolution of the V_{OS} adjust procedure by connecting a 1 kΩ resistor between the inverting input of the op amp to ground. After V_{OS} has been adjusted, remove the 1 kΩ.

Full-Scale Adjust (*Figure 4*)

Switch high all the digital inputs, A1–A10, and measure the op amp output voltage. Use a 500Ω potentiometer, as shown, to bring $\|V_{OUT}\|$ to a voltage equal to V_{REF} $\times$ 1023/1024.

SELECTING AND COMPENSATING THE OPERATIONAL AMPLIFIER

Op Amp Family	C_F	R_i	P	V_W	Circuit Settling Time, t_s	Circuit Small Signal BW
LF357	10 pF	2.4k	25k	V^+	1.5 μs	1M
LF356	22 pF	∞	25k	V^+	3 μs	0.5M
LF351	24 pF	∞	10k	V^-	4 μs	0.5M
LM741	0	∞	10k	V^-	40 μs	200 kHz



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$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$$-10V \leq V_{REF} \leq 10V$$

$$0 \leq V_{OUT} \leq -\frac{1023}{1024}V_{REF}$$

where A_N = 1 if the A_N digital input is high

A_N = 0 if the A_N digital input is low

FIGURE 3. Basic Connection: Unipolar or 2-Quadrant Multiplying Configuration (Digital Attenuator)

Typical Applications (Continued)

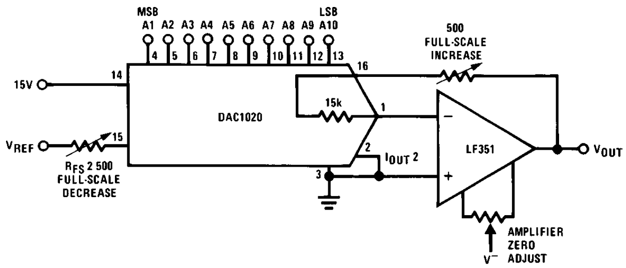


FIGURE 4. Full-Scale Adjust

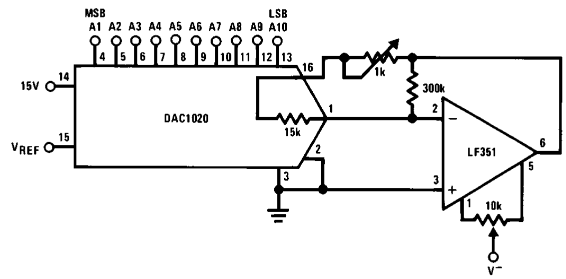
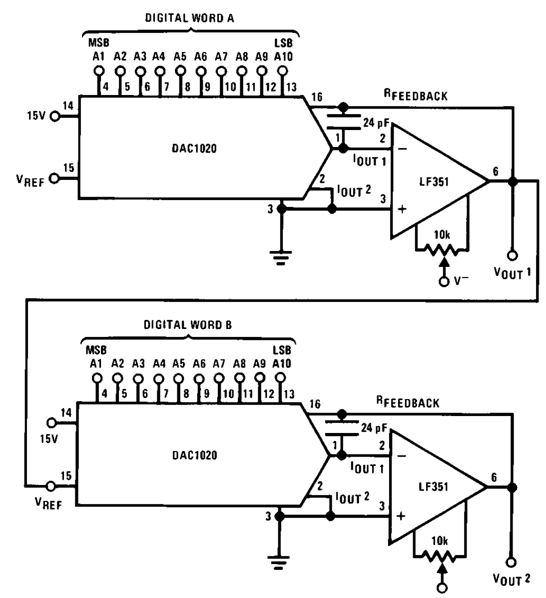


FIGURE 5. Alternate Full-Scale Adjust: (Allows Increasing or Decreasing the Gain)



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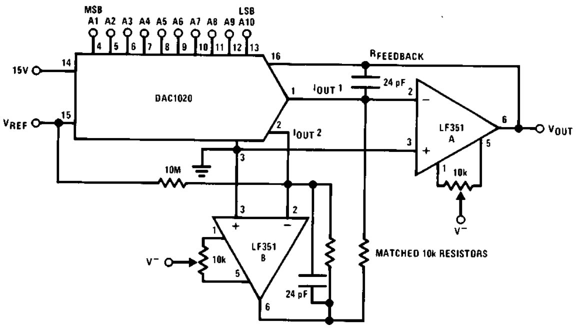
$$V_{OUT\,1} = -V_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\bullet\bullet\bullet\frac{A10}{1024}\right)$$

$$V_{OUT2} = V_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\bullet\bullet\bullet\frac{A10}{1024}\right)\times\left(\frac{B1}{2}+\frac{B2}{4}+\frac{B3}{8}+\bullet\bullet\bullet\frac{B10}{1024}\right)$$

where V_{REF} can be an AC signal

FIGURE 6. Precision Analog-to-Digital Multiplier

Typical Applications (Continued)



TL/H/5689–5

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \bullet\bullet\bullet + \frac{A10}{1024} - \frac{1}{1024}\right)$$

where: $AN = +1$ if A_N input is high

$AN = -1$ if A_N input is low

COMPLEMENTARY OFFSET BINARY (BIPOLAR) OPERATION

DIGITAL INPUT	V_{OUT}
0 0 0 0 0 0 0 0 0 0	$+V_{REF}$
0 0 0 0 0 0 0 0 0 1	$V_{REF} \times 1022/1024$
0 1 1 1 1 1 1 1 1 1	$V_{REF} \times 2/1024$
1 0 0 0 0 0 0 0 0 0	0
1 0 0 0 0 0 0 0 0 1	$-V_{REF} \times 2/1024$
1 1 1 1 1 1 1 1 1 1	$-V_{REF}$ (1022/1024)

Note that:

- $I_{OUT\,1} + I_{OUT\,2} = \frac{V_{REF}}{R_{LADDER}} \times \left(\frac{1023}{1024}\right)$
- By doubling the output range we get half the resolution
- The 10M resistor, adds a 1 LSB "thump", to allow full offset binary operation where the output reaches zero for the half-scale code. If symmetrical output excursions are required, omit the 10M resistor.

FIGURE 7. Bipolar 4-Quadrant Multiplying Configuration

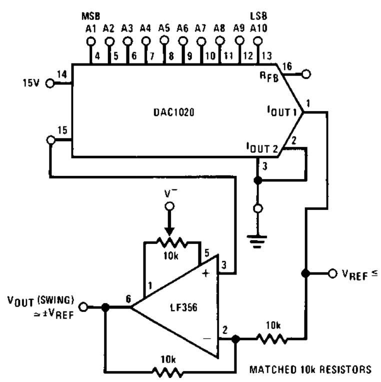
Operational Amplifiers V_{OS} Adjust (*Figure 7*)

a) Switch all the digital inputs high; adjust the V_{OS} potentiometer of op amp B to bring its output to a value equal to $-(V_{REF}/1024)$ (V).

b) Switch the MSB high and the remaining digital inputs low. Adjust the V_{OS} potentiometer of op amp A, to bring its output value to within a 1 mV from ground potential. For $V_{REF} < 10V$, a finer adjust is necessary, as already mentioned in the previous application.

Gain Adjust (Full-Scale Adjust)

Assuming that the external 10k resistors are matched to better than 0.1%, the gain adjust of the circuit is the same with the one previously discussed.



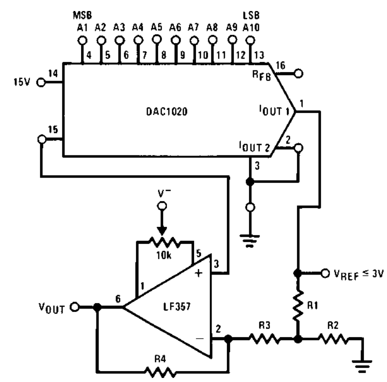
TRUE OFFSET BINARY OPERATION

DIGITAL INPUT	V_{OUT}
1 1 1 1 1 1 1 1 1 1	$V_{REF} \times 1022/1024$
1 0 0 0 0 0 0 0 0 0	0
0 0 0 0 0 0 0 0 0 0	$-V_{REF}$

$t_s = 1.8\ \mu s$

use LM336 for a voltage reference

FIGURE 8. Bipolar Configuration with a Single Op Amp



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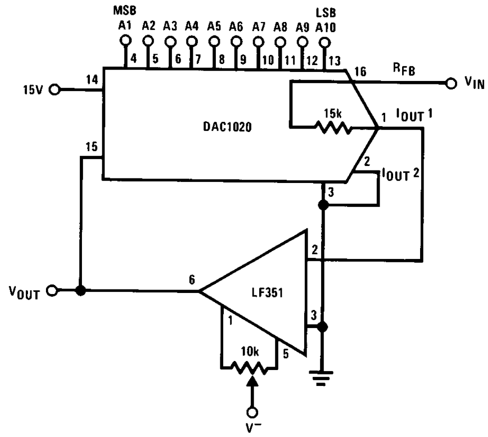
- $R4 = (2A_V^- - 1)\,R, \frac{R2}{R1} = \frac{A_V^-}{A_V^- - 1},$

  $R3 + R1 \| R2 = R;\ A_V^- = \frac{V_{OUT(PEAK)}}{V_{REF}}, R = 20k$

- Example: $V_{REF} = 2V$, V_{OUT} (swing) $\cong \pm 10V$: $A_V^- = 5V$
  Then $R4 = 9R$, $R1 = 0.8\ R2$. If $R1 = 0.2R$ then $R2 = 0.25R$, $R3 = 0.64R$

FIGURE 9. Bipolar Configuration with Increased Output Swing

Typical Applications (Continued)

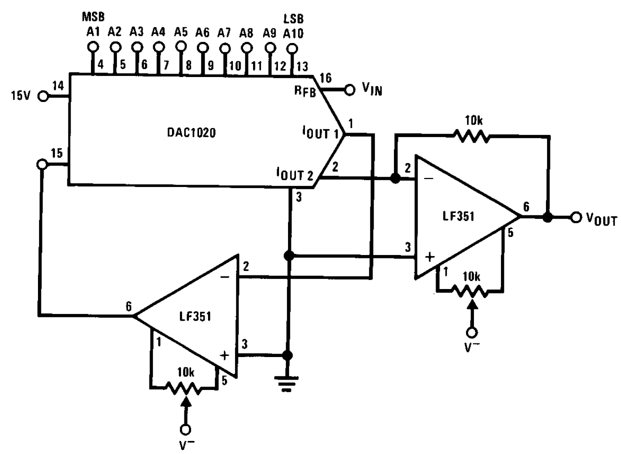


$$V_{OUT} = \frac{-V_{REF}}{\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)}$$

where: V_{REF} can be an AC signal

- By connecting the DAC in the feedback loop of an operational amplifier a linear digitally control gain block can be realized
- Note that with all digital inputs low, the gain of the amplifier is infinity, that is, the op amp will saturate. In other words, we cannot divide the V_{REF} by zero!

FIGURE 10. Analog-to-Digital Divider (or Digitally Gain Controlled Amplifier)



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$$V_{OUT} = V_{REF}\left[\frac{\frac{\overline{A1}}{2} + \frac{\overline{A2}}{4} + \ldots + \frac{\overline{A10}}{1024}}{\frac{A1}{2} + \frac{A2}{4} + \ldots + \frac{A10}{1024}}\right] \text{ or } V_{OUT} = V_{REF}\left(\frac{1023 - N}{N}\right)$$

where: $0 \leq N \leq 1023$

$N = 0$ for A_N = all zeros

$N = 1$ for $A10 = 1$, $A1-A9 = 0$

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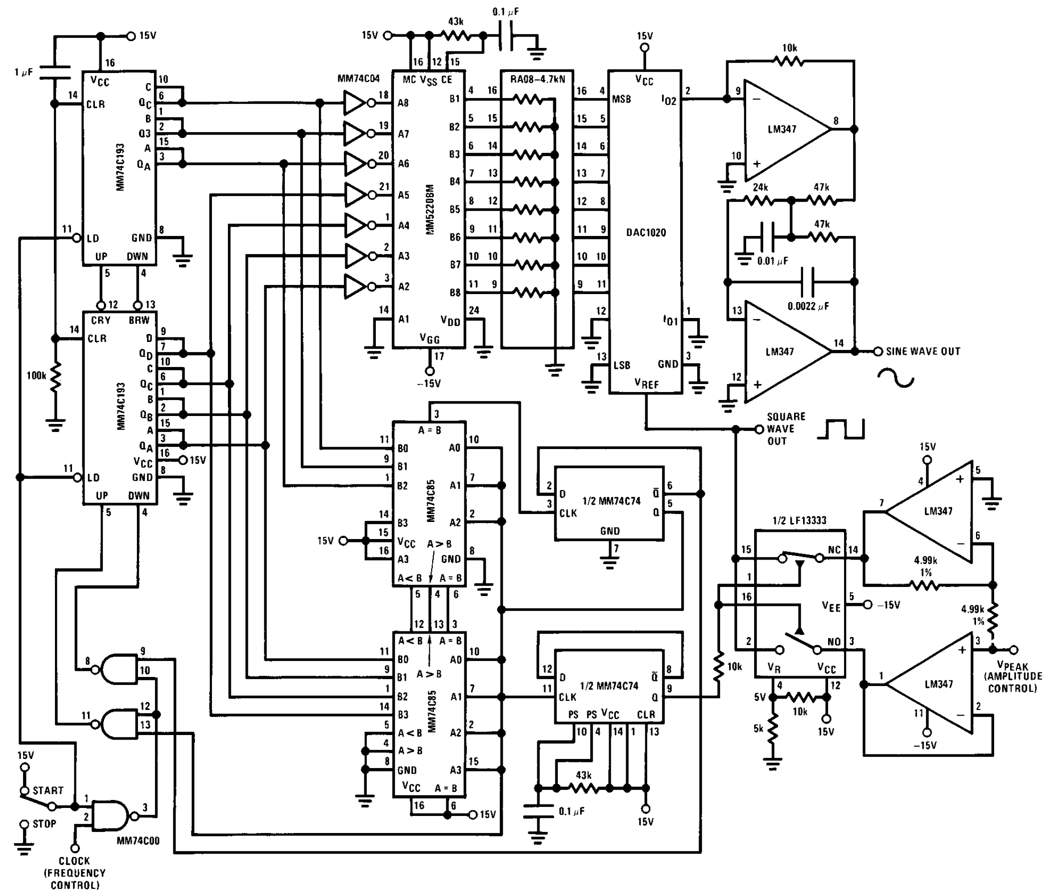
$N = 1023$ for A_N = all 1's

FIGURE 11. Digitally controlled Amplifier-Attenuator

Typical Applications (Continued)

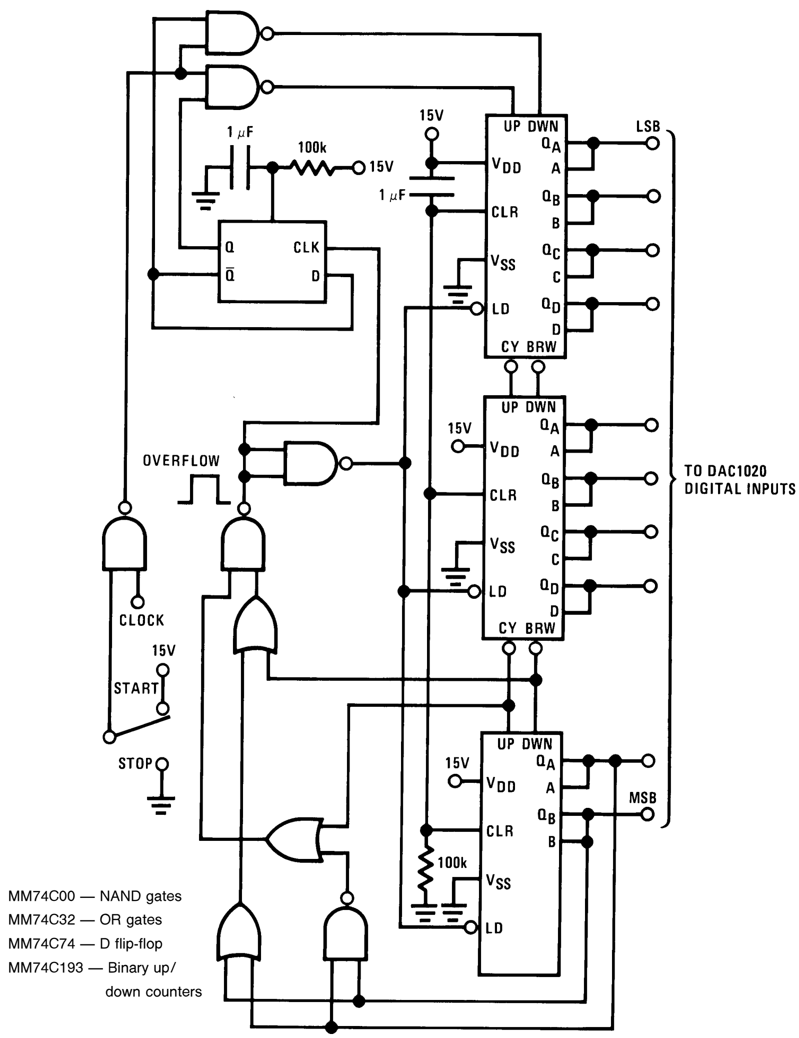


TL/H/5689–8

- Output frequency $= \frac{f_{CLK}}{512}$; $f_{MAX} \cong 2$ kHz
- Output voltage range = 0V − 10V peak
- THD < 0.2%
- Excellent amplitude and frequency stability with temperature
- Low pass filter shown has a 1 kHz corner (for output frequencies below 10 Hz, filter corner should be reduced)
- Any periodic function can be implemented by modifying the contents of the look up table ROM
- No start up problems

FIGURE 12. Precision Low Frequency Sine Wave Oscillator Using Sine Look-Up ROM

Typical Applications (Continued)



TL/H/5689–9

- Binary up/down counter digitally "ramps" the DAC output
- Can stop counting at any desired 10-bit input code
- Senses up or down count overflow and automatically reverses direction of count

FIGURE 13. A Useful Digital Input Code Generator for DAC Attenuator or Amplifier Circuits

Definition of Terms

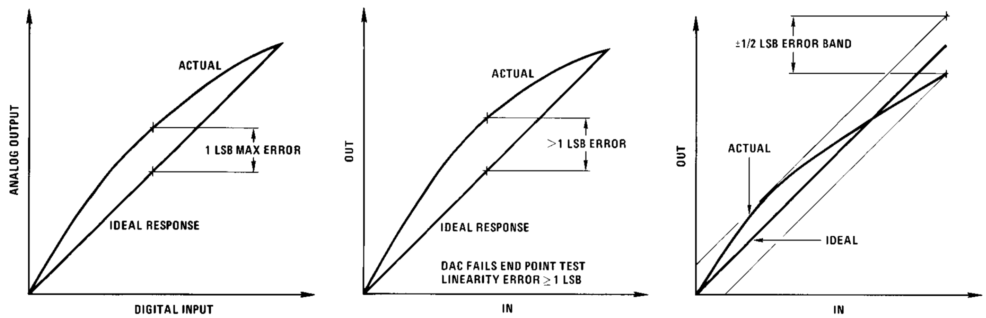
Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the D/A output. It is directly related to the number of switches or bits within the D/A. For example, the DAC1020 has 2^{10} or 1024 steps while the DAC1220 has 2^{12} or 4096 steps. Therefore, the DAC1020 has 10-bit resolution, while the DAC1220 has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from *a straight line passing through the endpoints of the D/A transfer characteristic.* It is measured after calibrating for zero (see V_{OS} adjust in typical applications) and full-scale. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time: Full-scale settling time requires a zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the D/A output reaches within $\pm 1/2$ LSB of final output value.

Full-Scale Error: Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1020 full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 9.8\ mV = 9.9902V$. Full-scale error is adjustable to zero as shown in *Figure 5*.



TL/H/5689–10

a **b1** **b2**

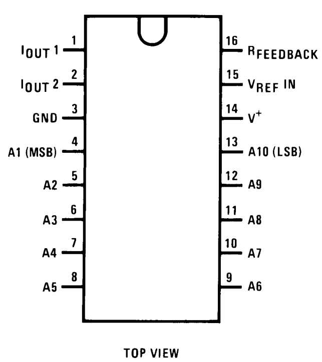
(a) End point test after zero and full-scale adjust. The DAC has 1 LSB linearity error.

(b) By shifting the full-scale calibration on of the DAC of *Figure (b1)* we could pass the "best straight line" (b2) test and meet the $\pm 1/2$ linearity error specification.

Note. (a), (b1) and (b2) above illustrate the difference between "end point" National's linearity test (a) and "best straight line" test. Note that both devices in (a) and (b2) meet the $\pm 1/2$ LSB linearity error specification but the end point test is a more "real life" way of characterizing the DAC.

Connection Diagrams

DAC102X
Dual-In-Line Package



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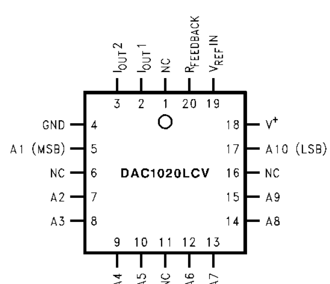
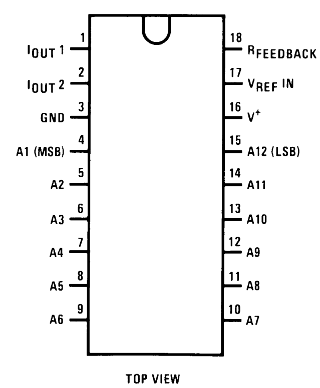
DAC1020
PLCC Package



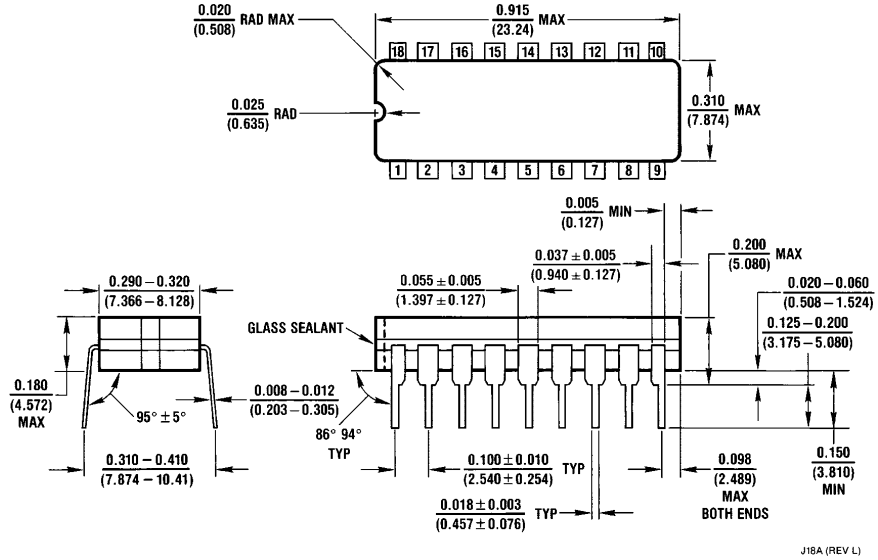
TL/H/5689–12

DAC122X
Dual-In-Line Package

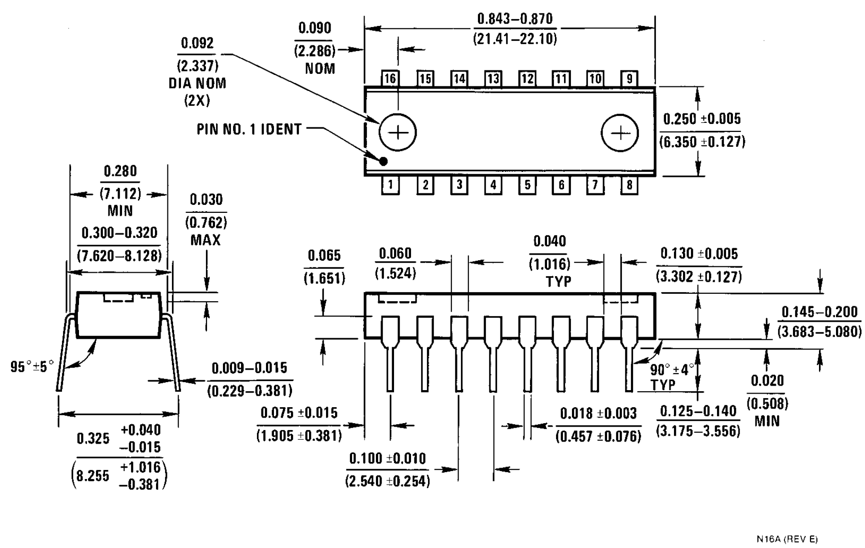


TL/H/5689–11

Physical Dimensions inches (millimeters) unless otherwise noted

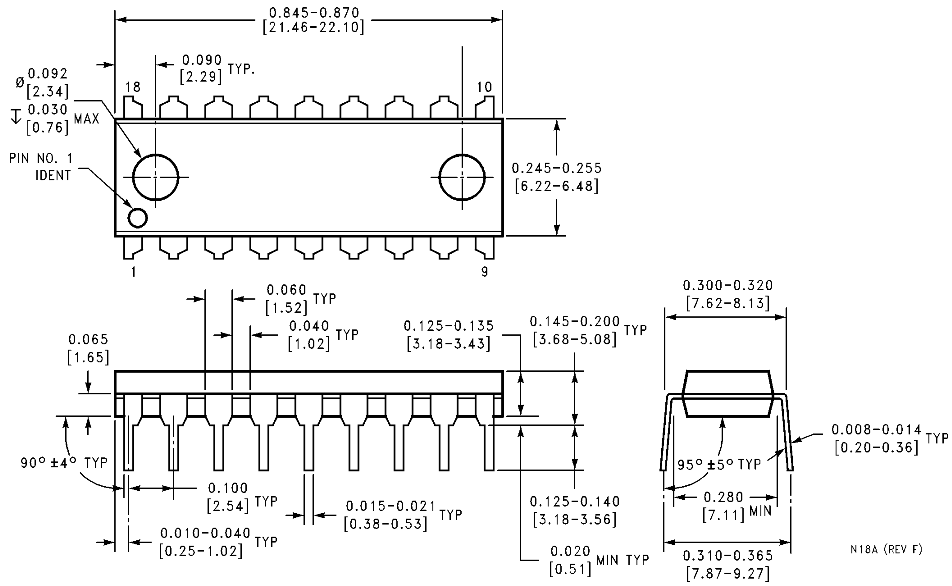


Cavity Dual-In-Line Package (J)
Order Number DAC1220LCJ or DAC1222LCJ
NS Package Number J18A



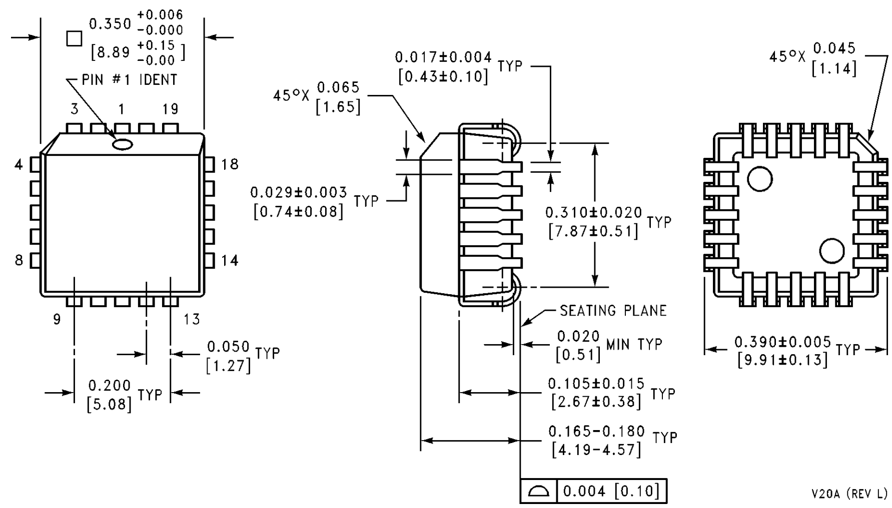
Molded Dual-In-Line Package (N)
Order Number DAC1020LCN, DAC1021LCN or DAC1022LCN
NS Package Number N16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number DAC1220LCN, DAC1221LCN or DAC1222LCN
NS Package Number N18A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Plastic Leaded Chip Carrier (V)
Order Number DAC1020LCV or DAC1020LIV
NS Package Number V20A

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408