

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4019B**

## **MSI**

## **Quadruple 2-input multiplexer**

Product specification  
File under Integrated Circuits, IC04

January 1995

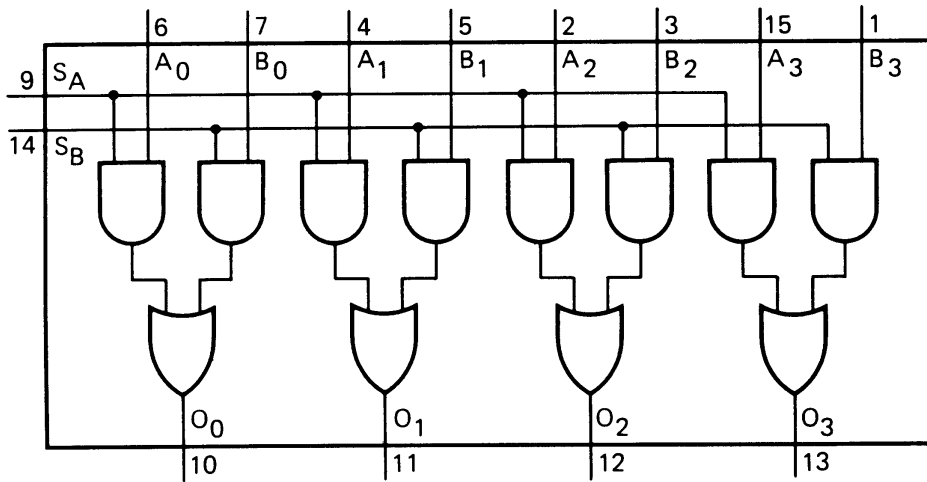
# Quadruple 2-input multiplexer

## HEF4019B MSI

### DESCRIPTION

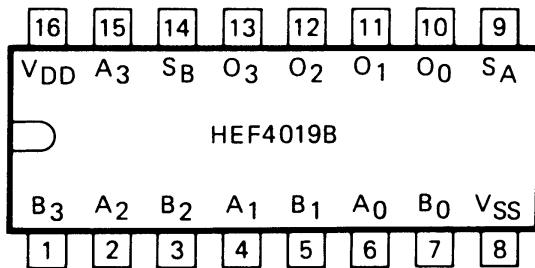
The HEF4019B provides four multiplexing circuits with common select inputs ( $S_A$ ,  $S_B$ ); each circuit contains two inputs ( $A_n$ ,  $B_n$ ) and one output ( $O_n$ ). It may be used to select four bits of information from one of two sources.

The A inputs are selected when  $S_A$  is HIGH, the B inputs when  $S_B$  is HIGH. When  $S_A$  and  $S_B$  are HIGH, output ( $O_n$ ) is the logical OR of the  $A_n$  and  $B_n$  inputs ( $O_n = A_n + B_n$ ). When  $S_A$  and  $S_B$  are LOW, output ( $O_n$ ) is LOW independent of the multiplexer inputs.



7Z69542.3

Fig.1 Functional diagram.



7Z69487.1

Fig.2 Pinning diagram.

- HEF4019BP(N): 16-lead DIL; plastic (SOT38-1)
  - HEF4019BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
  - HEF4019BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

### PINNING

- $S_A$ ,  $S_B$  select inputs (active HIGH)
- $A_0$  to  $A_3$  multiplexer inputs
- $B_0$  to  $B_3$  multiplexer inputs
- $O_0$  to  $O_3$  multiplexer outputs

### FAMILY DATA, $I_{DD}$ LIMITS category MSI

See Family Specifications

Quadruple 2-input multiplexer

HEF4019B  
MSI

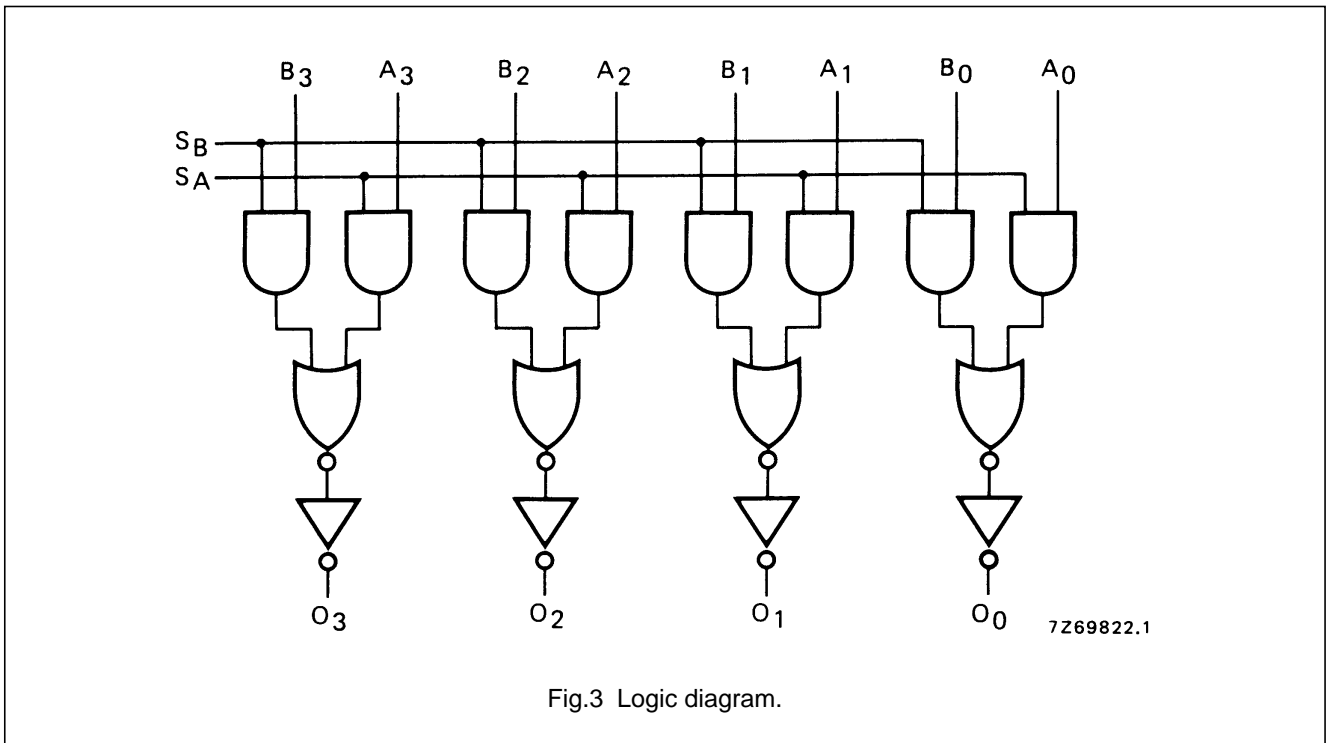


Fig.3 Logic diagram.

TRUTH TABLE

SELECT		INPUTS		OUTPUT
S <sub>A</sub>	S <sub>B</sub>	A <sub>n</sub>	B <sub>n</sub>	O <sub>n</sub>
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

Notes

1. H = HIGH state (the more positive voltage)  
 L = LOW state (the less positive voltage)  
 X = state is immaterial

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### AC CHARACTERISTICS

$V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $A_n, B_n, S_A, S_B \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	70	145	ns	43 ns + (0,55 ns/pF) $C_L$	
	10		30	60	ns	19 ns + (0,23 ns/pF) $C_L$	
	15		25	50	ns	17 ns + (0,16 ns/pF) $C_L$	
	LOW to HIGH	5	$t_{PLH}$	60	130	ns	33 ns + (0,55 ns/pF) $C_L$
		10		25	50	ns	14 ns + (0,23 ns/pF) $C_L$
		15		15	35	ns	7 ns + (0,16 ns/pF) $C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120	ns	10 ns + (1,0 ns/pF) $C_L$	
	10		30	60	ns	9 ns + (0,42 ns/pF) $C_L$	
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$	
	LOW to HIGH	5	$t_{TLH}$	60	120	ns	10 ns + (1,0 ns/pF) $C_L$
		10		30	60	ns	9 ns + (0,42 ns/pF) $C_L$
		15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P)	5	$1200 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$5100 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$18\ 700 f_i + \sum (f_o C_L) \times V_{DD}^2$	

### APPLICATION INFORMATION

An example of an application for the HEF4019B is:

- True/complement selection.

This datasheet has been download from:

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

Datasheets for electronics components.