

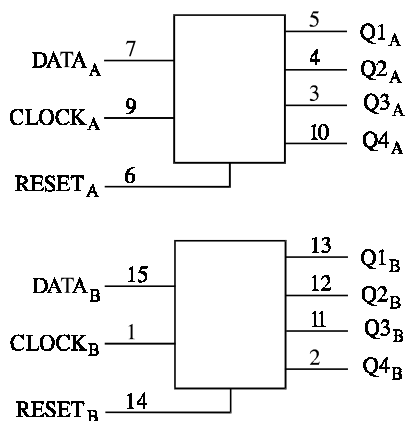
IW4015B

Dual 4-Stage Static Shift Register High-Voltage Silicon-Gate CMOS

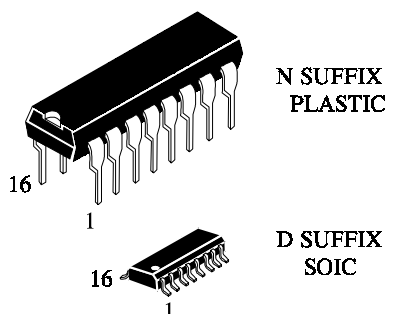
The IW4015B consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one IW4015B package, or to more than 8 stages using additional IW4015B's is possible.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND



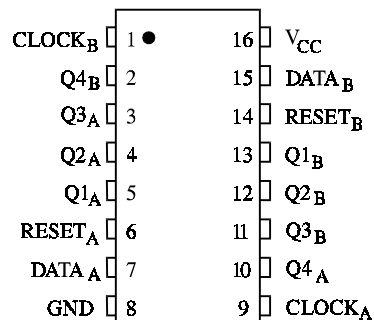
ORDERING INFORMATION

IW4015BN Plastic

IW4015BD SOIC

$T_A = -55^\circ$ to 125° C for all packages

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
Clock	Data	Reset	Q1	Q _n
	L	L	L	Q _{n-1}
	H	L	H	Q _{n-1}
	X	L	No change	
X	X	H	L	L

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).
Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V	5.0	3.5	3.5	3.5	V
		V _{OUT} = 1.0 V or V _{CC} - 1.0 V	10	7	7	7	
		V _{OUT} = 1.5 V or V _{CC} - 1.5V	15	11	11	11	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V	5.0	1.5	1.5	1.5	V
		V _{OUT} = 1.0 V or V _{CC} - 1.0 V	10	3	3	3	
		V _{OUT} = 1.5 V or V _{CC} - 1.5V	15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	5	5	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC}					mA
		U _{OL} =0.4 V	5.0	0.64	0.51	0.36	
		U _{OL} =0.5 V	10	1.6	1.3	0.9	
I _{OH}	Minimum Output High (Source) Current	U _{OL} =1.5 V	15	4.2	3.4	2.4	mA
		V _{IN} = GND or V _{CC}					
		U _{OH} =2.5 V	5.0	-2	-1.6	-1.15	
		U _{OH} =4.6 V	5.0	-0.64	-0.51	-0.36	
		U _{OH} =9.5 V	10	-1.6	-1.3	-0.9	
		U _{OH} =13.5 V	15	-4.2	-3.4	-2.4	

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
$t_{\max}$	Maximum Clock Frequency (Figure 1)	5.0 10 15	3 6 8.5	3 6 8.5	1.5 3 4.25	MHz
$t_{\text{PHL}}, t_{\text{PLH}}$	Maximum Propagation Delay, Clock to Q (Figure 1)	5.0 10 15	320 160 120	320 160 120	640 320 240	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figure 2)	5.0 10 15	400 200 160	400 200 160	800 400 320	ns
$t_{\text{THL}}, t_{\text{TLH}}$	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS($C_L=50\text{pF}$, $R_L=200\text{ k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	180 80 50	180 80 50	360 160 100	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	5.0 10 15	200 80 60	200 80 60	400 160 120	ns
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	5.0 10 15	70 40 30	70 40 30	140 80 60	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	5.0 10 15	0 0 0	0 0 0	0 0 0	ns
t_r, t_f	Maximum Input Rise and Fall Time (Figure 1)	5.0 10 15	15 6 2	15 6 2	30 12 4	μs

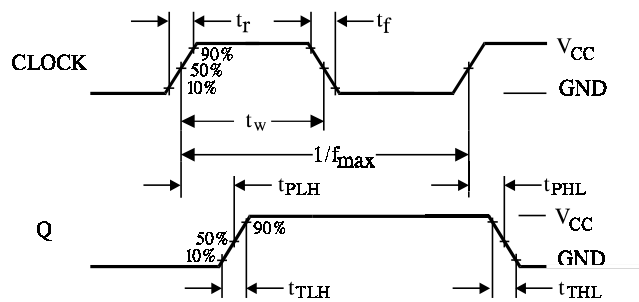


Figure 1. Switching Waveforms

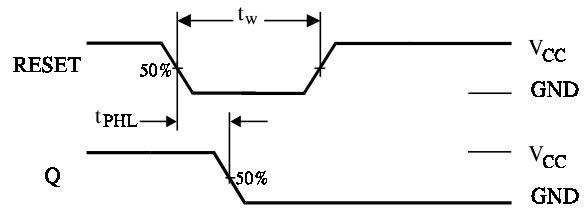


Figure 2. Switching Waveforms

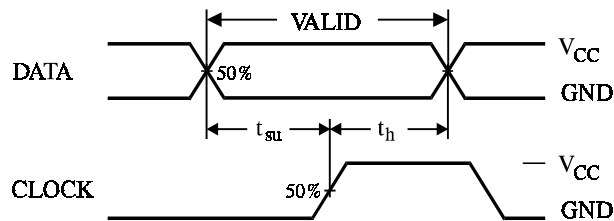


Figure 3. Switching Waveforms

EXPANDED LOGIC DIAGRAM (1/2 of the Device)

