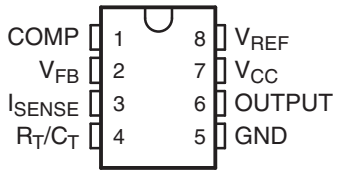
CURRENT-MODE PWM CONTROLLER

FEATURES

- **Qualified for Automotive Applications**
- **Extended Temperature Performance of –40°C to 125°C**
- **Optimized for Off-Line and DC-to-DC Converters**
- **Low Start-Up Current (<0.5 mA)**
- **Trimmed Oscillator-Discharge Current**
- **Automatic Feed-Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load-Response Characteristics**
- **Under-Voltage Lockout With Hysteresis**
- **Double-Pulse Suppression**
- **High-Current Totem-Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500-kHz Operation**
- **Low R_O Error Amp**

D PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The UC2843A control IC is a pin-for-pin compatible improved version of the UC2843. Providing the necessary features to control current mode switched mode power supplies, this device has the following improved features. Start up current is specified to be less than 0.5 mA. Oscillator discharge is trimmed to 8.3 mA. During undervoltage lockout, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

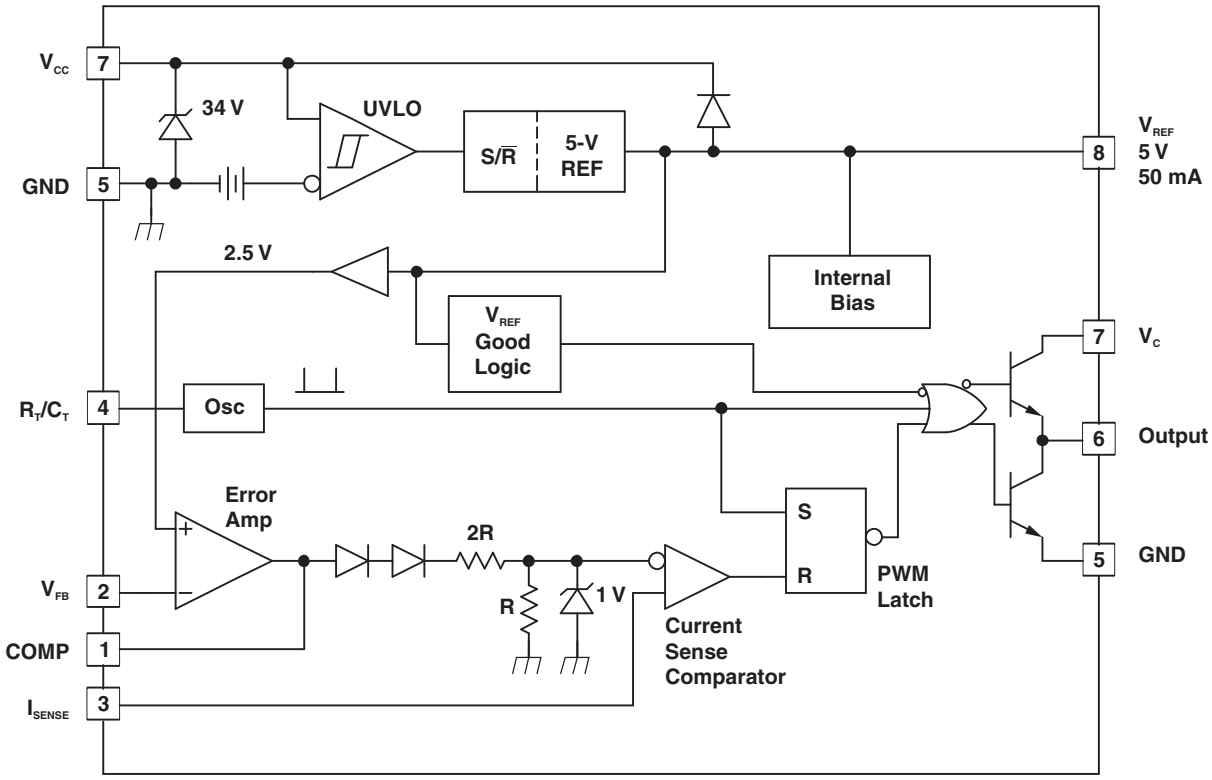
PART NUMBER	UVLO ON	UVLO OFF	MAXIMUM DUTY CYCLE
UC2843A	8.5 V	7.9 V	<100%

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC-8 – D8	Reel of 2500	UC2843AQD8RQ1	UC2843AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	V_{CC} voltage (low impedance source)	30	V
	V_{CC} voltage (I_{CC} mA)	Self limiting	
I_O	Output current	±1	A
	Output energy (capacitive load)	5	µJ
	Analog inputs (pins 3 and 5)	–0.3 to 6.3	V
	Error amplifier output sink current	10	mA
	Power dissipation at T_A < 25°C (14-pin D package)	1	W
θ_{JA}	Package thermal impedance(3)	97	°C/W
T_{stg}	Storage temperature range	–65 to 150	°C
	Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Unless otherwise indicated, voltages are reference to ground, and currents are positive into and negative out of the specified terminals.
(3) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 125°C, V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reference Section						
Output voltage	T_J = 25°C, I_O = 1 mA		4.95	5.0	5.05	V
Line regulation voltage	V_{IN} = 12 V to 25 V			6	20	mV
Load regulation voltage	I_O = 1 mA to 20 mA			6	25	mV
Temperature stability(2)(3)				0.2	0.4	mV/°C
Total output variation voltage	Line, load, temperature		4.9		5.1	V
Output noise voltage	f = 10 Hz to 10 kHz	T_J = 25°C		50		μV
Long term stability	1000 hours	T_A = 125°C		5	25	mV
Output short-circuit current			–30	–100	–180	mA
Oscillator Section						
Initial accuracy(4)		T_J = 25°C	47	52	57	kHz
Voltage stability	V_{CC} = 12 V to 25 V			0.2	1	%
Temperature stability	T_A = MIN to MAX			5		%
Amplitude peak-to-peak	V pin 7			1.7		V
Discharge current(5)	V pin 7 = 2 V	T_J = 25°C	7.8	8.3	8.8	mA
		T_J = Full range	7.5		8.8	
Error Amplifier Section						
Input voltage	COMP = 2.5 V		2.45	2.5	2.55	V
Input bias current				–0.3	–1	μA
Open loop voltage gain (AVOL)	V_O = 2 V to 4 V		65	90		dB
Unity gain bandwidth(3)		T_J = 25°C	0.7	1		MHz
PSRR	V_{CC} = 12 V to 25 V		60	70		dB
Output sink current	FB = 2.7 V, COMP = 1.1 V		2	6		mA
Output source current	FB = 2.3 V, COMP = 5 V		–0.5	–0.8		mA
VOUT high	FB = 2.3 V, RL = 15 kΩ to GND		5	6		V
VOUT low	FB = 2.7 V, RL = 15 kΩ to V_{REF}			0.7	1.1	V
Current Sense Section						
Gain(6)(7)			2.85	3	3.15	V/V
Maximum input signal(6)	COMP = 5 V		0.9	1	1.1	V
PSRR(6)	V_{CC} = 12 V to 25 V			70		dB
Input bias current				–2	–10	μA
Delay to output(3)	I_{SENSE} = 0 V to 2 V			150	300	ns

(1) Adjust V_{CC} above the start threshold before setting at 15 V.
(2) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:
Temperature Stability = (V_{REF} (max) – V_{REF} (min))/(T_J (max) – T_J (min)). V_{REF} (max) and V_{REF} (min) are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(3) Specified by design.
(4) Output frequency equals oscillator frequency for the UC2843A.
(5) This parameter is measured with R_T = 10 kΩ to V_{REF}. This contributes approximately 300 μA of current to the measurement. The total current flowing into the R_T/R_C pin is approximately 300 μA higher than the measured value.
(6) Parameter measured at trip point of latch with V_{FB} at 0 V.
(7) Gain is defined by: A = $\Delta V_{COMP}/\Delta V_{SENSE}$; 0 ≤ V_{SENSE} ≤ 0.8 V.

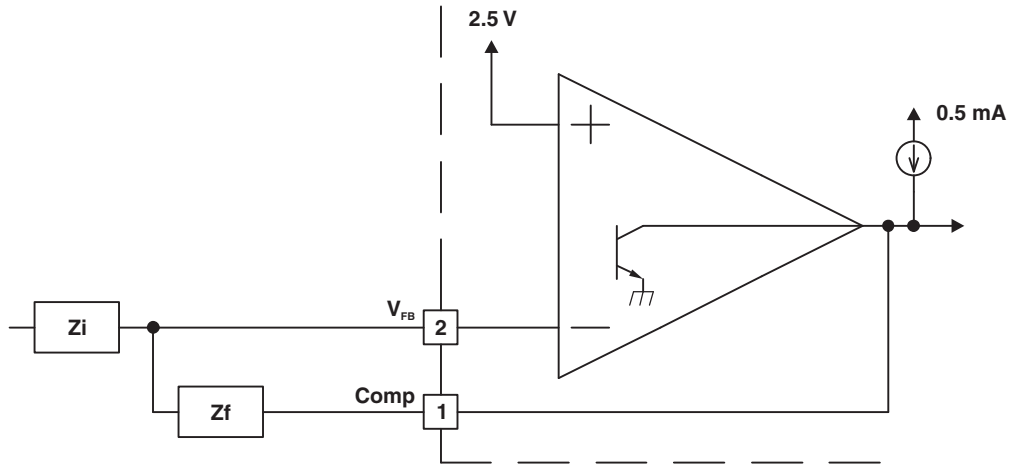
ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 125°C, V_{CC} = 15 V, R_T = 10 kΩ, C_T = 3.3 nF, T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Section (OUT)						
Low level output voltage	I_{OUT} = 20 mA			0.1	0.4	V
	I_{OUT} = 200 mA			15	2.2	
High level output voltage	I_{OUT} = –20 mA		13	13.5		V
	I_{OUT} = –200 mA		12	13.5		
Rise time[8]	C_L = 1 nF	T_J = 25°C		50	150	ns
Fall time[8]	C_L = 1 nF	T_J = 25°C		50	150	ns
UVLO saturation	V_{CC} = 5 V, I_{OUT} = 10 mA			0.7	1.2	V
Undervoltage Lockout Section (UVLO)						
Start threshold			7.8	8.4	9	V
Minimum operation voltage after turn on			7	7.6	8.2	V
PWM Section						
Maximum duty cycle			94	96	100	%
Minimum duty cycle					0	%
Total Standby Current						
Start-up current				0.3	0.5	mA
Operating supply current	FB = 0 V, SENSE = 0 V			11	17	mA
V_{CC} internal zener voltage	I_{CC} = 25 mA		30	34		V

(8) Specified by design.

PARAMETER MEASUREMENT INFORMATION



A. The error amplifier can source up to 0.5 mA and sink up to 2 mA.

Figure 1. Error Amp Configuration

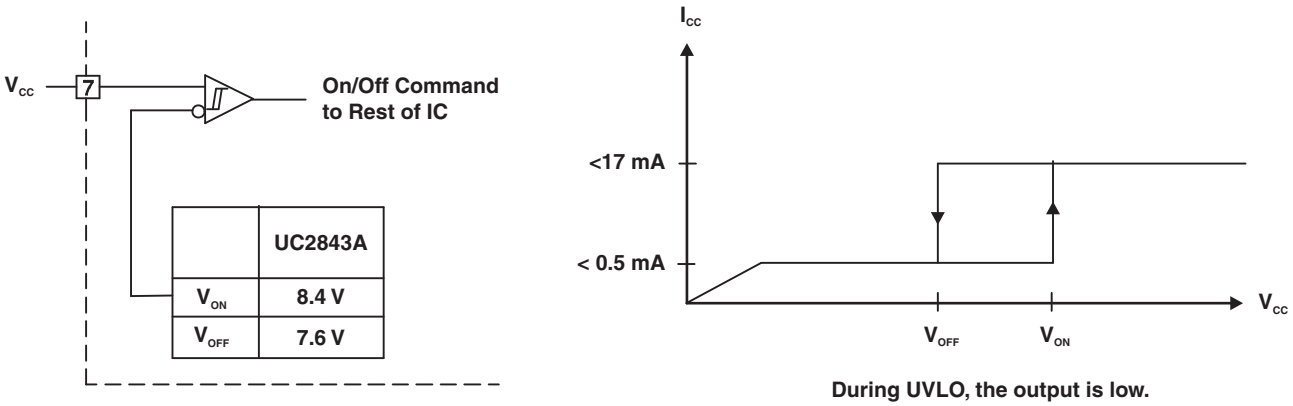
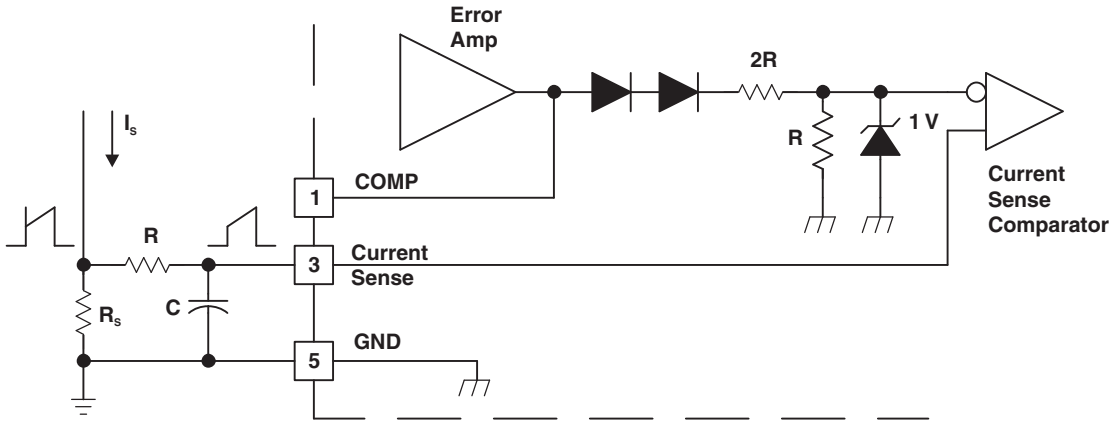


Figure 2. Undervoltage Lockout



A. Peak current (Is) is determined by the formula: Ismax = 1.0 V/R_S
A small RC filter may be required to supress switch transients.

Figure 3. Current Sense Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

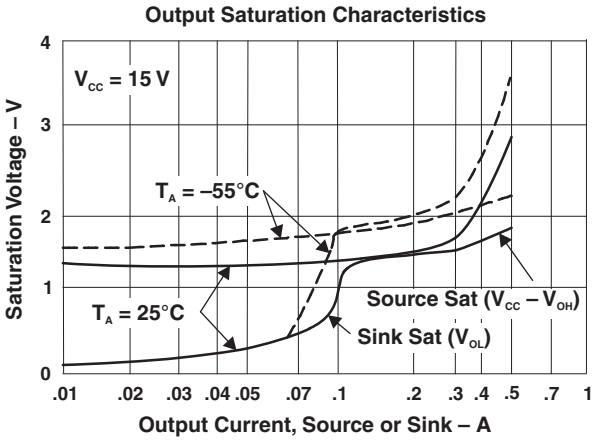


Figure 4.

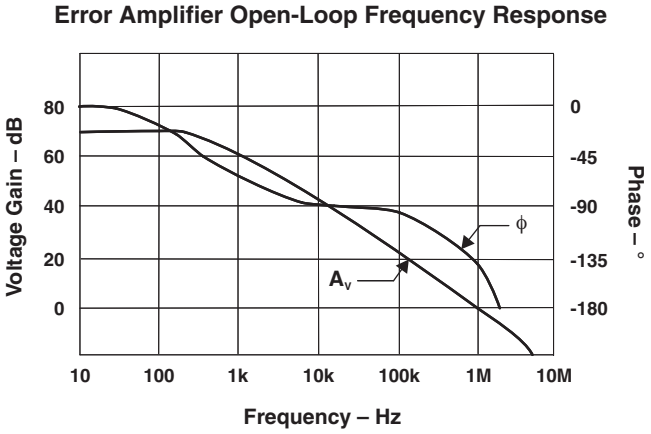


Figure 5.

APPLICATION INFORMATION

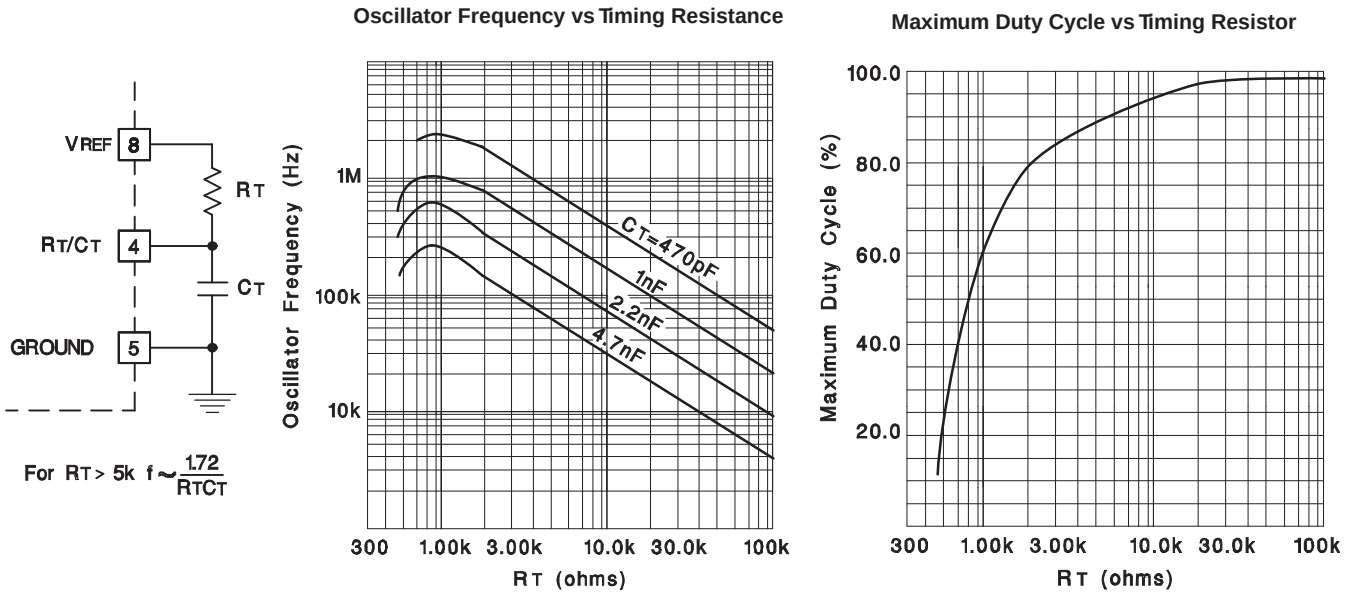
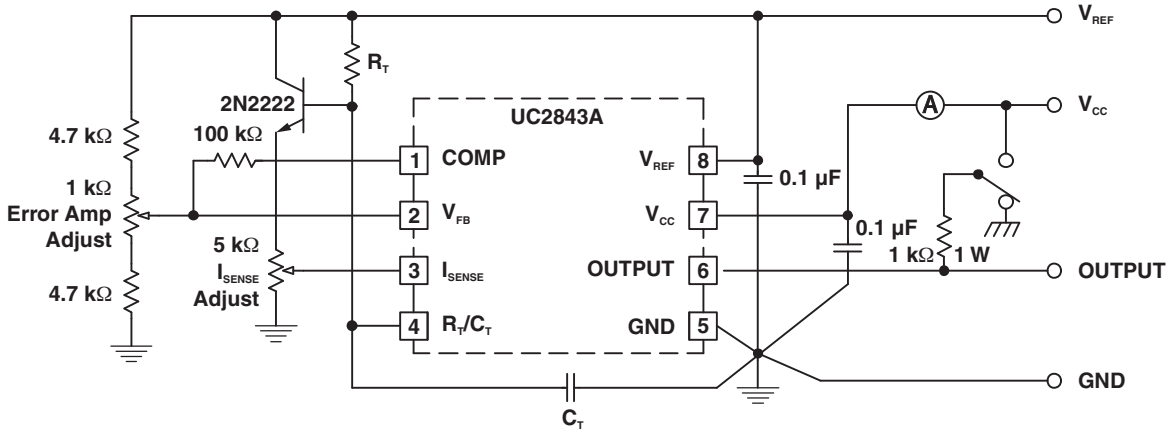
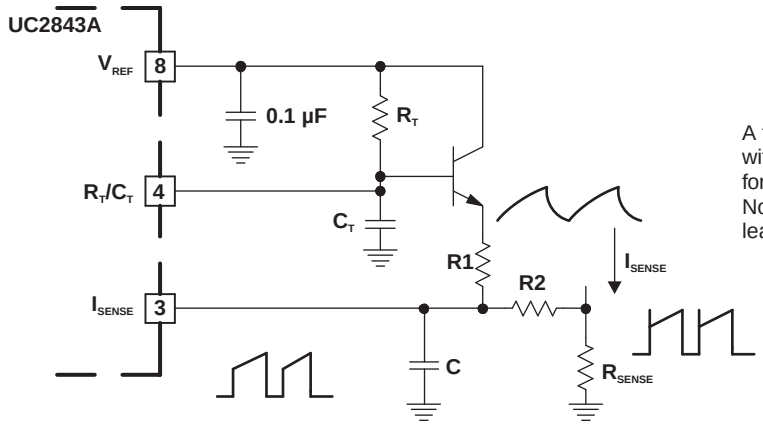


Figure 6. Oscillator



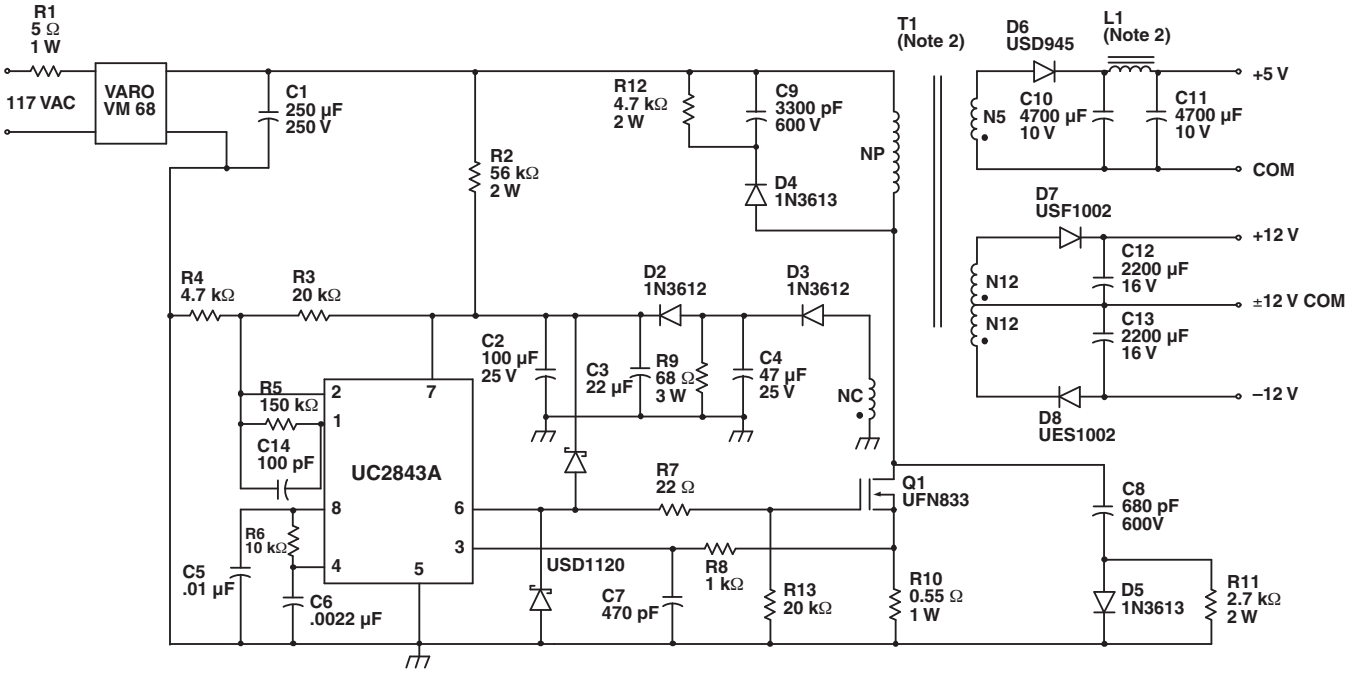
A. High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 7. Open-Loop Laboratory Text Fixture



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

Figure 8. Slope Compression



Power Supply Specifications

1. Input Voltage 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation 3750 V
3. Switching Frequency 40 kHz
4. Efficiency, Full Load 70%
5. Output Voltage:
   A. 5 V ±5%; 1-A to 4-A Load
   B. 12 V ±3%; 0.1-A to 0.3-A Load; Ripple voltage: 100 mV P-P Max
   C. -12 V ±3%; 0.1-A to 0.3-A Load; Ripple voltage: 100 mV P-P Max

Figure 9. Off-Line Flyback Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2843AQD8RQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2843AQ, UC2843AQ)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC2843A-Q1 :

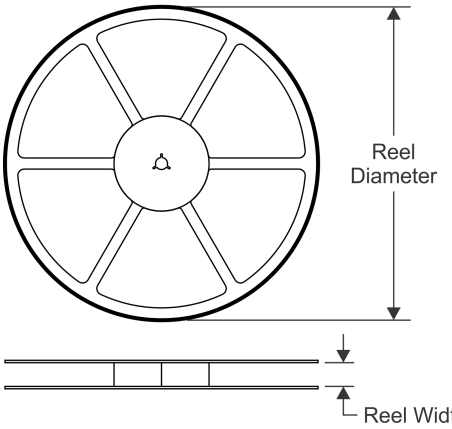
- Catalog: UC2843A

NOTE: Qualified Version Definitions:

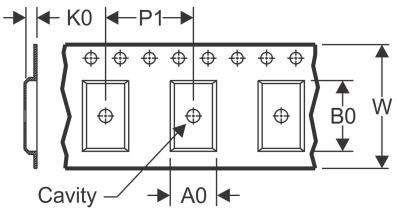
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

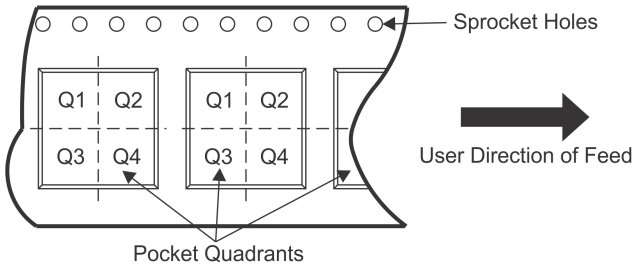


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

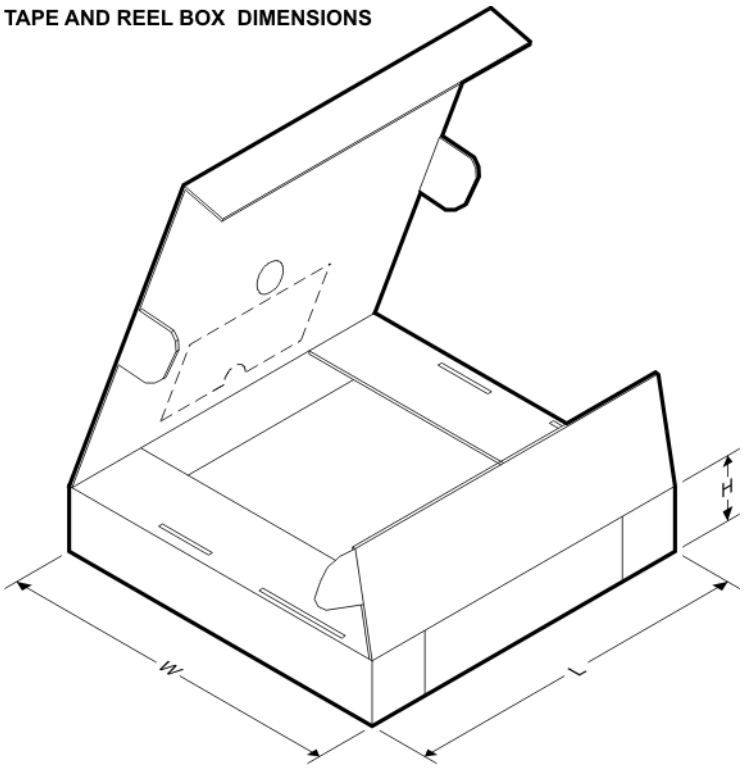
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

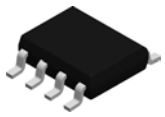
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2843AQD8RQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2843AQD8RQ1	SOIC	D	8	2500	367.0	367.0	35.0

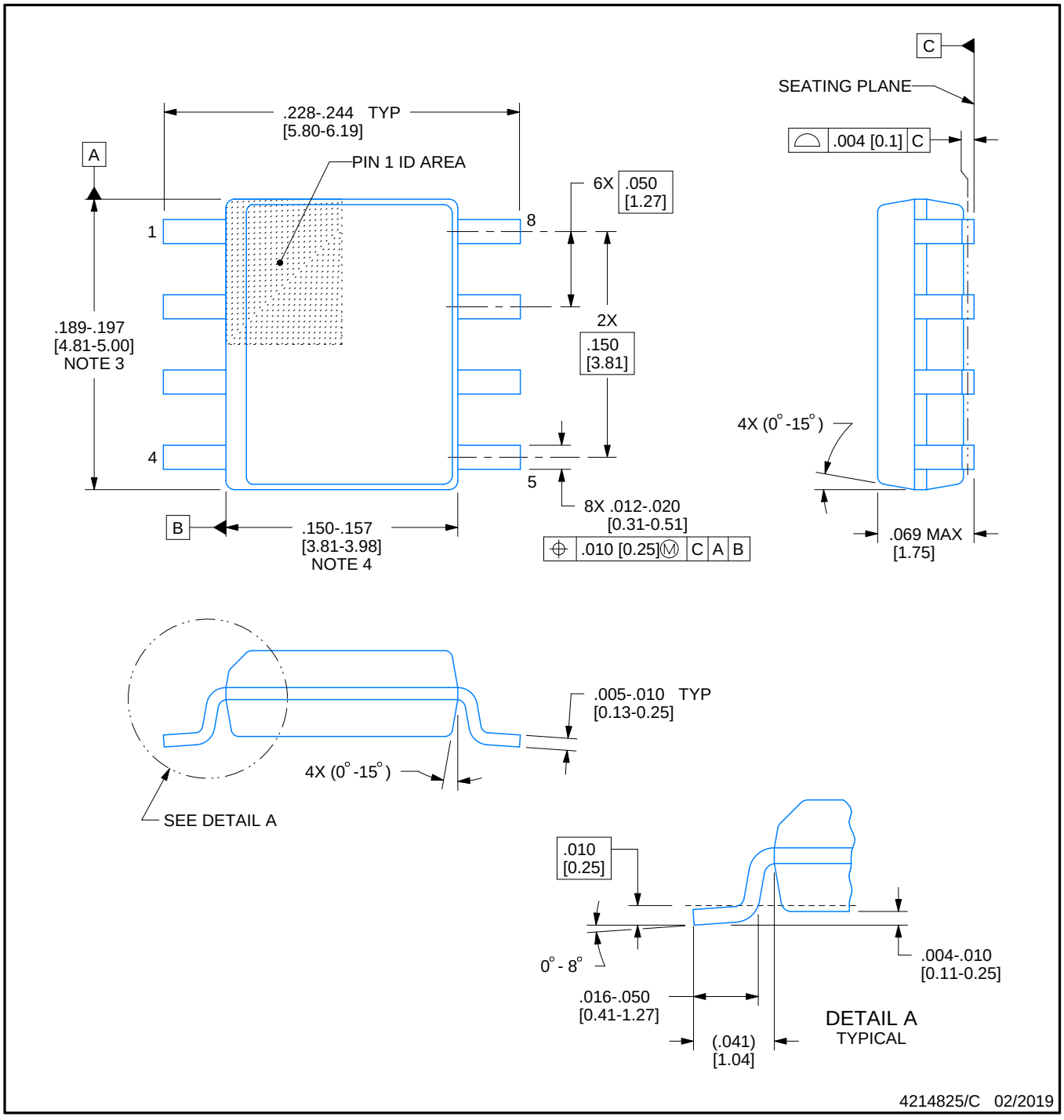


PACKAGE OUTLINE

D0008A

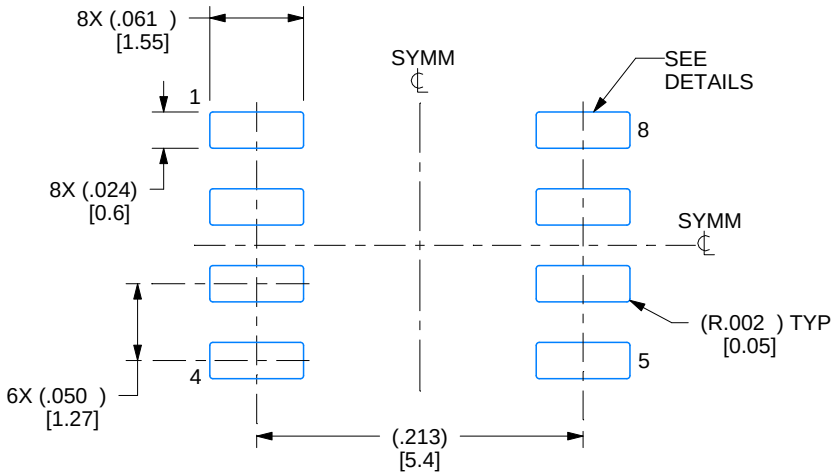
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

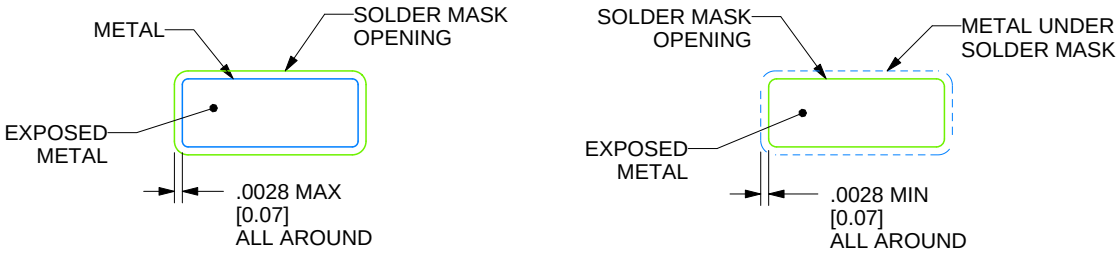


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

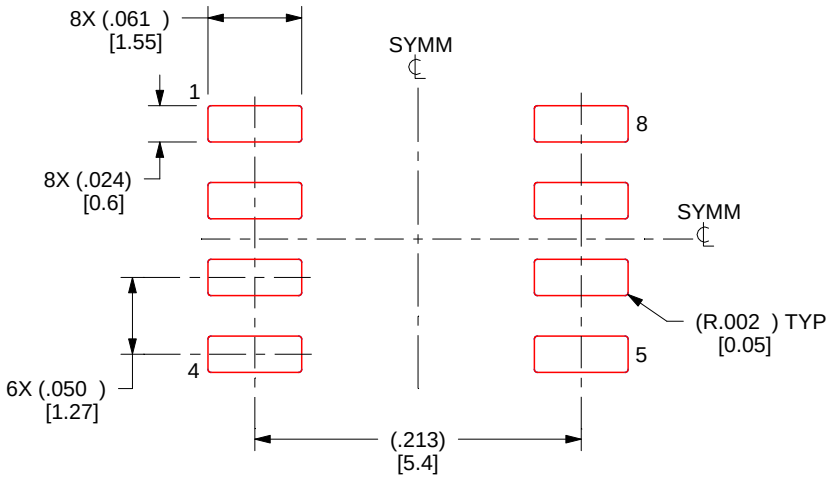
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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