

# Resonant-Mode Power Supply Controllers

## FEATURES

- Controls Zero Current Switched (ZCS) or Zero Voltage Switched (ZVS) Quasi-Resonant Converters
- Zero-Crossing Terminated One-Shot Timer
- Precision 1%, Soft-Started 5V Reference
- Programmable Restart Delay Following Fault
- Voltage-Controlled Oscillator (VCO) with Programmable Minimum and Maximum Frequencies from 10kHz to 1MHz
- Low Start-Up Current (150µA typical)
- Dual 1 Amp Peak FET Drivers
- UVLO Option for Off-Line or DC/DC Applications

## DESCRIPTION

The UC1861-1868 family of ICs is optimized for the control of Zero Current Switched and Zero Voltage Switched quasi-resonant converters. Differences between members of this device family result from the various combinations of UVLO thresholds and output options. Additionally, the one-shot pulse steering logic is configured to program either on-time for ZCS systems (UC1865-1868), or off-time for ZVS applications (UC1861-1864).

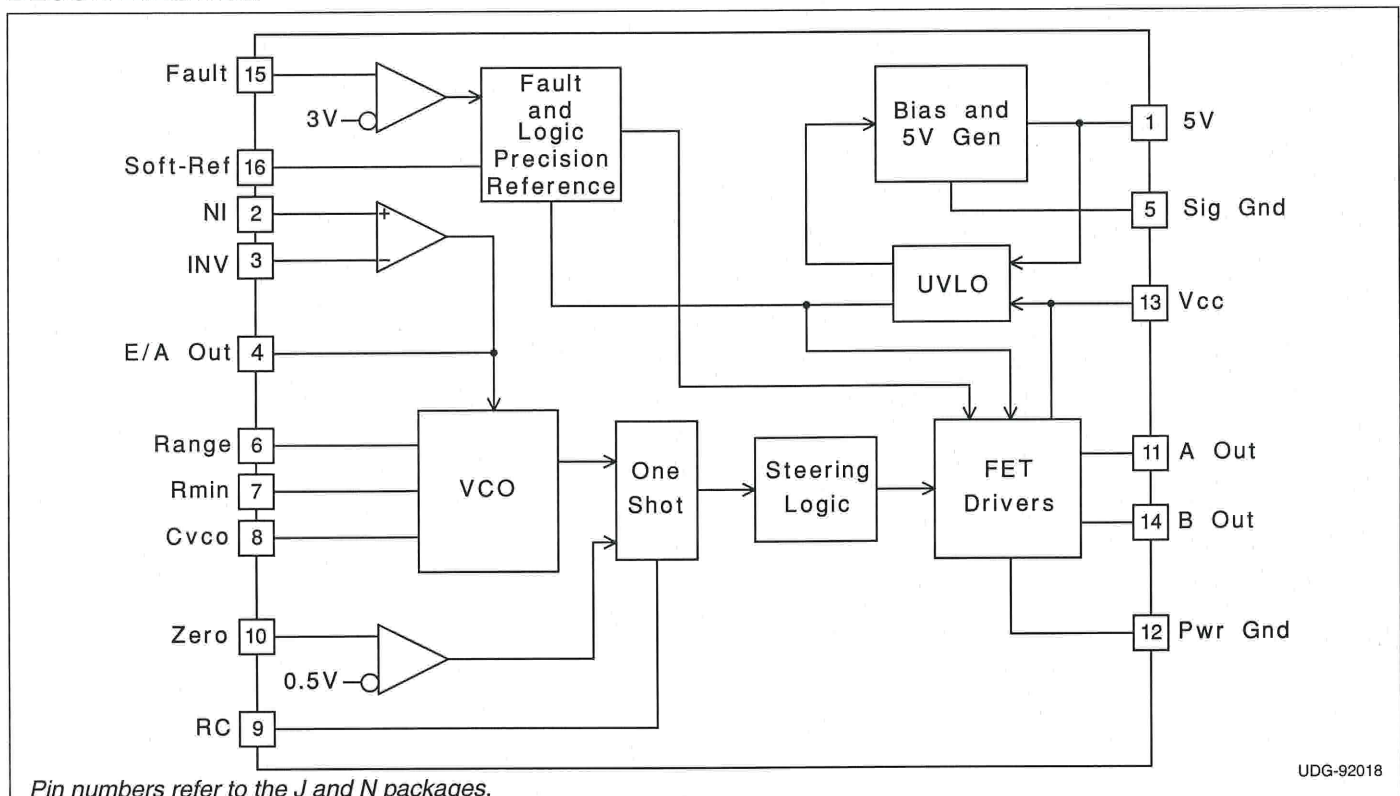
The primary control blocks implemented include an error amplifier to compensate the overall system loop and to drive a voltage controlled oscillator (VCO), featuring programmable minimum and maximum frequencies. Triggered by the VCO, the one-shot generates pulses of a programmed maximum width, which can be modulated by the Zero Detection comparator. This circuit facilitates "true" zero current or voltage switching over various line, load, and temperature changes, and is also able to accommodate the resonant components' initial tolerances.

Under-Voltage Lockout is incorporated to facilitate safe starts upon power-up. The supply current during the under-voltage lockout period is typically less than 150µA, and the outputs are actively forced to the low state.

(continued)

Device	1861	1862	1863	1864	1865	1866	1867	1868
UVLO	16.5/10.5	16.5/10.5	8/7	8/7	16.5/10.5	16.5/10.5	8/7	8/7
Outputs	Alternating	Parallel	Alternating	Parallel	Alternating	Parallel	Alternating	Parallel
"Fixed"	Off Time	Off Time	Off Time	Off Time	On Time	On Time	On Time	On Time

## BLOCK DIAGRAM



UDG-92018

**DESCRIPTION (cont.)**

UVLO thresholds for the UC1861/62/65/66 are 16.5V (ON) and 10.5V (OFF), whereas the UC1863/64/67/68 thresholds are 8V (ON) and 7V (OFF). After  $V_{CC}$  exceeds the UVLO threshold, a 5V generator is enabled which provides bias for the internal circuits and up to 10mA for external usage.

A Fault comparator serves to detect fault conditions and set a latch while forcing the output drivers low. The Soft-Ref pin serves three functions: providing soft start, restart

delay, and the internal system reference.

Each device features dual 1 Amp peak totem pole output drivers for direct interface to power MOSFETS. The outputs are programmed to alternate in the UC1861/63/65/67 devices. The UC1862/64/66/68 outputs operate in unison allowing a 2 Amp peak current.

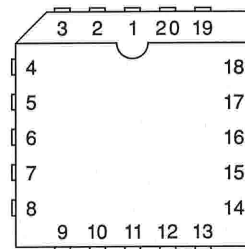
**ABSOLUTE MAXIMUM RATINGS**

$V_{CC}$ .....	22V
Output Current	
Source or Sink (Pins 11 & 14) .....	0.5A
DC Pulse (0.5 $\mu$ s) .....	1.5A
Power Ground Voltage .....	$\pm 0.2V$
Inputs (Pins 2, 3, 10, & 15) .....	-0.4 to 7V
Error Amp Output Current .....	$\pm 2mA$
Power Dissipation .....	1W
Junction Temperature (Operating) .....	150°C
Lead Temperature (Soldering, 10 seconds) .....	300°C

*All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the J and N packages. Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.*

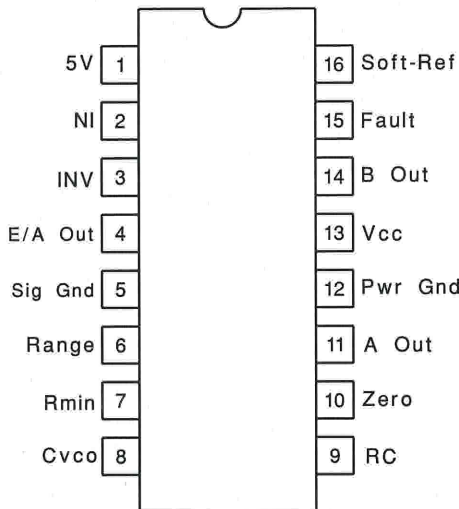
**CONNECTION DIAGRAMS**

**PLCC-20 & LCC-20 (Top View)  
 Q & L Package**



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Soft Ref	1
5V	2
NI	3
INV	4
E/A Out	5
Sig Gnd	6
Range	7
RMIN	8
Cvco	9
RC	10
Zero	11
NC	12
NC	13
A Out	14
Pwr Gnd	15
Pwr Gnd	16
Vcc	17
B Out	18
NC	19
Fault	20

**DIL-16, SOIC-16 (Top View)  
 J or N, DW Packages**



**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, all specifications apply for  $-55^{\circ}\text{C} \leq \text{T}_A \leq 125^{\circ}\text{C}$  for the UC186x,  $-25^{\circ}\text{C} \leq \text{T}_A \leq 85^{\circ}\text{C}$  for the UC286x, and  $0^{\circ}\text{C} \leq \text{T}_A \leq 70^{\circ}\text{C}$  for the UC386x,  $V_{\text{CC}}=12\text{V}$ ,  $C_{\text{VCO}}=1\text{nF}$ ,  $\text{Range}=7.15\text{k}$ ,  $R_{\text{MIN}}=86.6\text{k}$ ,  $C=200\text{pF}$ ,  $R=4.02\text{k}$ , and  $C_{\text{sr}}=0.1\mu\text{F}$ .  $\text{T}_A=\text{T}_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>5V Generator</b>					
Output Voltage	$12\text{V} \leq V_{\text{CC}} \leq 20\text{V}$ , $-10\text{mA} \leq I_{\text{O}} \leq 0\text{mA}$	4.8	5.0	5.2	V
Short Circuit Current	$V_{\text{O}} = 0\text{V}$	-150		-15	mA
<b>Soft-Reference</b>					
Restart Delay Current	$V = 2\text{V}$	10	20	35	$\mu\text{A}$
Soft Start Current	$V = 2\text{V}$	-650	-500	-350	$\mu\text{A}$
Reference Voltage	$\text{T}_J = 25^{\circ}\text{C}$ , $I_{\text{O}} = 0\text{A}$	4.95	5.00	5.05	V
	$12\text{V} \leq V_{\text{CC}} \leq 20\text{V}$ , $-200\mu\text{A} \leq I_{\text{O}} \leq 200\mu\text{A}$	4.85		5.15	V
Line Regulation	$12\text{V} \leq V_{\text{CC}} \leq 20\text{V}$		2	20	mV
Load Regulation	$-200\mu\text{A} \leq I_{\text{O}} \leq 200\mu\text{A}$		10	30	mV
<b>Error Amplifier (Note 3)</b>					
Input Offset Voltage	$V_{\text{CM}} = 5\text{V}$ , $V_{\text{O}} = 2\text{V}$ , $I_{\text{O}} = 0\text{A}$	-10		10	mV
Input Bias Current	$V_{\text{CM}} = 0\text{V}$	-2.0	-0.3		$\mu\text{A}$
Voltage Gain	$V_{\text{cm}} = 5\text{V}$ , $0.5\text{V} \leq V_{\text{O}} \leq 3.7\text{V}$ , $I_{\text{O}} = 0\text{A}$	70	100		dB
Power Supply Rejection Ratio	$V_{\text{cm}} = 5\text{V}$ , $V_{\text{O}} = 2\text{V}$ , $12\text{V} \leq V_{\text{CC}} \leq 20\text{V}$	70	100		dB
<b>Error Amplifier (Note 3) (cont.)</b>					
Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{cm}} \leq 6\text{V}$ , $V_{\text{O}} = 2\text{V}$	65	100		dB
V <sub>OUT</sub> Low	$V_{\text{ID}} = -100\text{mV}$ , $I_{\text{O}} = 200\mu\text{A}$		0.17	0.25	V
V <sub>OUT</sub> High	$V_{\text{ID}} = 100\text{mV}$ , $I_{\text{O}} = -200\mu\text{A}$	3.9	4.2		V
Unity Gain Bandwidth	(Note 4)	0.5	0.8		MHz
<b>Voltage Controlled Oscillator</b>					
Maximum Frequency	$V_{\text{ID}} (\text{Error Amp}) = 100\text{mV}$ , $\text{T}_J = 25^{\circ}\text{C}$	450	500	550	kHz
	$V_{\text{ID}} (\text{Error Amp}) = 100\text{mV}$	425		575	kHz
Minimum Frequency	$V_{\text{ID}} (\text{Error Amp}) = -100\text{mV}$ , $\text{T}_J = 25^{\circ}\text{C}$	45	50	55	kHz
	$V_{\text{ID}} (\text{Error Amp}) = -100\text{mV}$	42		58	kHz
<b>One Shot</b>					
Zero Comparator V <sub>th</sub>		0.45	0.50	0.55	V
Propagation Delay	(Note 4)		120	200	ns
Maximum Pulse Width	$V_{\text{ZERO}} = 1\text{V}$	850	1000	1150	ns
Maximum to Minimum Pulse Width Ratio	$V_{\text{ZERO}} = 0\text{V}$ UCx861 – UCx864	2.5	4	5.5	
	$V_{\text{ZERO}} = 0\text{V}$ UCx865 – UCx868. $-55^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	4	5.5	7	
	$V_{\text{ZERO}} = 0\text{V}$ UCx865 – UCx868, $+125^{\circ}\text{C}$	3.8	5.5	7	
<b>Output Stage</b>					
Rise and Fall Time	$C_{\text{LOAD}} = 1\text{nF}$ (Note 4)		25	45	ns
Output Low Saturation	$I_{\text{O}} = 20\text{mA}$		0.2	0.5	V
	$I_{\text{O}} = 200\text{mA}$		0.5	2.2	V
Output High Saturation	$I_{\text{O}} = -200\text{mA}$ , down from $V_{\text{CC}}$		1.7	2.5	V
UVLO Low Saturation	$I_{\text{O}} = 20\text{mA}$		0.8	1.5	V
<b>Fault Comparator</b>					
Fault Comparator V <sub>th</sub>		2.85	3.00	3.15	V
Delay to Output	(Note 4) (Note 5)		100	200	ns



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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>UVLO</b>					
Vcc Turn-on Threshold	UCx861, UCx862, UCx865, UCx866	15	16.5	18	V
	UCx863, UCx864, UCx867, UCx868	7	8.0	9	V
Vcc Turn-off Threshold	UCx861, UCx862, UCx865, UCx866	9.5	10.5	11.5	V
	UCx863, UCx864, UCx867, UCx868	6	7.0	8	V
Icc Start	$V_{CC} = V_{CC(\text{on})} - 0.3\text{V}$		150	300	$\mu\text{A}$
Icc Run	$V_{\text{ID}} = 100\text{mV}$		25	32	$\text{mA}$

Note 1: Currents are defined as positive into the pin.

Note 2: Pulse measurement techniques are used to insure that  $T_J = T_A$ .

Note 3:  $V_{\text{ID}} = V(\text{NI}) - V(\text{INV})$ .

Note 4: This parameter is not 100% tested in production but guaranteed by design.

Note 5:  $V_i = 0$  to  $4\text{V}$        $t_r(V_i) = 10\text{ns}$        $t_{\text{pd}} = t(V_o = 6\text{V}) - t(V_i = 3\text{V})$

## APPLICATION INFORMATION

**UVLO & 5V GENERATOR (See Figure 1):** When power is applied to the chip and  $V_{CC}$  is less than the upper UVLO threshold,  $I_{CC}$  will be less than  $300\mu\text{A}$ , the 5V generator will be off, and the outputs will be actively held low.

When  $V_{CC}$  exceeds the upper UVLO threshold, the 5V generator turns on. Until the 5V pin exceeds  $4.9\text{V}$ , the outputs will still remain low.

The 5V pin should be bypassed to signal ground with a  $0.1\mu\text{F}$  capacitor. The capacitor should have low equivalent series resistance and inductance.

**FAULT AND SOFT-REFERENCE (See Figure 1):** The Soft-Ref pin serves three functions: system reference, restart delay, and soft-start. Designed to source or sink  $200\mu\text{A}$ , this pin should be used as the input reference for the error amplifier circuit. This pin requires a bypass capacitor of at least  $0.1\mu\text{F}$ . This yields a minimum soft-start time of  $1\text{ms}$ .

Under-Voltage Lockout sets both the fault and restart delay latches. This holds the outputs low and discharges the Soft-Ref pin. After UVLO, the fault latch is reset by the low voltage on the Soft-Ref pin. The reset fault latch resets the delay latch and Soft-Ref charges via the  $0.5\text{mA}$  current source.

The fault pin is input to a high speed comparator with a threshold of  $3\text{V}$ . In the event of a detected fault, the fault latch is set and the outputs are driven low. If Soft-Ref is above  $4\text{V}$ , the delay latch is set. Restart delay is timed as Soft-Ref is discharged by  $20\mu\text{A}$ . When Soft-Ref is fully discharged, the fault latch is reset if the fault input signal is low. The Fault pin can be used as a system shutdown pin.

If a fault is detected during soft-start, the fault latch is set and the outputs are driven low. The delay latch will remain reset until Soft-Ref charges to  $4\text{V}$ . This sets the delay latch, and restart delay is timed. Note that restart delay for a single fault event is longer than for recurring faults since Soft-Ref must be discharged from  $5\text{V}$  instead of  $4\text{V}$ .

The restart delay to soft-start time ratio is 24:1 for a fault occurring during normal operation and 19:1 for faults occurring during soft-start. Shorter ratios can be programmed down to a limit of approximately 3:1 by the addition of a  $20\text{k}\Omega$  or larger resistor from Soft-Ref to ground.

A  $100\text{k}\Omega$  resistor from Soft-Ref to  $5\text{V}$  will have the effect of permanent shut down after a fault since the internal  $20\mu\text{A}$  current source can't pull Soft-Ref low. This feature can be used to require recycling  $V_{CC}$  after a fault. Care must be taken to insure Soft-Ref is indeed low at start up, or the fault latch will never be reset.

APPLICATION INFORMATION

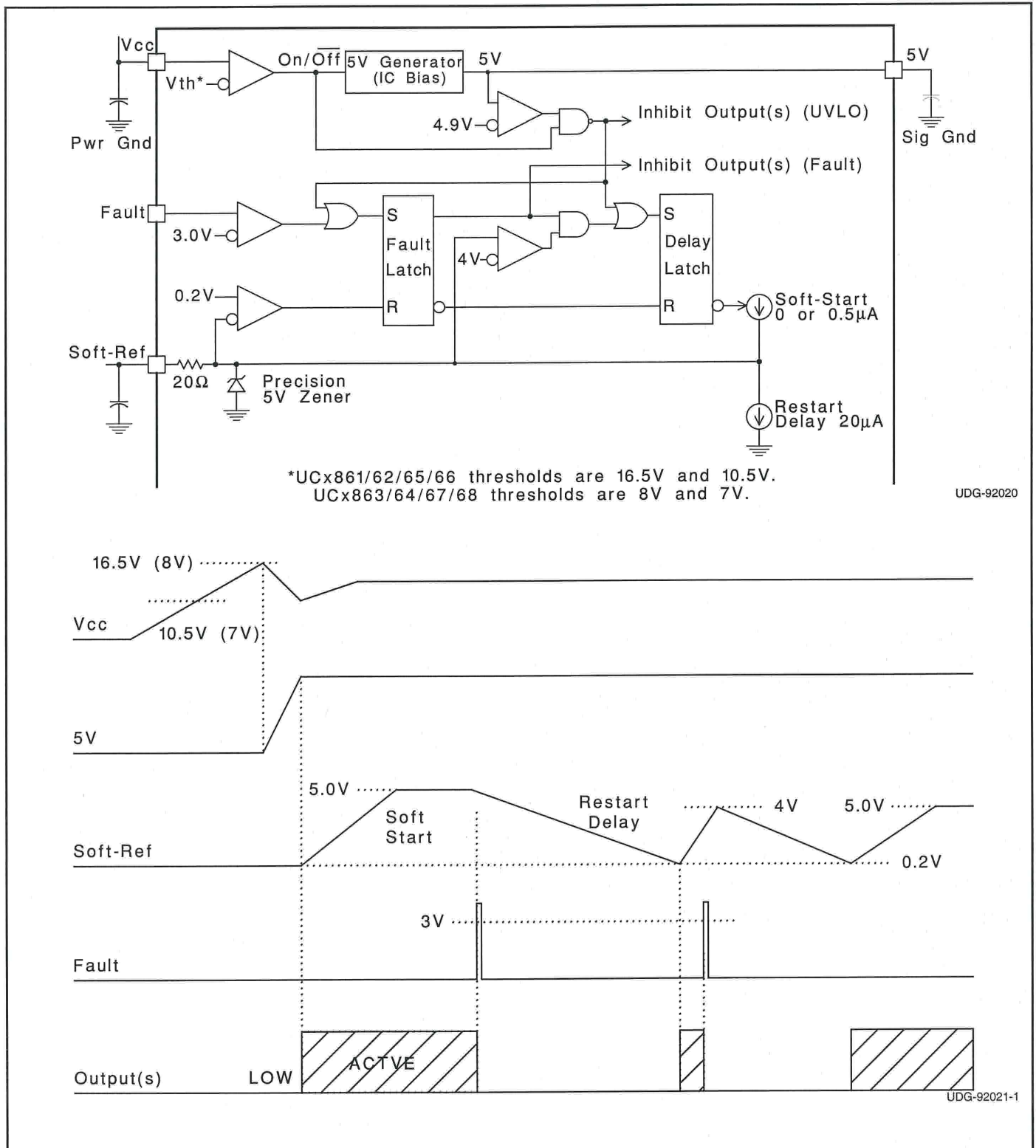
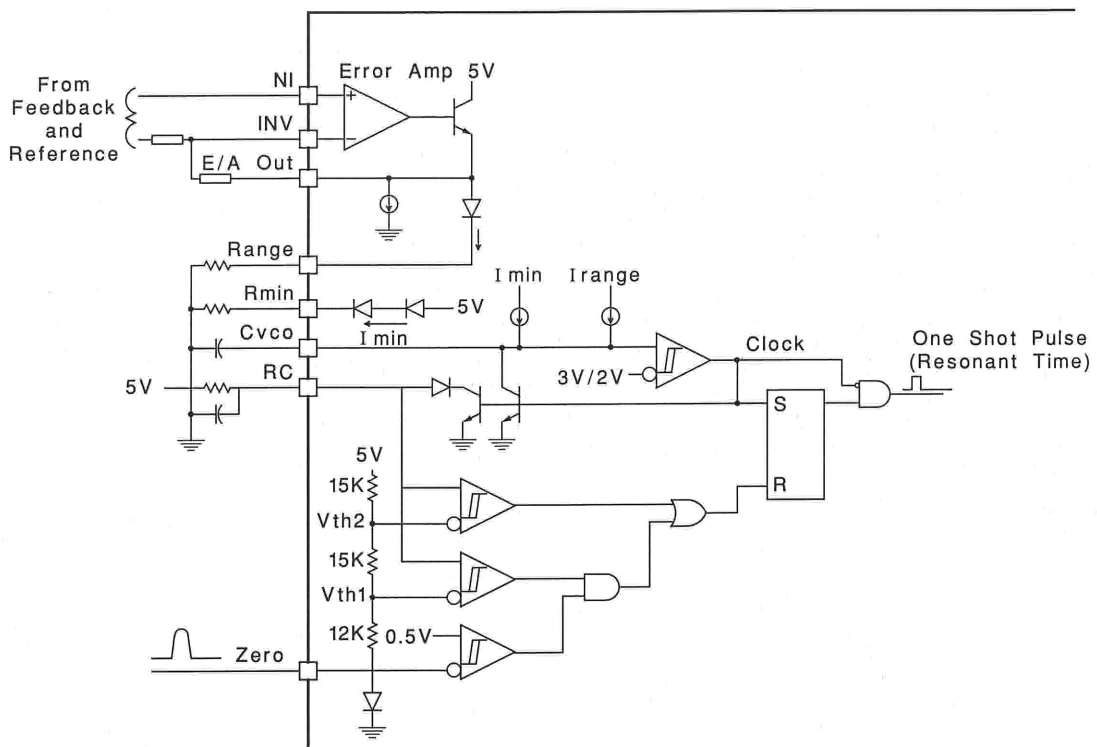
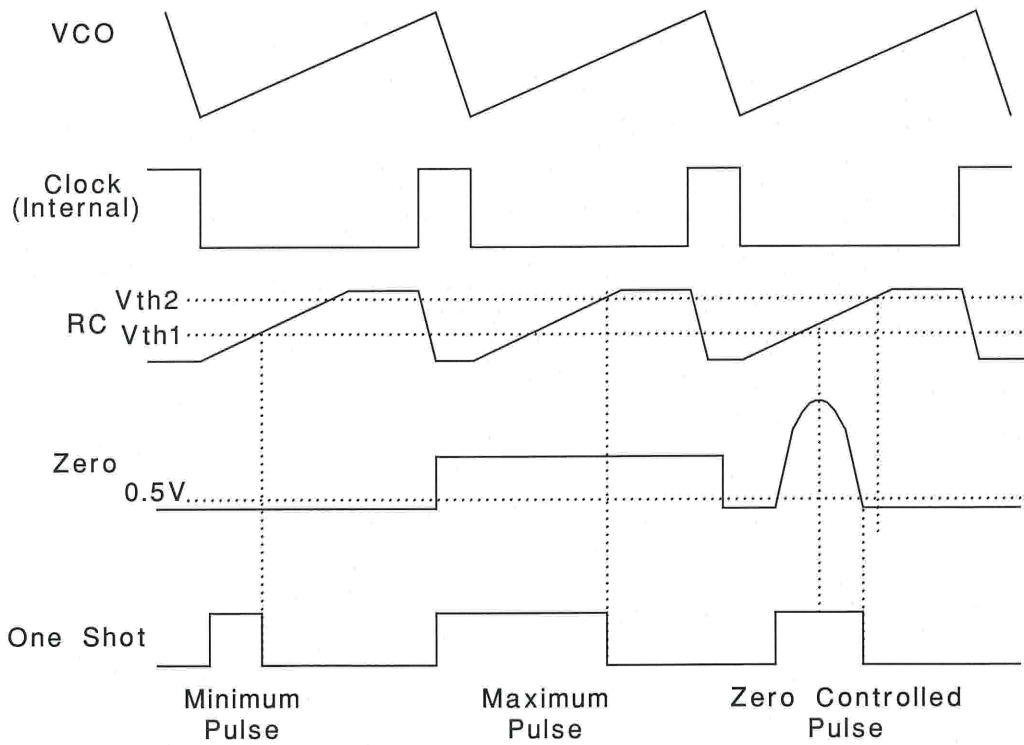


Figure 1. UVLO, 5V, fault and soft-ref.



UDG-92022-1



UDG-92023-1

Figure 2. Error Amp, Voltage Controlled Oscillator, and One Shot

## APPLICATION INFORMATION

Minimum oscillator frequency is set by  $R_{min}$  and  $C_{VCO}$ . The minimum frequency is approximately given by the equation:

$$F_{MIN} \cong \frac{3.6}{R_{MIN} \cdot C_{VCO}}$$

Maximum oscillator frequency is set by  $R_{min}$ , Range &  $C_{VCO}$ . The maximum frequency is approximately given by the equation:

$$F_{MAX} \cong \frac{3.6}{(R_{MIN} // Range) \cdot C_{VCO}}$$

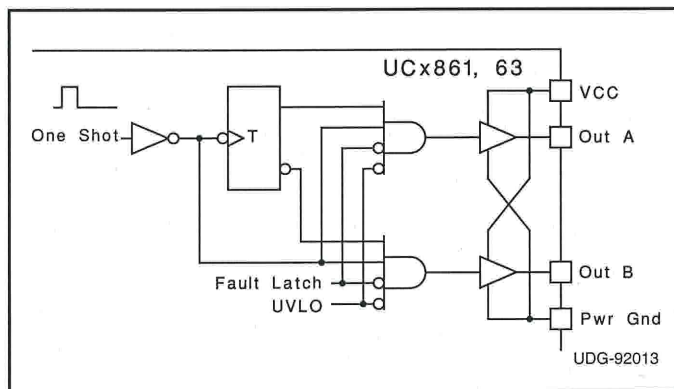
The Error Amplifier directly controls the oscillator frequency. E/A output low corresponds to minimum frequency and output high corresponds to maximum frequency. At the end of each oscillator cycle, the RC pin is discharged to one diode drop above ground. At the beginning of the oscillator cycle,  $V(RC)$  is less than  $V_{th1}$  and so the output of the zero detect comparator is ignored. After  $V(RC)$  exceeds  $V_{th1}$ , the one shot pulse will be terminated as soon as the zero pin falls below 0.5V or  $V(RC)$  exceeds  $V_{th2}$ . The minimum one shot pulse width is approximately given by the equation:

$$Tp_{w(min)} \approx 0.3 R C.$$

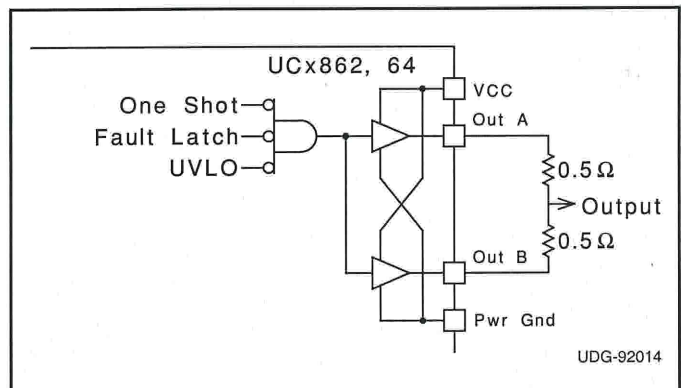
The maximum pulse width is approximately given by:

$$Tp_{w(max)} \approx 1.2 R C.$$

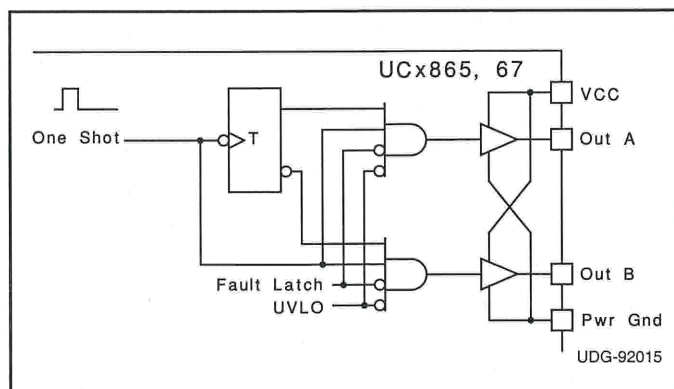
## STEERING LOGIC



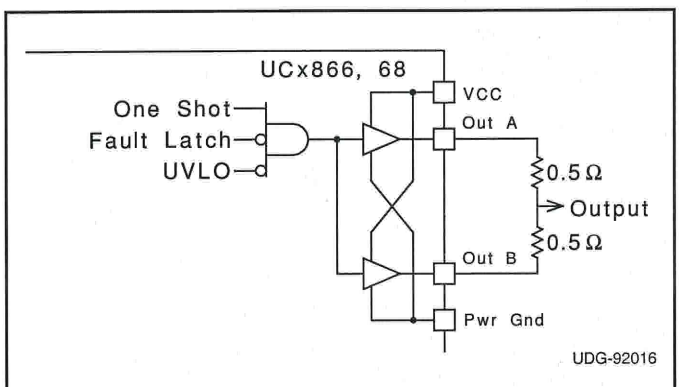
The steering logic is configured on the UC1861,63 to result in dual non-overlapping square waves at outputs A & B. This is suited to drive dual switch ZVS systems.



The steering logic is configured on the UC1862,64 to result in inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZVS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.



The steering logic is configured on the UC1865,67 to result in alternating pulse trains at outputs A & B. This is suited to drive dual switch ZCS systems.



The steering logic is configured on the UC1866,68 to result in non-inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZCS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.

APPLICATION INFORMATION (cont.)

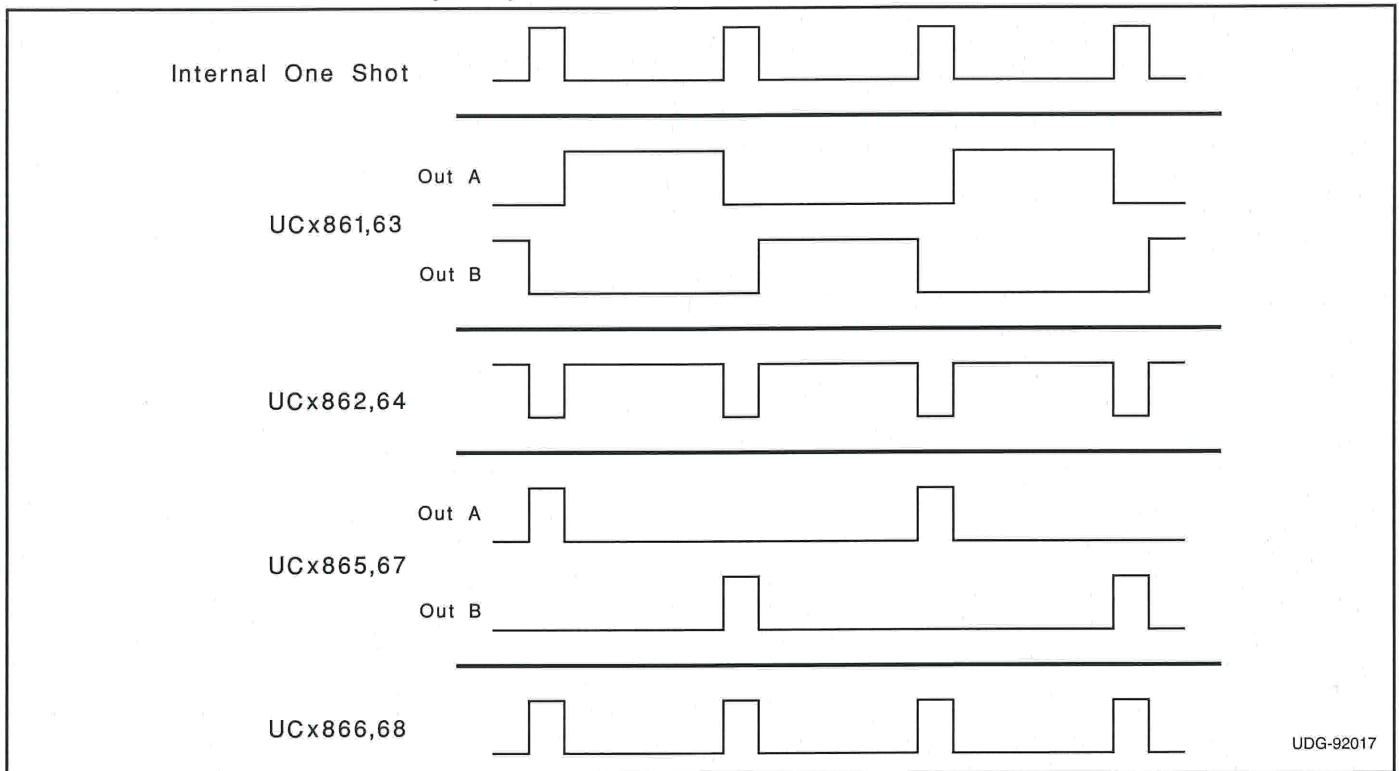


Figure 3. Current waveforms.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9203103Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9203103Q2A UC1863L/ 883B	<a href="#">Samples</a>
5962-9203103QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9203103QE A UC1863J/883B	<a href="#">Samples</a>
5962-9203103V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9203103V2A UC1863L QMLV	<a href="#">Samples</a>
UC1863J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1863J	<a href="#">Samples</a>
UC1863J883B	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9203103QE A UC1863J/883B	<a href="#">Samples</a>
UC1863L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1863L	<a href="#">Samples</a>
UC1863L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9203103Q2A UC1863L/ 883B	<a href="#">Samples</a>
UC2861DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2861DW	<a href="#">Samples</a>
UC2863DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2863DW	<a href="#">Samples</a>
UC2864DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2864DW	<a href="#">Samples</a>
UC3861DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3861DW	<a href="#">Samples</a>
UC3861DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3861DW	<a href="#">Samples</a>
UC3861N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3861N	<a href="#">Samples</a>
UC3863DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3863DW	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3865DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3865DW	<a href="#">Samples</a>
UC3867DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3867DW	<a href="#">Samples</a>
UC3867DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3867DW	<a href="#">Samples</a>
UC3867N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3867N	<a href="#">Samples</a>
UC3867NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3867N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UC1863, UC1863-SP, UC3863 :**

- Catalog: [UC3863](#), [UC1863](#)
- Military: [UC1863](#)
- Space: [UC1863-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3867DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1



TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3867DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

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