Agilent Technologies
Innovating the HP Way

Low Input Current, High Gain Optocouplers

Technical Data

6N139 6N138
HCPL-0701 HCPL-0700
HCNW139 HCNW138

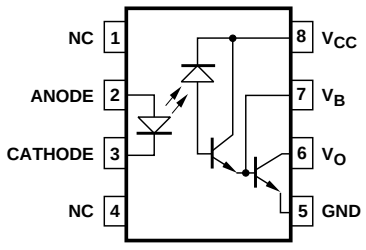
Features

- **High Current Transfer Ratio – 2000% Typical (4500% Typical for HCNW139/138)**
- **Low Input Current Requirements – 0.5 mA**
- **TTL Compatible Output – 0.1 V V_{OL} Typical**
- **Performance Guaranteed over Temperature 0°C to 70°C**
- **Base Access Allows Gain Bandwidth Adjustment**
- **High Output Current – 60 mA**
- **Safety Approval**
  UL Recognized – 2500 V rms for 1 Minute and 5000 V rms* for 1 Minute per UL 1577
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 1414 V peak for HCNW139 and HCNW138
  BSI Certified (HCNW139 and HCNW138)
- **Available in 8-Pin DIP or SOIC-8 Footprint or Widebody Package**
- **MIL-STD-1772 Version Available (HCPL-5700/1)**

Applications

- **Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL**
- **Low Input Current Line Receiver**
- **High Voltage Insulation (HCNW139/138)**
- **EIA RS-232C Line Receiver**
- **Telephone Ring Detector**
- **117 V ac Line Voltage Status Indicator – Low Input Power Dissipation**
- **Low Power Systems – Ground Isolation**

Functional Diagram



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photodetector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

*5000 V rms/1 minute rating is for HCNW139/138 and Option 020 (6N139/138) products only.
A 0.1 µF bypass capacitor connected between pins 8 and 5 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The 6N139, HCPL-0701, and CNW139 are for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over 0 to 70°C operating range for only 0.5 mA of LED current.

The 6N138, HCPL-0700, and HCNW138 are designed for use mainly in TTL applications. Current Transfer Ratio (CTR) is 300% minimum over 0 to 70°C for an LED current of 1.6 mA (1 TTL Unit load). A 300% minimum CTR enables operation with 1 TTL Load using a 2.2 kΩ pull-up resistor.

Selection for lower input current down to 250 μA is available upon request.

The HCPL-0701 and HCPL-0700 are surface mount devices packaged in an industry standard SOIC-8 footprint.

The SOIC-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

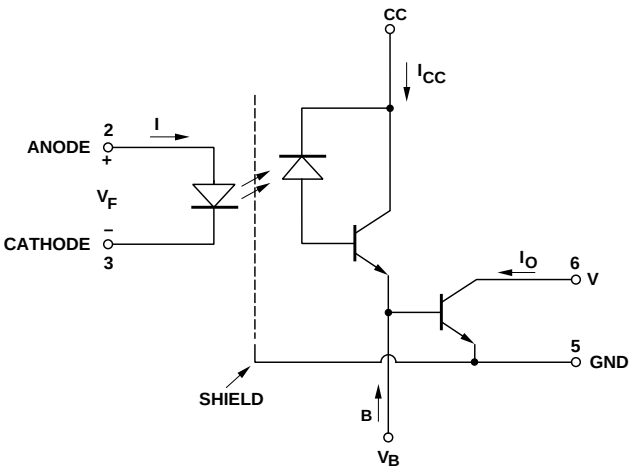
The HCNW139 and HCNW138 are packaged in a widebody encapsulation that provides creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

Selection Guide

					$_F$)	**CTR**	**V_{CC}**	**HCPL-**
6N139	2731							
6N138	2730	0700	0730	HCNW138	1.6 mA	300%	7 V	
HCPL-4701[1]	4731[1]	070A	073A[1]					
					0.5 mA	300%	20 V	5701[1] 5700[1] 5731[1] [1]

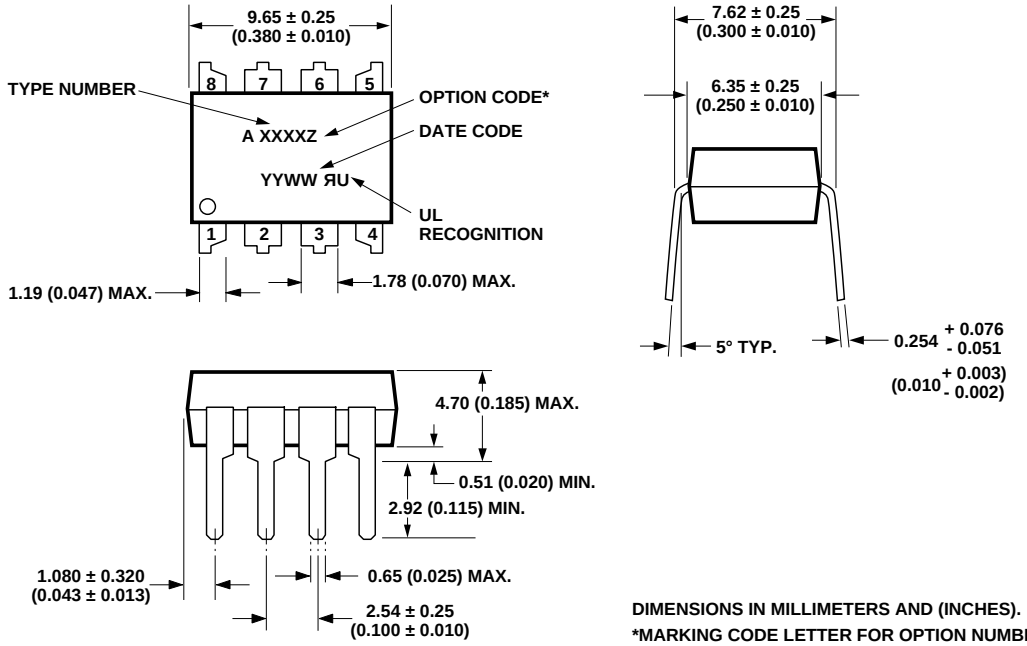
Note:
1. Technical data are on separate Agilent publications.

Schematic



Package Outline Drawings

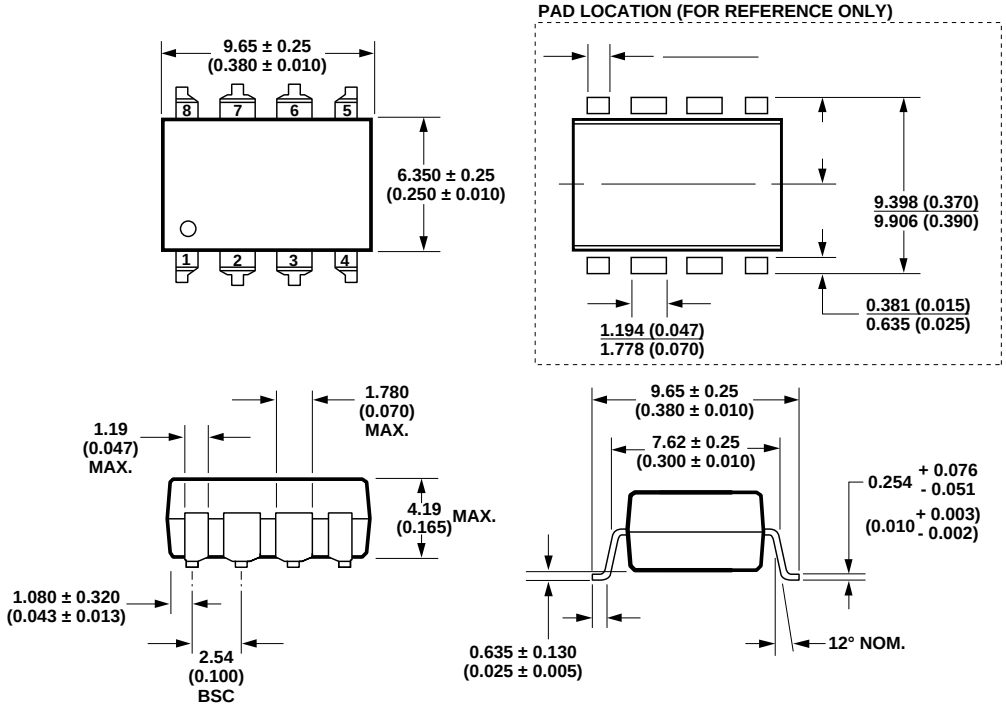
8-Pin DIP Package (6N139/6N138)**



DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
OPTION NUMBERS 300 AND 500 NOT MARKED.

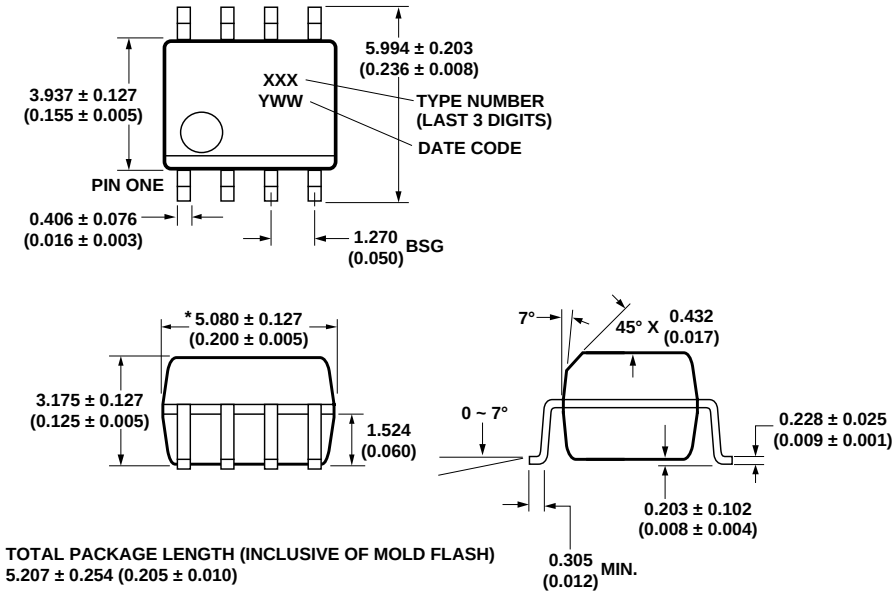
**JEDEC Registered Data.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (6N139/6N138)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

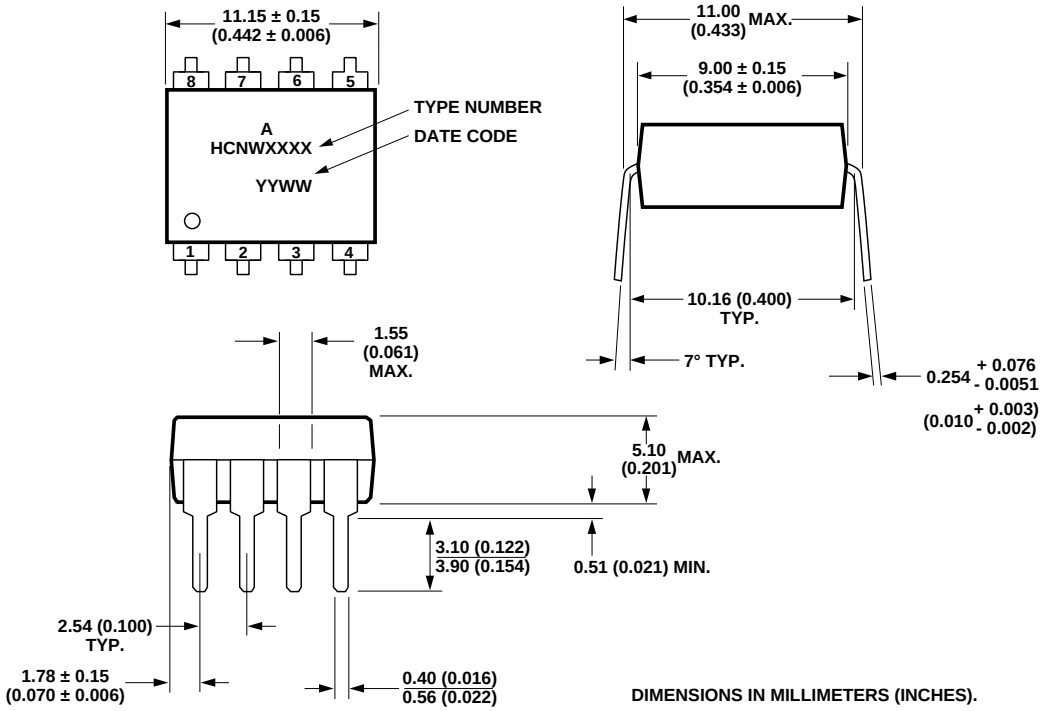
Small Outline SO-8 Package (HCPL-0701/HCPL-0700)



TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

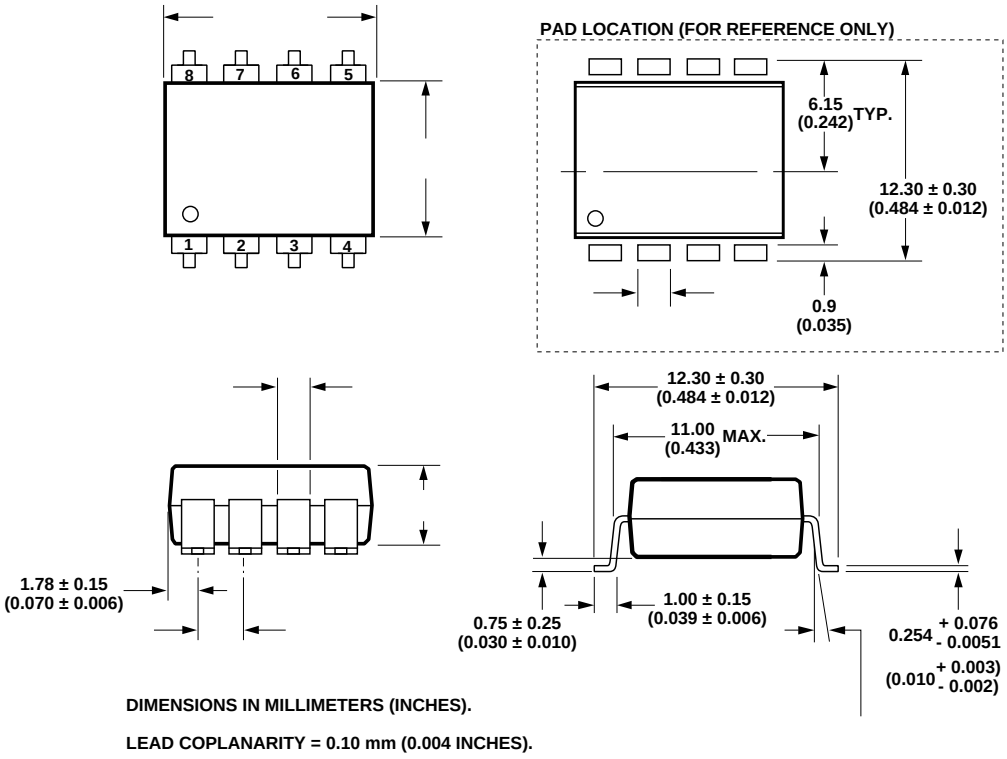
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

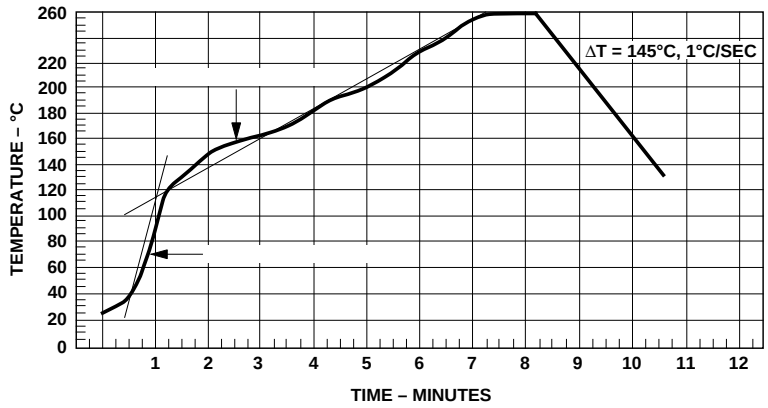
8-Pin Widebody DIP Package (HCNW139/HCNW138)



DIMENSIONS IN MILLIMETERS (INCHES).

8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW139/HCNW138)





Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The 6N139/138, HCNW139/138, and HCPL-0701/0700 have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/ 06.92 (HCNW139/138 only).

BSI

Certification according to BS415:1994, (BS EN60065:1994); BS EN60950:1992 (BS7002:1992) and EN41003:1993 for Class II applications (HCNW139/ HCNW138 only.)

Insulation and Safety Related Specifications

Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 Insulation Related Characteristics (HCNW139 and HCNW138)

Description	Symbol	Characteristic	Units
for rated mains voltage ≤ 1000 V rms		I-III	
Pollution Degree (DIN VDE 0110/1.89)		2	
		1414	V peak
PR IORM, 100% Production Test with t = 1 sec, Partial Discharge < 5 pC	V_{PR}		peak
Input to Output Test Voltage, Method a* V_{PR} IORM, Type and Sample Test, t_P = 60 sec, Partial Discharge < 5 pC	V_{PR}		peak
ini = 10 sec)	V_{IOTM}	8000	V peak
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 11, Thermal Derating curve.)			
Case Temperature	T	175	°C
Current (Input Current I_F, P_S = 0)	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$		
S, V = 500 V	R	> 10^9	

Absolute Maximum Ratings* (No Derating Required up to 85°C)

Storage Temperature	T			
Operating Temperature**	T_A			
	F(AVG)		20	mA
Peak Forward Input Current	I			
Peak Transient Input Current (<1 µs Pulse Width, 300 pps)	$I_{F(TRAN)}$		1.0	A
Reverse Input Voltage	V_R		5	V
Input Power Dissipation	P_I		35	mW
			60	mA
	EB		0.5	V
Supply Voltage and Output Voltage	V_{CC}			
(6N138, HCPL-0700, HCNW138)	CC	-0.5	7	V
Output Power Dissipation	P			
	T		135	mW

Recommended Operating Conditions

Power Supply Voltage	V_{CC}	4.5	18	V
Forward Input Current (ON)	$I_{F(ON)}$	0.5	12.0	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
Operating Temperature	T_A			

Electrical Specifications

0°C ≤ T_A $_{F(ON)}$ ≤ 12 mA, 0 V ≤ V ≤ 0.8 V, unless otherwise specified. All Typicals at T_A

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions		Fig.	Note
Current Transfer Ratio	CTR	6N139 HCPL-0701	400*	2000	5000	%	I_F	= 4.5 V_O = 0.4 V	2, 3	1, 2, 4
		HCNW139	400	4500						
		HCPL-0701					$_F$ = 1.6 mA			
			300	1600			I_F = 5.0 mA			
			200	850			I_F = 12 mA			
		HCPL-0700					$_F$ = 1.6 mA			
		HCNW138		1500						
Voltage	OL	6N139 HCPL-0701 HCNW139		0.1	0.4	V	I = 0.5 mA, I_O = 2 mA	V = 4.5	1	2
							$_F$ = 1.6 mA, I_O			
							= 5.0 mA, I = 15 mA			
				0.2			I = 12 mA, I_O			
		HCPL-0700 HCNW138					$_F$ = 1.6 mA, I = 4.8 mA			
Logic High Output Current	I_{OH}	6N139 HCPL-0701 HCNW139		0.05	100	µA	V_O = V_{CC} = 18 V	I_F = 0 mA		2
		6N138		0.1	250		V CC			
Current		6N138/139 HCPL-0701/ 0700		0.4	1.5	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V		10	2
		HCNW139 HCNW138		0.5	2					
Logic High Supply Current	I_{CCH}	6N138/139 HCPL-0701/ 0700		0.01	10	µA	I_F = 0 mA, V_O = Open, V_{CC} = 18 V			2
		HCNW139 HCNW138			1					
Voltage		6N138 6N139	1.25	1.40	1.7*	V	T_A = 25°C	I_F = 1.6 mA	4, 8	
		HCPL-0701 HCPL-0700			1.75					
		HCNW139	1.0	1.45	1.85		T_A			
Input Reverse Breakdown Voltage	BVR		5.0*			V	I_R = 10 µA, T_A = 25°C			
		HCNW138					$_R$ = 100 µA, T_A = 25°C			
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6 mA		8	
Capacitance	IN			60		pF	f = 1 MHz, V_F = 0 V			
		HCNW139 HCNW138		90						

*JEDEC Registered Data for 6N139 and 6N138.

**All typical values at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Switching Specifications (AC)

Over recommended operating conditions (T = 0 to 70°C), V

Time to Logic Low at Output		HCPL-0701 HCNW139			30		$_A$ = 25°C I_F	5, 6, 7, 9, 12	2, 4
		6N139		0.2	1* 2	µs	T_A = 25°C I_F		
		6N138 HCPL-0700 HCNW138		1.6	10* 15	µs	T = 25°C I_F = 1.6 mA, Rl = 2.2 kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}	6N139 HCPL-0701 HCNW139		18	60* 90	µs	T_A = 25°C I_F = 0.5 mA, Rl = 4.7 kΩ	5, 6, 7, 9, 12	2, 4
		HCNW139			115				
		6N139		2	7*	µs	T_A F		
		HCPL-0700 HCNW138					$_A$ = 25°C I_F = 1.6 mA, Rl = 2.2 kΩ		
		6N138 HCPL-0700			50				
		HCNW139			70				
Transient Immunity at Logic High Output	$_H$|		1000	10000		V/µs	I_F = 0 mA, T_A = 25°C Rl = 2.2 kΩ |V_{CM}| = 10 Vp-p	13	5, 6
Common Mode Transient Immunity at Logic Low Output	|CM_L|		1000	10000		V/µs	I_F = 1.6 mA, T_A = 25°C Rl = 2.2 kΩ |V_{CM}| = 10 Vp-p	13	5, 6

$_A$ = 25°C and V_{CC} = 5 V, unless otherwise noted.

Package Characteristics

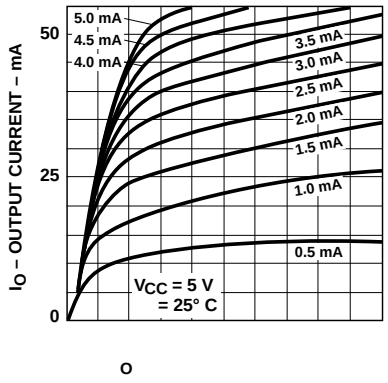
Parameter	Sym.	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Withstand Voltage†		2500			V rms	RH < 50%, t = 1 min., T_A		3, 8
Option 020 HCNW139 HCNW138		5000						3, 9
Resistance (Input-Output)	R_{I-O}		^{12}			$_{I-O}$ = 500 Vdc RH < 45%		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

**All typicals at T = 25°C, unless otherwise noted.

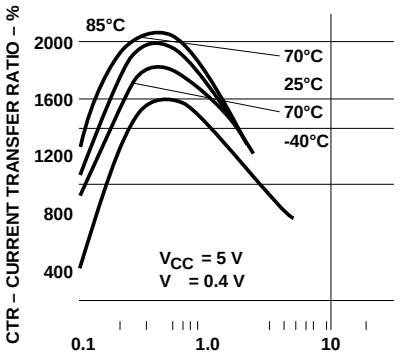
†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or Agilent Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

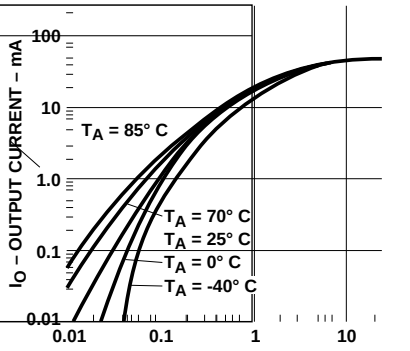
1. DC CURRENT TRANSFER RATI0 (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Pin 7 Open.
3. Device considered a two-terminal device. Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
4. Use of a resistor between pin 5 and 7 will decrease gain and delay time. Significant reduction in overall gain can occur when using resistor values below 47 kΩ. For more information, please contact your local HP Components representative.
5. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM} $_{CM}$, to assure that the output will remain in a Logic High state (i.e., V $_{CM}$/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
6. In applications where dV/dt may exceed 50,000 V/µs (such as static discharge) a series resistor, R , should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 220 Ω.
7. Use of a 0.1 µF bypass capacitor connected between pins 8 and 5 adjacent to the device is recommended.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage 3000 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 µA). This test is performed before the 100% production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 µA). This test is performed before the 100% production test for partial discharge (method b) shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.



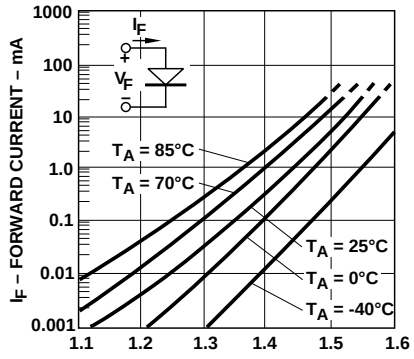
O



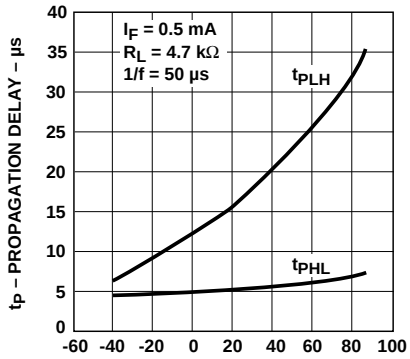
F – FORWARD CURRENT – mA



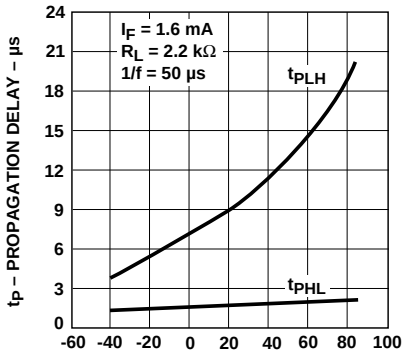
IF – INPUT DIODE FORWARD CURRENT – mA



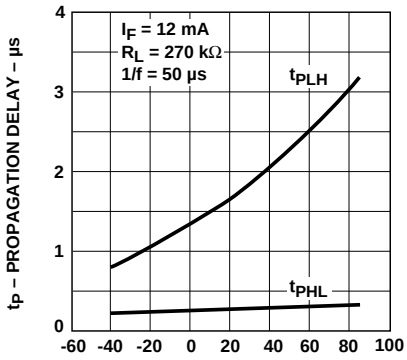
VF – FORWARD VOLTAGE – V



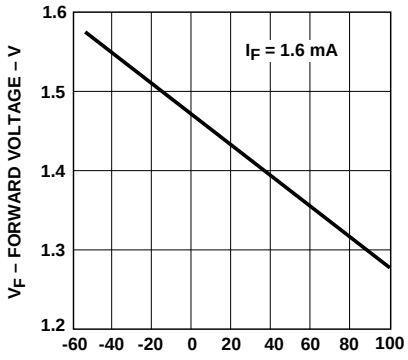
TA – TEMPERATURE – °C



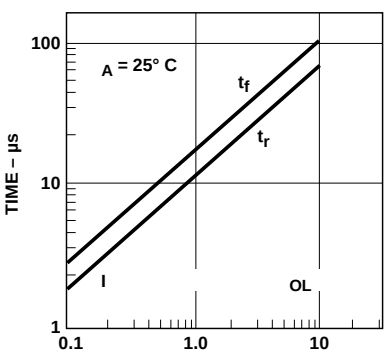
TA – TEMPERATURE – °C



TA – TEMPERATURE – °C



TA – TEMPERATURE – °C



– LOAD RESISTANCE – kΩ

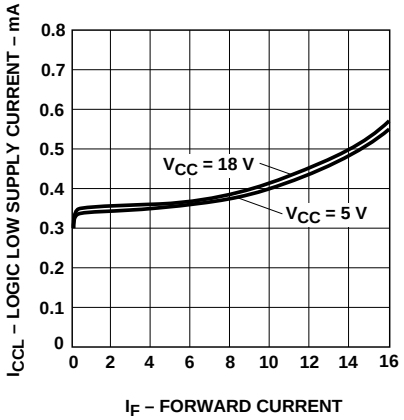


Figure 10. Logic Low Supply Current vs. Forward Current.

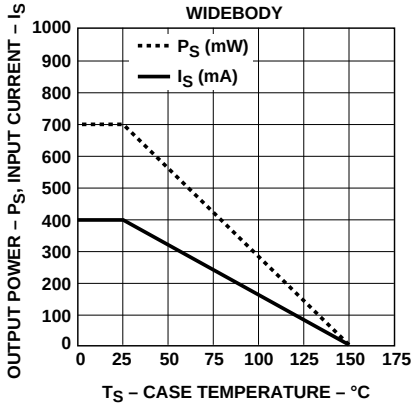


Figure 11. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

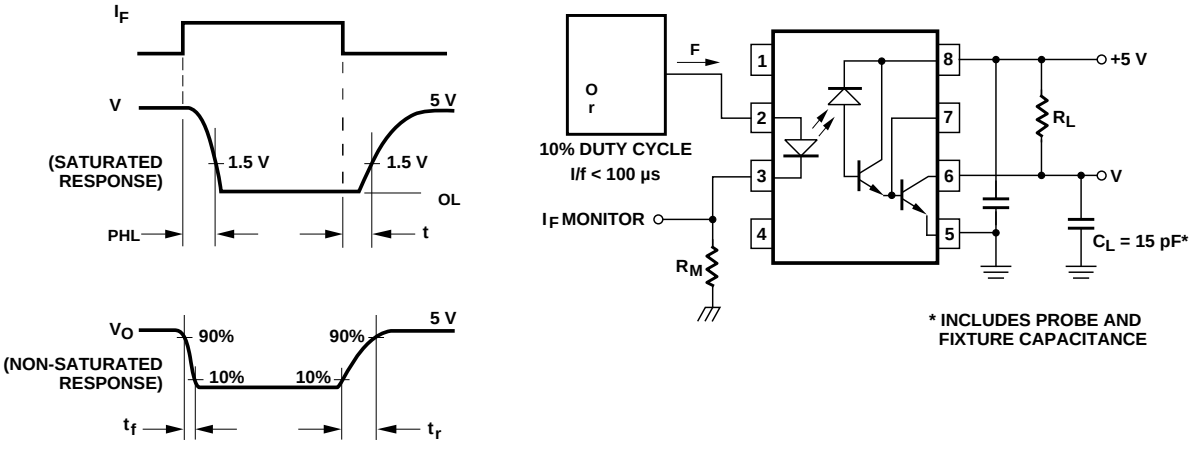


Figure 12. Switching Test Circuit.

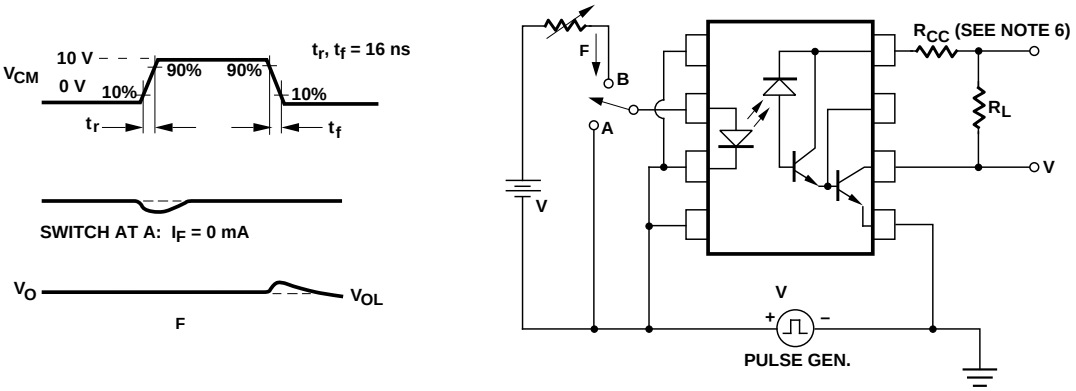


Figure 13. Test Circuit for Transient Immunity and Typical Waveforms.

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Data subject to change.

Obsoletes 5963-5166E, 5963-5168E,
5964-2258E

5965-3599E (11/99)