

# HD74HC259

## 8-bit Addressable Latch

REJ03D0603-0200  
 (Previous ADE-205-480)  
 Rev.2.00  
 Jan 31, 2006

### Description

The HD74HC259 has a single data input (D), 8 latch outputs (Q<sub>0</sub>-Q<sub>7</sub>), 3 address inputs (A, B, and C), a common enable input (E), and a common clear input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B and C inputs. When enable is taken low the data flows through to the addressed output. The data is stored when enable transitions from low to high. All unaddressed latches will remain unaffected. With enable in the high state the device is deselected, and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

If enable is held high and clear is taken low all eight latches are cleared to a low state. If enable is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

### Features

- High Speed Operation:  $t_{pd}$  (Data to Output) = 16 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC259P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC259FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC259RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

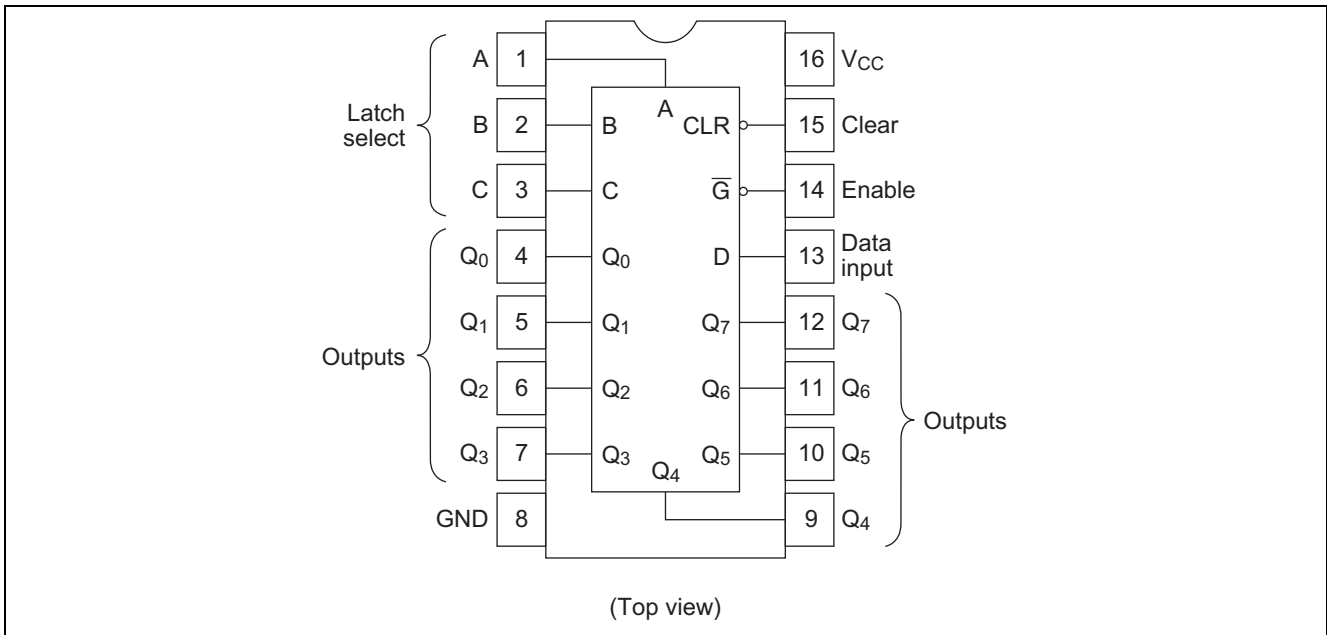
**Function Table**

Inputs		Output of Addressed Latch	Each Other Output	Function
Clear	G			
H	L	D	Q <sub>io</sub>	Addressable latch
H	H	Q <sub>io</sub>	Q <sub>io</sub>	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

- Notes: 1. D: the level at the data input  
 2. Q<sub>io</sub>: the level of Q<sub>i</sub> (i = 0, 1, ...7, as appropriate) before the indicated steady-state input conditions were established.

**Pin Arrangement**



### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
Input / Output voltage	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	$I_{IK}, I_{OK}$	$\pm 20$	mA
Output current	$I_O$	$\pm 25$	mA
$V_{CC}$ , GND current	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA
Power dissipation	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

### Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to 85	°C	
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Notes: 1. This item guarantees maximum limit when one input switches.  
Waveform: Refer to test circuit of switching characteristics.

### Electrical Characteristics

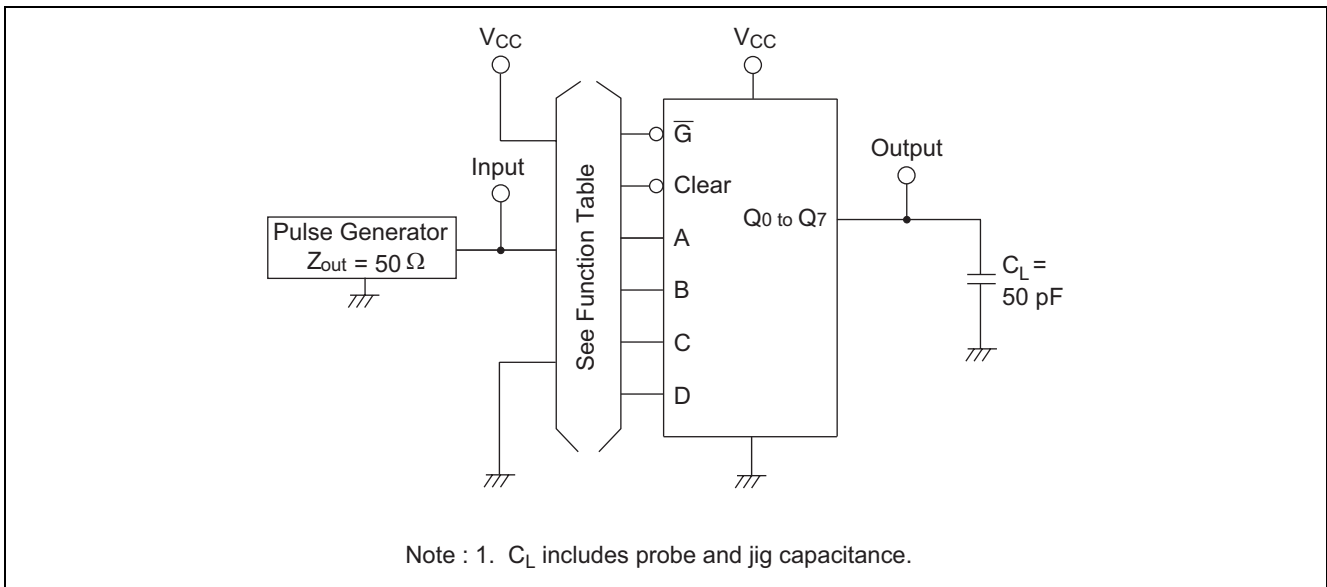
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	$V_{IH}$	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	$V_{IL}$	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	$V_{OH}$	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\ \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -4\ \text{mA}$
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -5.2\ \text{mA}$
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	$V_{OL}$	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\ \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4\ \text{mA}$
		6.0	—	—	0.26	—	0.33			$I_{OL} = 5.2\ \text{mA}$
Input current	$I_{in}$	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	$V_{in} = V_{CC}$ or GND	
Quiescent supply current	$I_{CC}$	6.0	—	—	4.0	—	40	$\mu\text{A}$	$V_{in} = V_{CC}$ or GND, $I_{out} = 0\ \mu\text{A}$	

### Switching Characteristics

( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

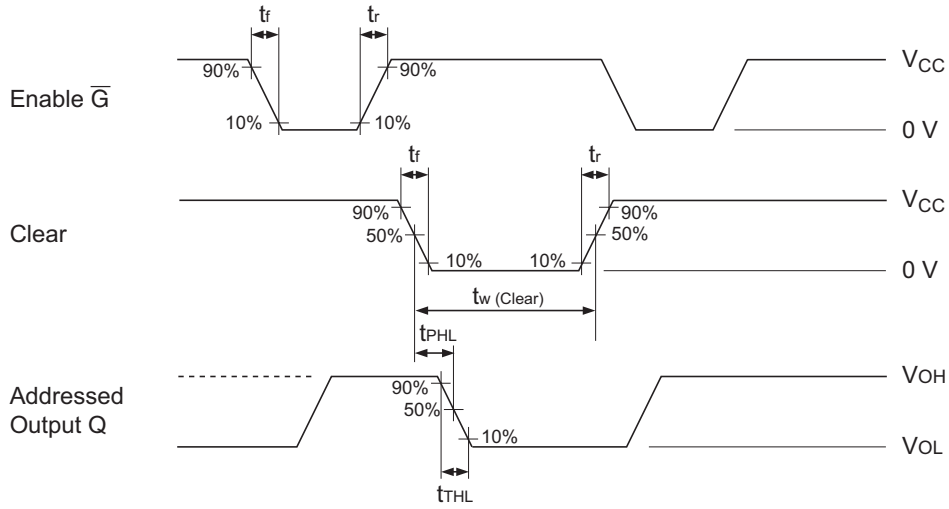
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	$t_{PHL}$	2.0	—	—	185	—	230	ns	Data to output
		4.5	—	16	37	—	46		
		6.0	—	—	31	—	39		
	$t_{PLH}$	2.0	—	—	215	—	270	ns	Latch select to output
		4.5	—	20	43	—	54		
		6.0	—	—	37	—	46		
	$t_{PHL}$	2.0	—	—	200	—	250	ns	Enable to output
		4.5	—	17	40	—	50		
		6.0	—	—	34	—	43		
	$t_{PHL}$	2.0	—	—	155	—	195	ns	Clear to output
		4.5	—	15	31	—	39		
		6.0	—	—	26	—	33		
Pulse width	$t_w$	2.0	80	—	—	100	—	ns	Clear, Enable
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Setup time	$t_{su}$	2.0	100	—	—	125	—	ns	Latch select or data to enable
		4.5	20	5	—	25	—		
		6.0	17	—	—	21	—		
Hold time	$t_h$	2.0	5	—	—	5	—	ns	Latch select or data to enable
		4.5	5	-1	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall time	$t_{TLH}$	2.0	—	—	75	—	95	ns	
	$t_{THL}$	4.5	—	5	15	—	19		
	$t_{THL}$	6.0	—	—	13	—	16		
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF	

### Test Circuit



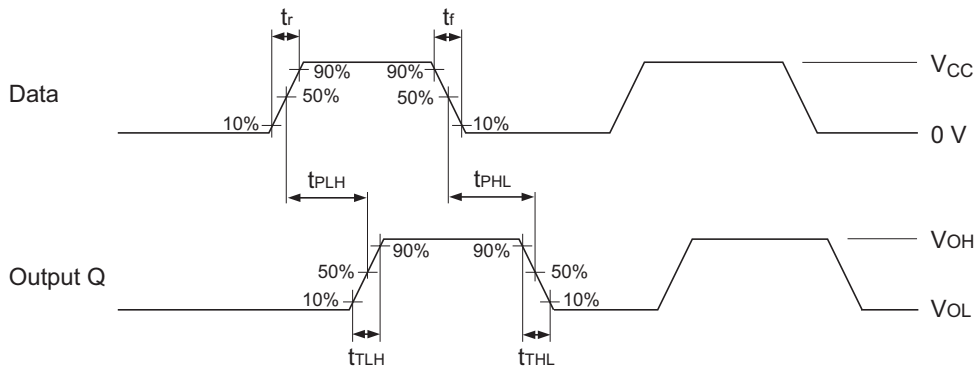
Waveforms

• Waveform – 1



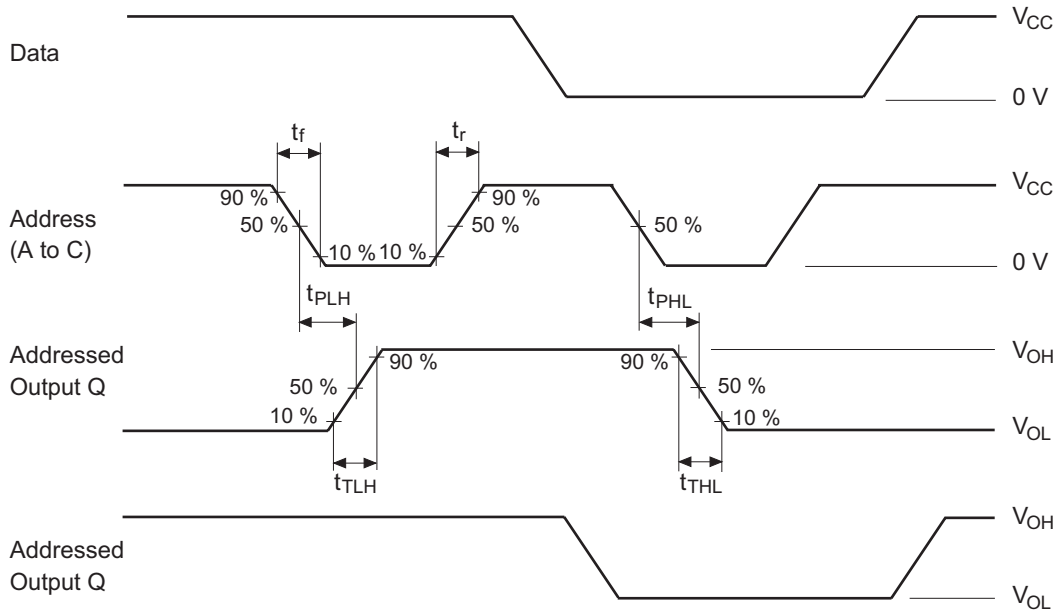
- Notes : 1. Input pulse :  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$
- 2.  $D = V_{CC}$ , Unaddressed  $Q = L$

• Waveform – 2



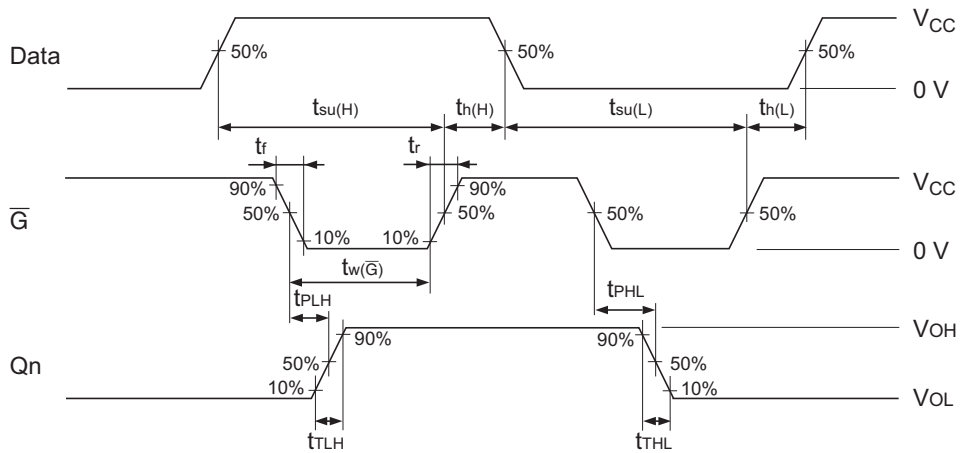
- Notes : 1. Input pulse :  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$
- 2. Other input :  $\bar{G} = \text{GND}$ , Clear =  $V_{CC}$ , A to C = Address

• Waveform – 3



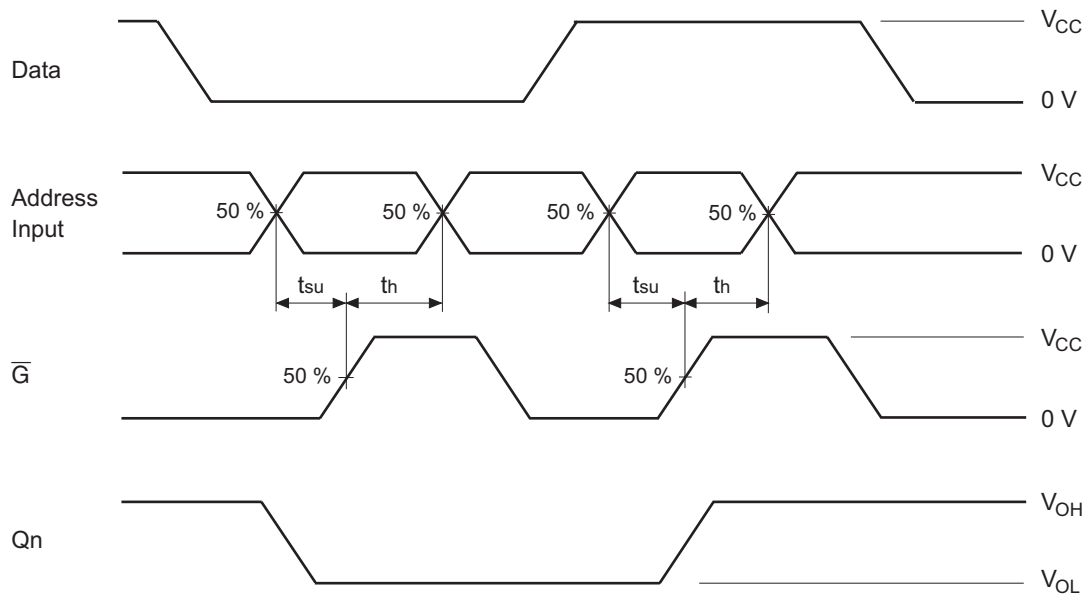
Notes : 1. Input pulse :  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$   
 2. Other input :  $\bar{G} = \text{GND}$ , Clear =  $V_{CC}$ , A to C = Address

• Waveform – 4



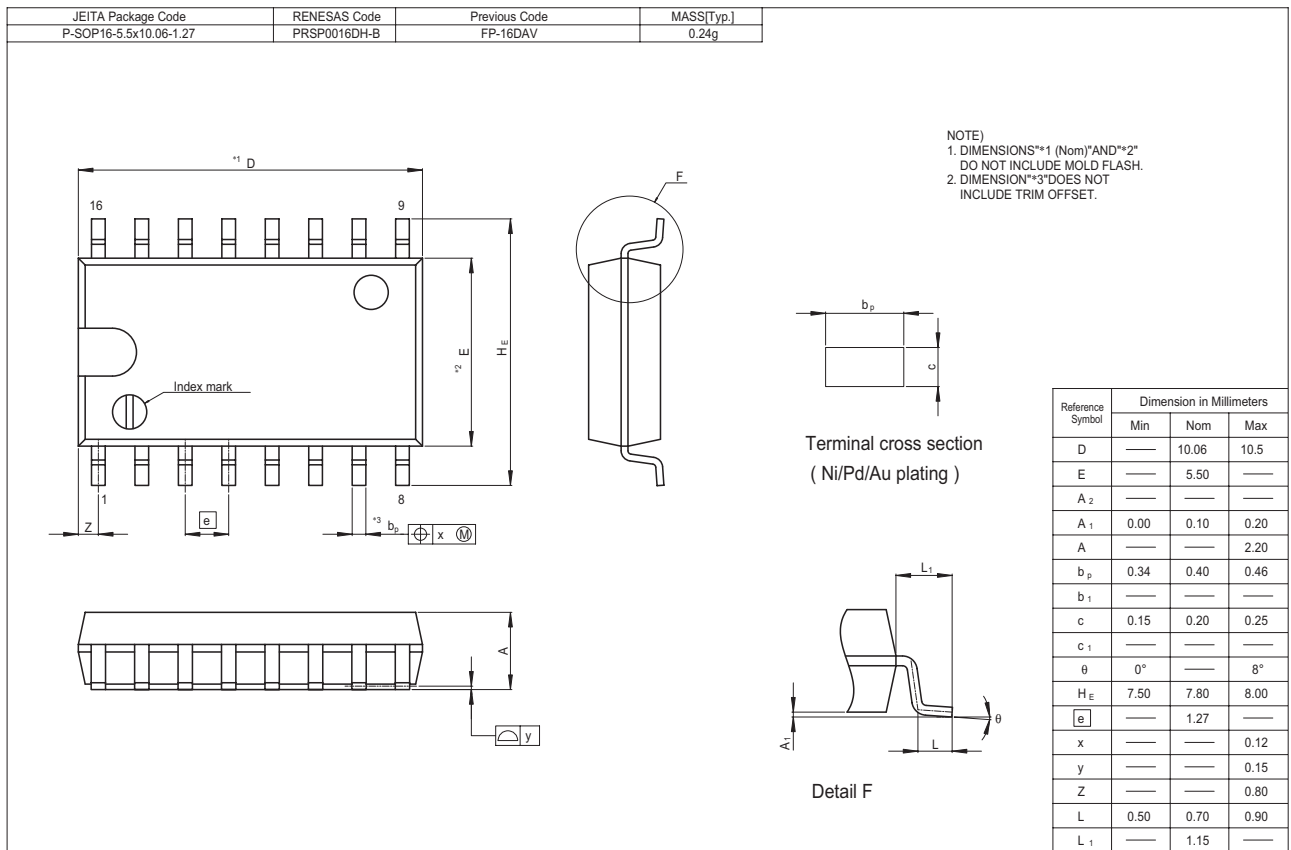
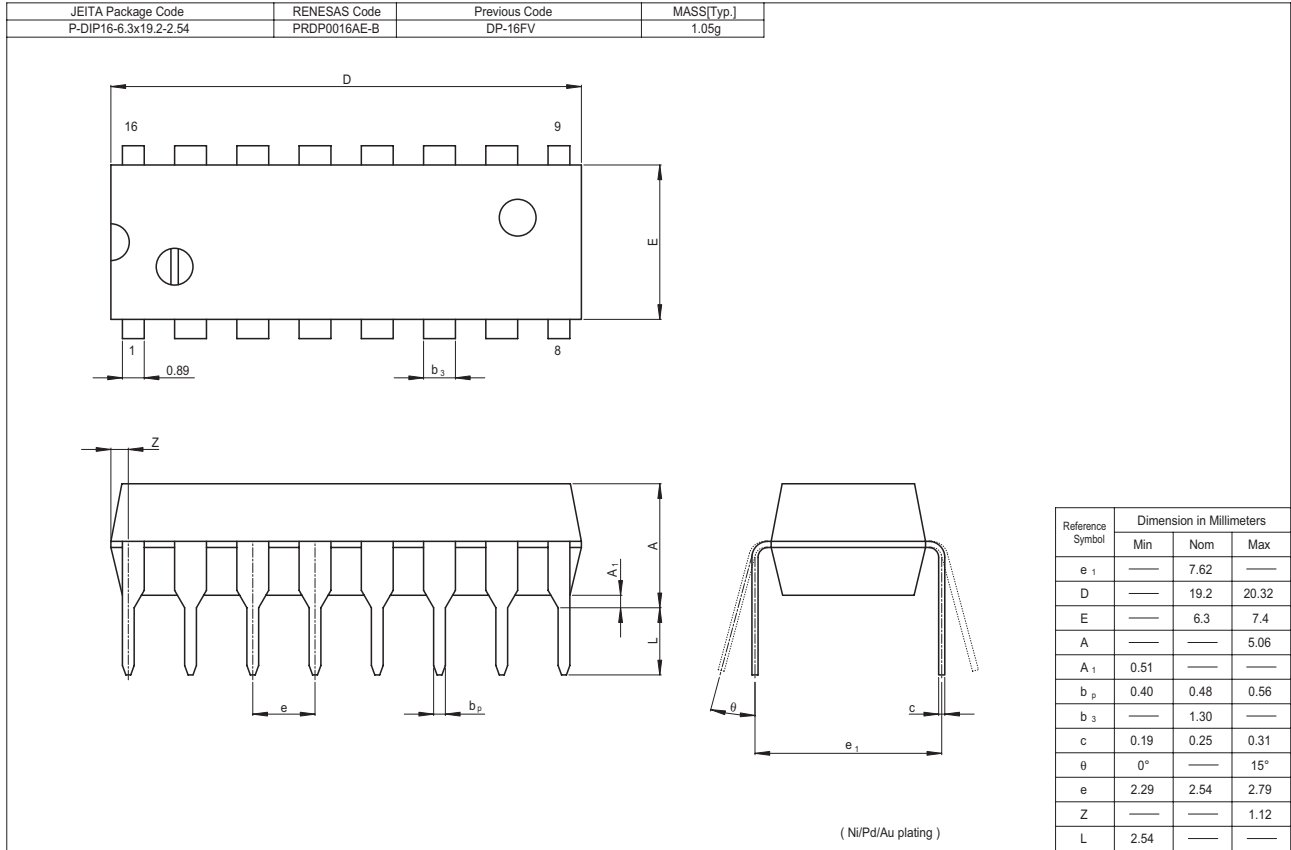
Notes : 1. Input pulse :  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$   
 2. Other input : Clear =  $V_{CC}$ , A to C = Address

• Waveform – 5



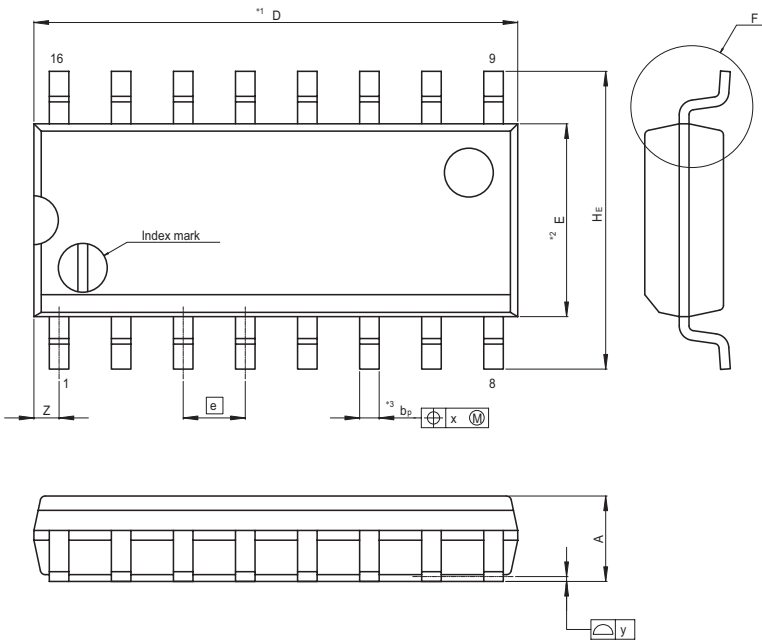
- Notes : 1. Input pulse : PRR ≤ 1 MHz, Z<sub>o</sub> = 50 Ω, t<sub>r</sub> ≤ 6 ns, t<sub>f</sub> ≤ 6 ns  
 2. Other input : Clear = V<sub>CC</sub>  
 3. Address inputs except appropriate inputs are set to address to appropriate Q outputs.

Package Dimensions

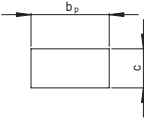




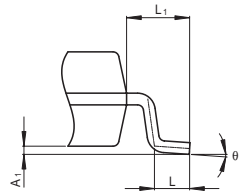
JEITA Package Code P-SOP16-3.95x9.9-1.27	RENESAS Code PRSP0016DG-A	Previous Code FP-16DNV	MASS[Typ.] 0.15g
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NOTE  
 1. DIMENSIONS\*\*1 (Nom)\*\*AND\*\*2  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION\*\*3\*\*DOES NOT  
 INCLUDE TRIM OFFSET.



Terminal cross section  
( Ni/Pd/Au plating )



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	9.90	10.30
E	—	3.95	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.10	0.14	0.25
A	—	—	1.75
b <sub>p</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.15
Z	—	—	0.635
L	0.40	0.60	1.27
L <sub>1</sub>	—	1.08	—

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