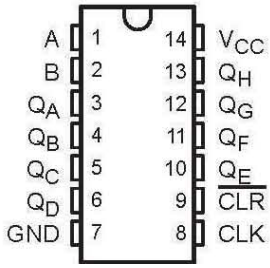
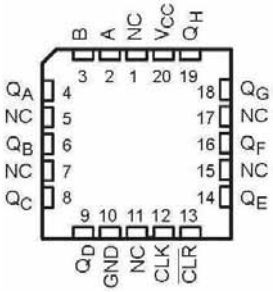
- **Wide Operating Voltage Range of 2 V to 6V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 80- μ A Max I_{CC}**
- **Typical t_{pd} =20 ns**
- **±4-mA Output Drive at 5V**
- **Low Input Current of 1 μ A Max**
- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**

MC54HC164…J OR W PACKAGE
MC74HC164…AD,N,NS, OR PW PACKAGE
(TOP VIEW)



MC54HC164…FK PACKAGE

(TOP VIEW)



NC-No Internal connection

Description/ordering information

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) input permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PARTNUMBER	TOP-SIDE MARKING
-40℃ to 85℃	PDIP –AN	Tube of 25	MC74HC164 AN	MC74HC164 AN
	PDIP –N	Tube of 25	MC74HC164N	MC74HC164N
	SOIC - D	Tube of 50	MC74HC164AD	HC164
		Reel of 2500	MC74HC164AD	
		Reel of 250	MC74HC164DT	
	SOP –NS	Reel of 2000	MC74HC164NSR	HC164
	TSSOP – PW	Tube of 90	MC74HC164PW	HC164
		Reel of 2000	MC74HC164PWR	
		Reel of 250	MC74HC164PWT	
-55℃ to 125℃	CDIP – J	Tube of 25	MC54HC164J	MCJ54HC164J
	CFP – W	Tube of 150	MC54HC164W	MCJ54HC164W
	LCCC - FK	Tube of 55	MC54HC164FK	MCJ54HC164FK

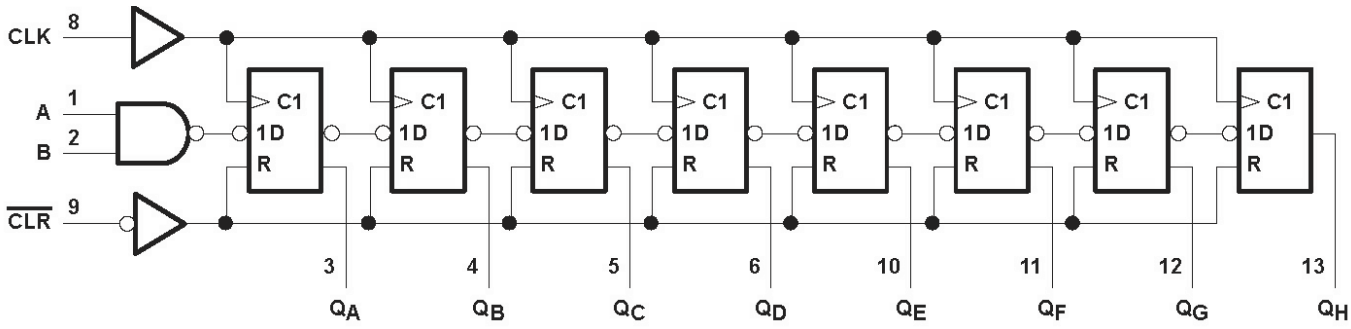
FUNCTION TABLE

INPUTS				OUTPUTS		
$\overline{CLR}$	CLK	A	B	Q_A	Q_B ... Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

Q_{A0}, Q_{B0},Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established

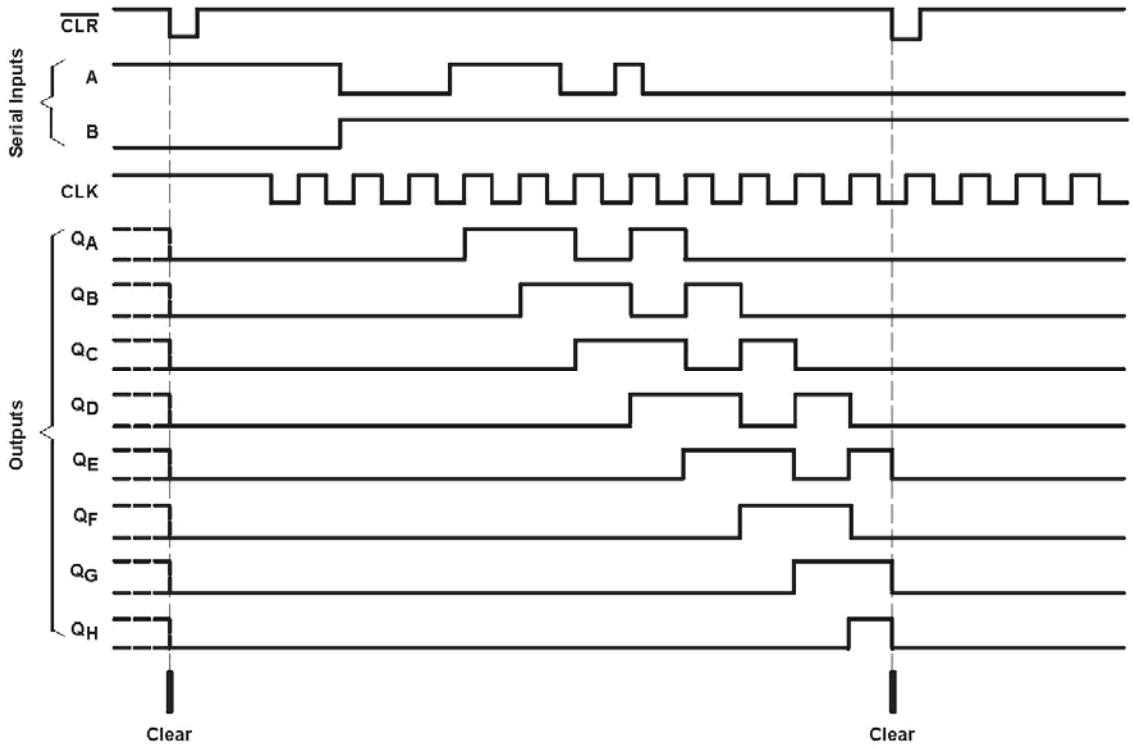
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of CLK: indicates a 1-bit shift

logic diagram (positive logic)



Pin numbers shown are for the AD,J,N,NS, PW, and W packages.

Typical clear, shift, and clear sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †

Supply voltage range, V_{CC}……-0.5 V to 7 V

Input clamp current, I_{IK}(V_I < 0 or V_I >V_{CC}) (see Note 1)……±20mA

Output clamp current, I_{oK}(V_o < 0 or V_o >V_{CC}) (see Note 1)…… ±20mA

Continuous output current, I_o (V_o = 0 to V_{CC}) ……±25mA

Continuous current through V_{CC} or GND……±50mA

Package thermal impedance, θ_{JA} (see Note 2): AD package……86℃/W

N package……80℃/W

NS package……76℃/W

PW package……113℃/W

Storage temperature range, T_{stg} ……-65℃ to 150℃

†Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7

Recommended operating conditions (see Note 3)

			MC54HC164			MC74HC164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC}=2V	1.5			1.5			V
		V_{CC}=4.5V	3.15			3.15			
		V_{CC}=6V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC}=2V			0.5			0.5	V
		V_{CC}=4.5V			1.35			1.35	
		V_{CC}=6V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
△t /△v†	Input transition rise/fall time	V_{CC}=2V			1000			1000	ns
		V_{CC}=4.5V			500			500	
		V_{CC}=6V			400			400	
T_A	Operating free-air temperature		-55		125	-40		85	℃

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report. Implications of Slow or Floating CMOS Inputs, literature number SCBAOO4.

† If this device is used in the threshold region (from V_{IL} max = 0.5V to V_{IH} min =1.5V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t =1000ns and V_{CC} = 2V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		VCC	T_A =25℃			MC54HC164		MC74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I= V_{IH} or V_{IL}	I_{OH} = -20 μA	2V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6V	5.9	5.999		5.9		5.9		
		I_{OH} = -4mA	4.5V	3.98	4.3		3.7		3.84		
		I_{OH} = -5.2mA	6V	5.48	5.8		5.2		5.34		
V_{OL}	V_I= V_{IH} or V_{IL}	I_{OL} = 20 μA	2V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6V		0.001	0.1		0.1		0.1	
		I_{OL} = 4mA	4.5V		0.17	0.26		0.4		0.33	
		I_{OH} = 5.2mA	6V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O =0	6V			8		160		80	μA
C_i			2V to 6V		3	10		10		10	pF

Timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A =25℃		MC54HC164AN		MC74HC164AN		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Clock frequency		2V		6		4.2		5	MHz
		4.5V		31		21		25	
		6V		36		25		28	
t_W Pulse duration	$\overline{CLR}$ low	2V	100		150		125		ns
		4.5V	20		30		25		
		6V	17		25		21		
	CLK high or low	2V	80		120		100		
		4.5V	16		24		20		
		6V	14		20		18		
t_{su} Setup time before CLK↑	Data	2V	100		150		125		ns
		4.5V	20		30		25		
		6V	17		25		21		
	$\overline{CLR}$ inactive	2V	100		150		125		
		4.5V	20		30		25		
		6V	17		25		21		
t_h Hold time, data after CLK↑		2V	5		5		5		ns
		4.5V	5		5		5		
		6V	5		5		5		

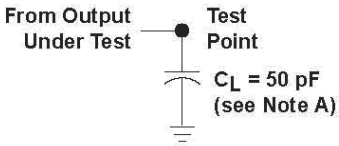
Switching characteristics over recommended operating free-air temperature range, CL = 50pF (unless otherwise noted) (see Figure1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A =25℃			MC54HC164AN		MC74HC164AN		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2V	6	10		4.2		5		MHz
			4.5V	31	54		21		25		
			6V	36	62		25		28		
t_{PHL}	$\overline{CLR}$	Any Q	2V		140	205		295		255	Ns
			4.5V		28	41		59		51	
			6V		24	35		51		46	
t_{pd}	CLK	Any Q	2V		115	175		265		220	
			4.5V		23	35		53		44	
			6V		20	30		45		38	
t_t			2V		38	75		110		95	ns
			4.5V		8	15		22		19	
			6V		6	13		19		16	

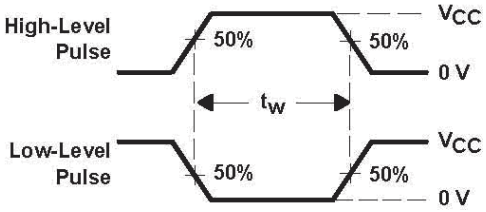
Operating characteristics, T_A = 25℃

PARAMETER	TESTCONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	135	pF

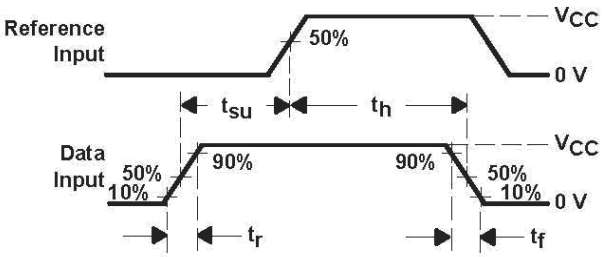
PARAMETER MEASUREMENT INFORMATION



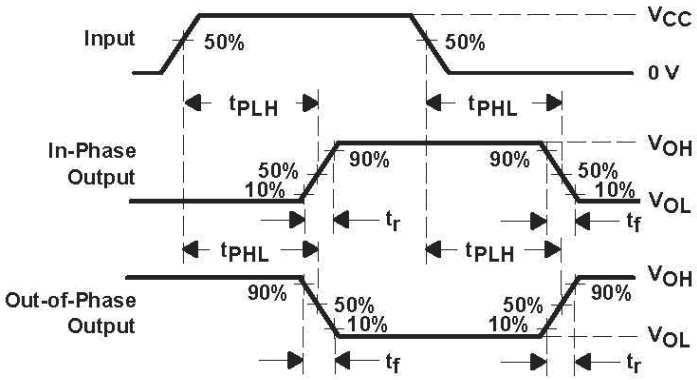
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.

B. Phase relation ships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR≤1MHz, Z_O =50Ω, t_r = 6ns, t_f =6ns.

C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.

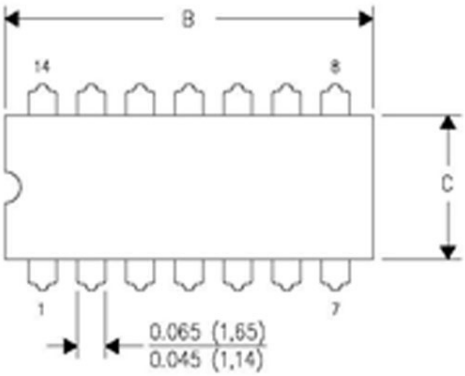
D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

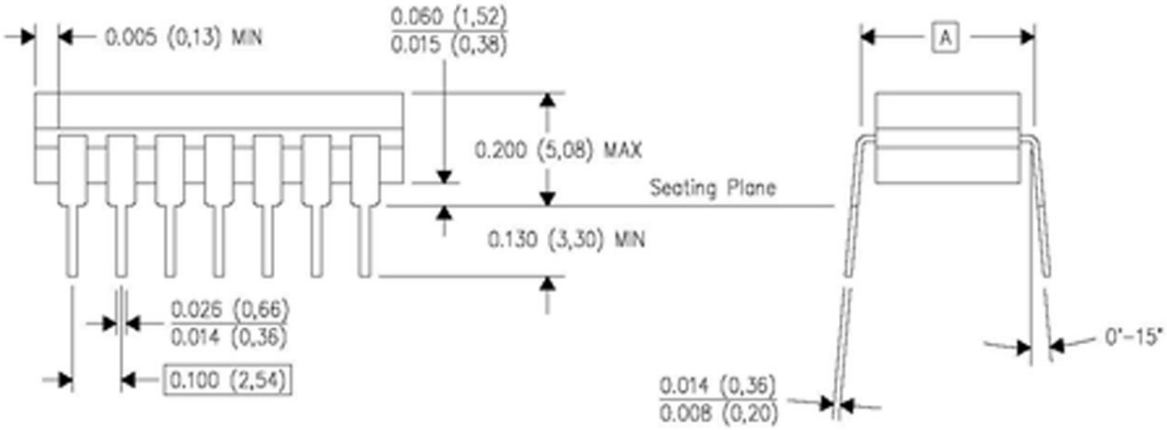
Figure 1. Load Circuit and Voltage Waveforms

J (R –GDIP –T **) **CERAMIC DUAL IN-LINE PACKAGE**

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

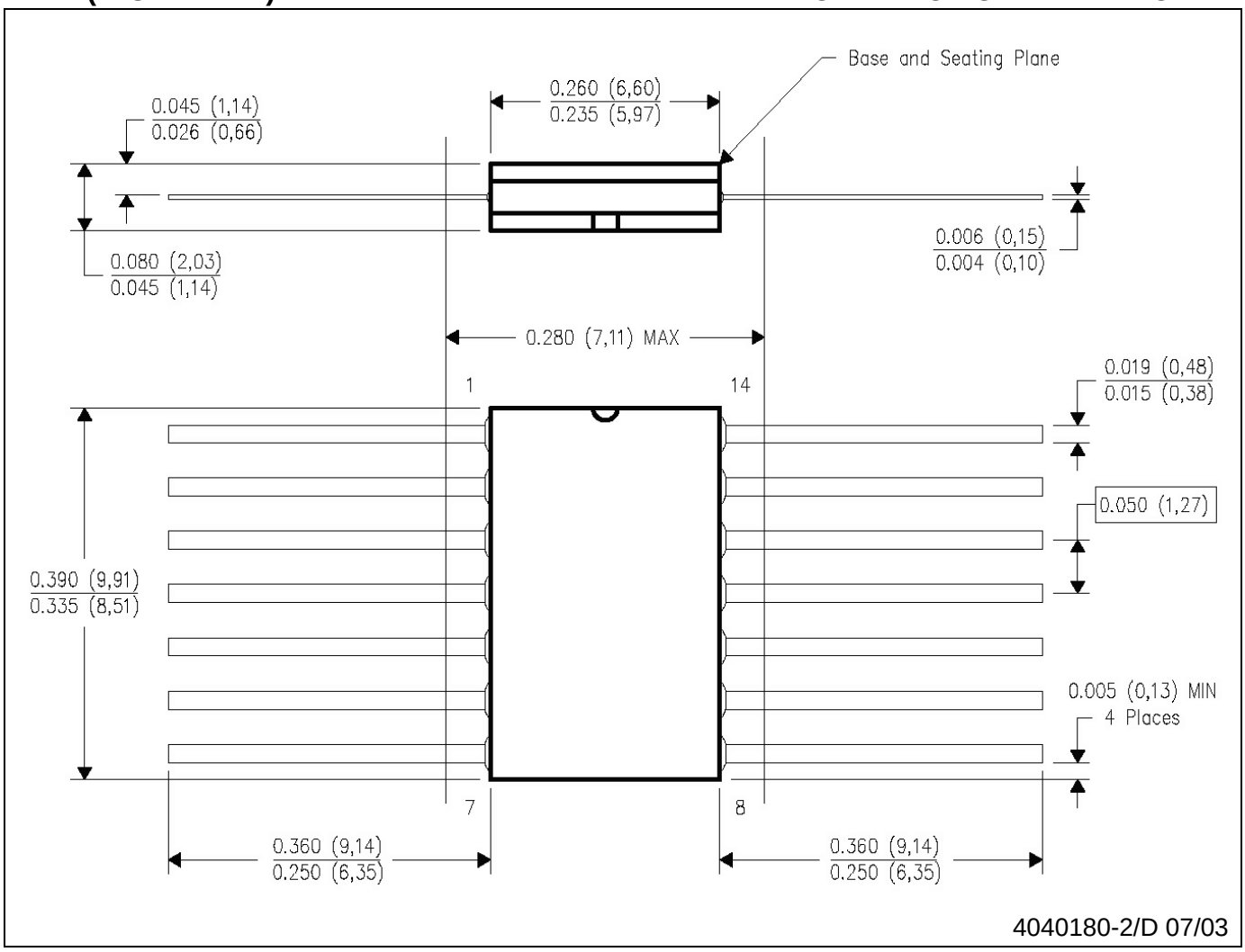


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cop for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W(R-GDFP-F14) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

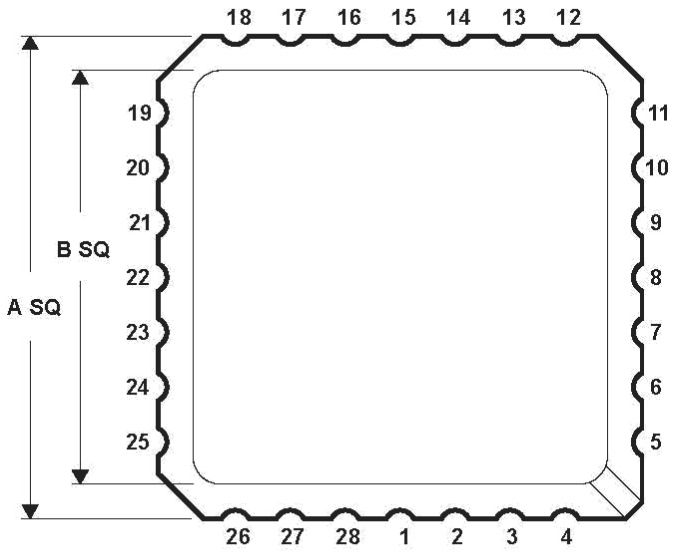
D. Index point is provided on cap for terminal identification only.

E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

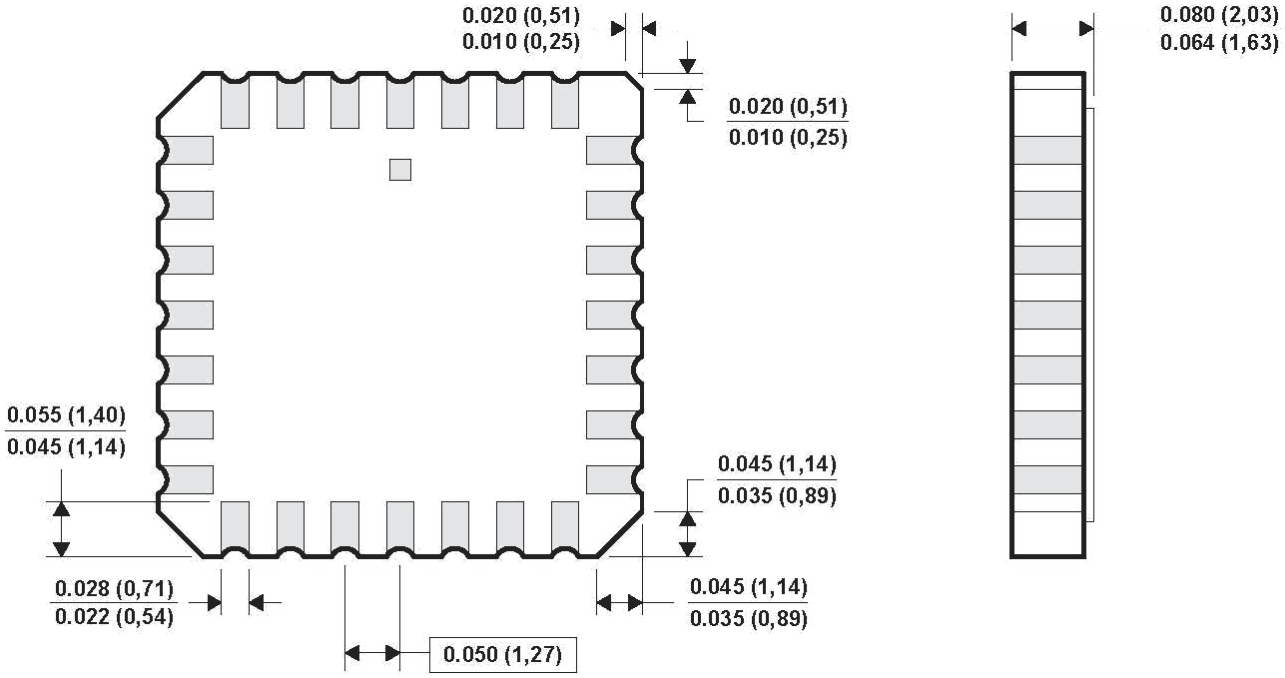
MECHANICAL DATA

FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



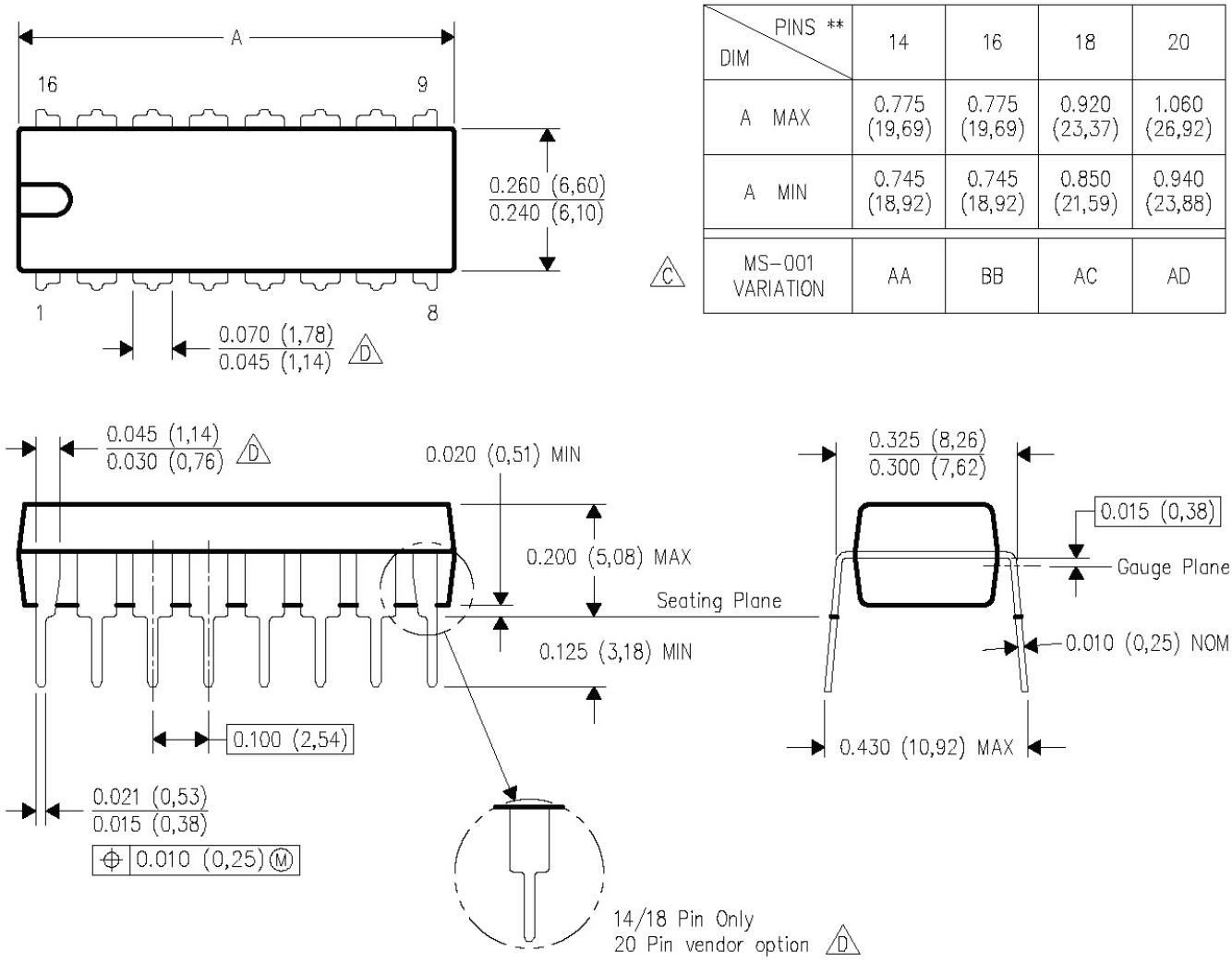
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004.

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).

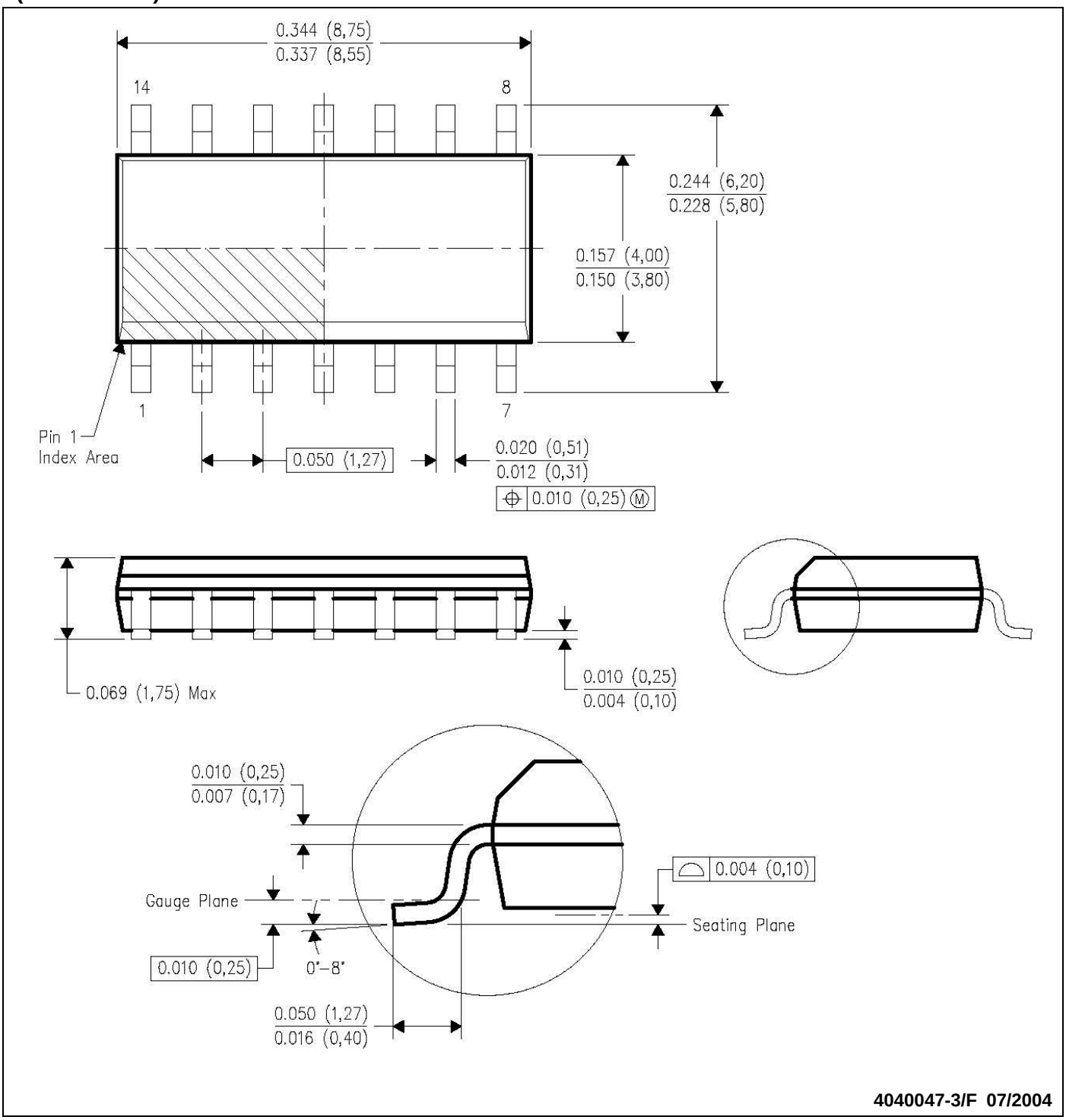
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G14) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

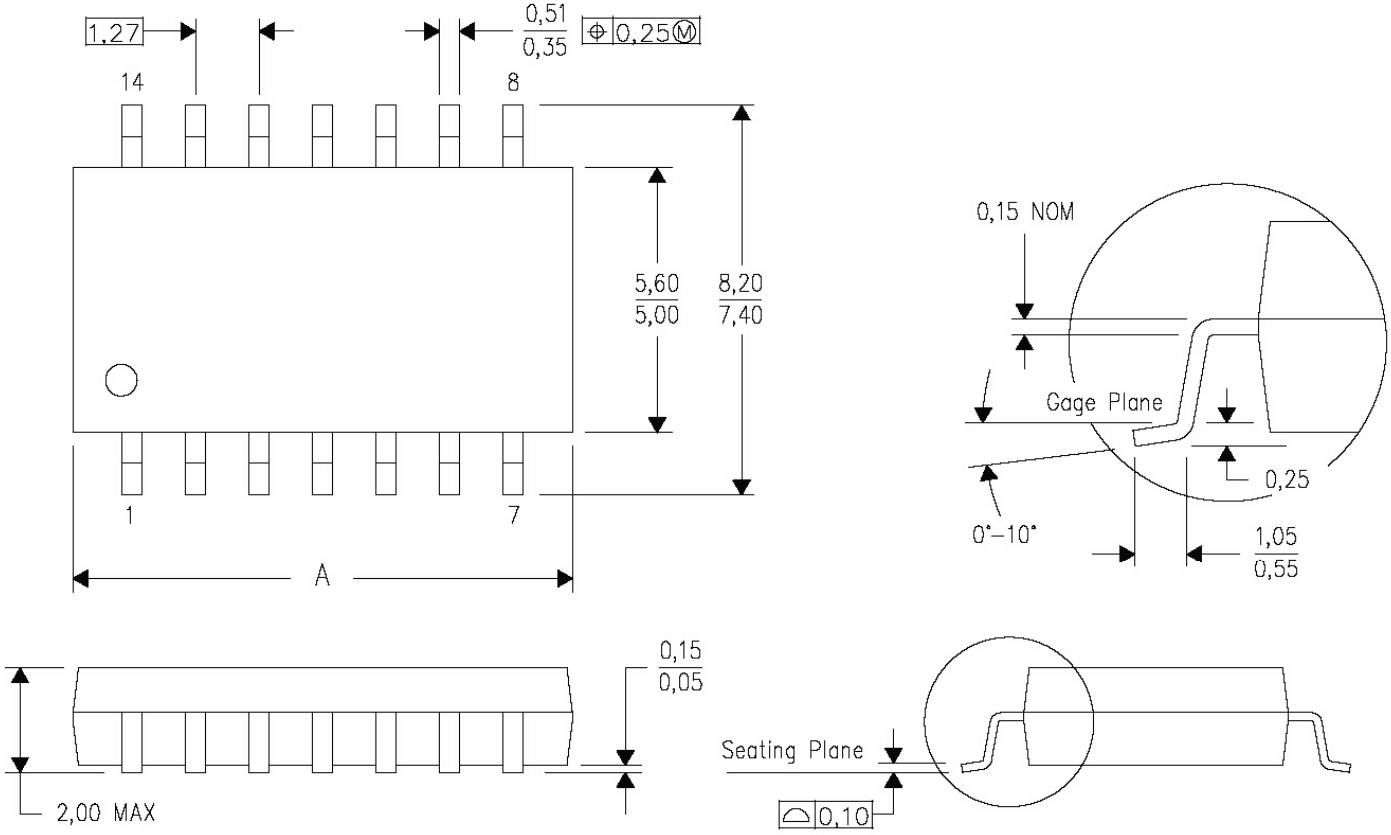
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).

D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS(R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

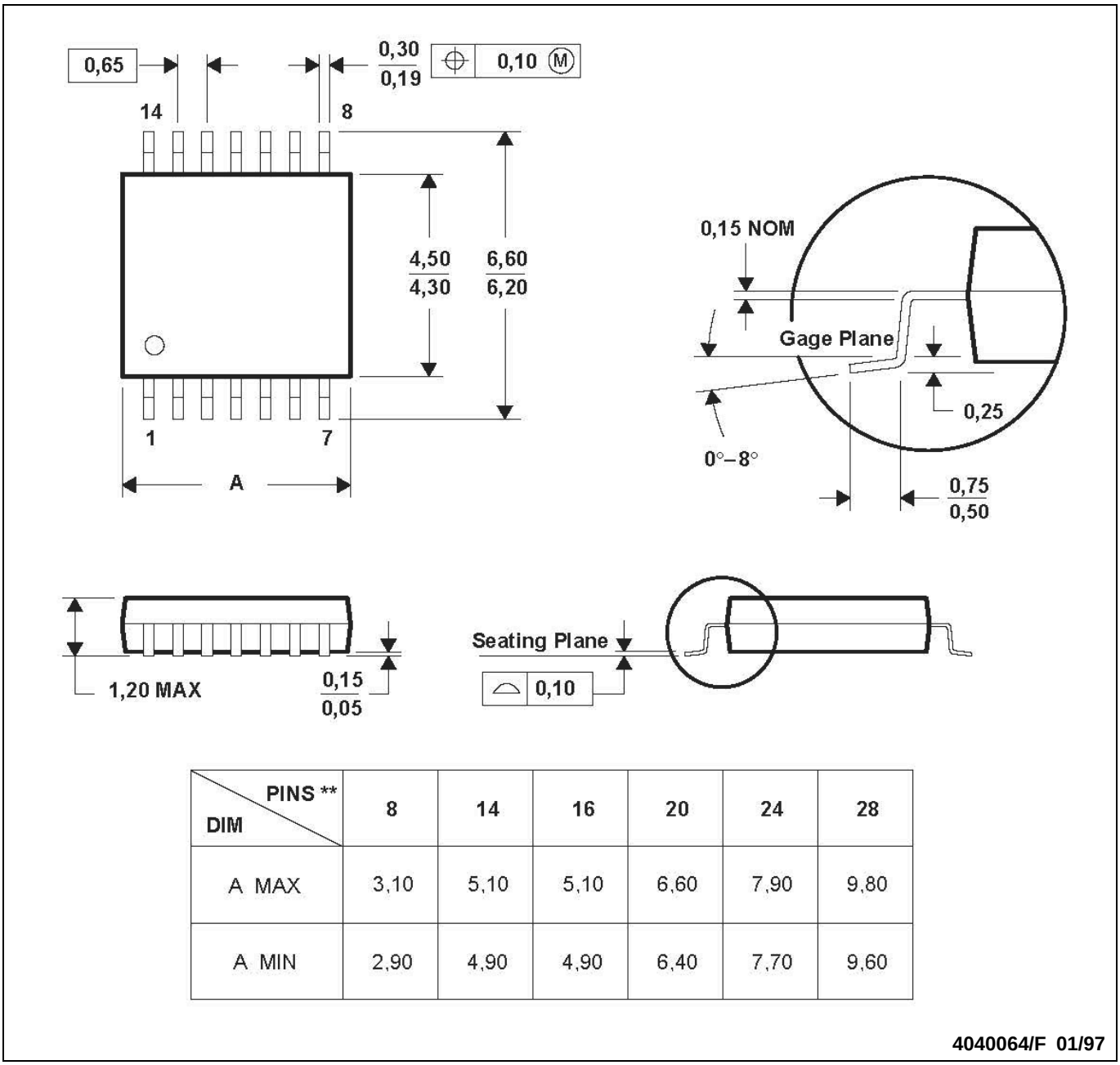
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. Falls within JEDEC MO-153.