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November 2015

FAN7688
Advanced Secondary Side LLC Resonant Converter Controller with Synchronous Rectifier Control

Features

- Secondary Side PFM Controller for LLC Resonant Converter with Synchronous Rectifier Control
- Charge Current Control for Better Transient Response and Easy Feedback Loop Design
- Adaptive Synchronous Rectification Control with Dual Edge Tracking
- Closed Loop Soft-Start for Monotonic Rising Output
- Wide Operating Frequency (39 kHz ~ 690 kHz)
- Green Functions to Improve Light-Load Efficiency
  - Symmetric PWM Control at Light-Load to Limit the Switching Frequency while Reducing Switching Losses
  - Disabling SR at Light-Load Condition
- Protection Functions with Auto-Restart
  - Over-Current Protection (OCP)
  - Output Short Protection (OSP)
  - NON Zero-Voltage Switching Prevention (NZS) by Compensation Cutback (Frequency Shift)
  - Power Limit by Compensation Cutback (Frequency Shift)
  - Overload Protection (OLP) with Programmable Shutdown Delay Time
  - Over-Temperature Protection (OTP)
- Programmable Dead Times for Primary Side Switches and Secondary Side Synchronous Rectifiers
- V_{DD} Under-Voltage Lockout (UVLO)
- Wide Operating Temperature Range -40°C to +125°C

Description

The FAN7688 is an advanced Pulse Frequency Modulated (PFM) controller for LLC resonant converters with Synchronous Rectification (SR) that offers best in class efficiency for isolated DC/DC converters. It employs a current mode control technique based on a charge control, where the triangular waveform from the oscillator is combined with the integrated switch current information to determine the switching frequency. This provides a better control-to-output transfer function of the power stage simplifying the feedback loop design while allowing true input power limit capability. Closed-loop soft-start prevents saturation of the error amplifier and allows monotonic rising of the output voltage regardless of load condition. A dual edge tracking adaptive dead time control minimizes the body diode conduction time thus maximizing efficiency.

Applications

- Desktop ATX, Desktop-Derived Server, Blade Server, and Telecom Power Supplies
- Intelligent 100 W-2 kW+ Off-Line Power Supplies
- High Efficiency Isolated DC-DC Converters
- Large Screen Display Power
- Industrial Power

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN7688SJX	-40° to 125°C	16-Lead, Small-Outline Package	Tape & Reel

Note:

1. All packages are lead free per JEDEC: J-STD-020B standard.

Pin Configuration

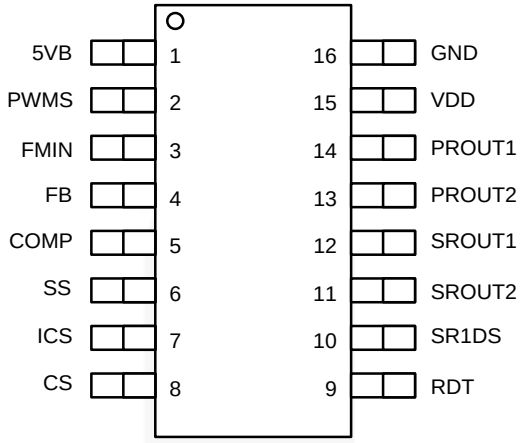


Figure 1. Pin Assignment

Thermal Impedance

Symbol	Parameter	Value	Unit
Θ_{JA}	Junction-to-Ambient Thermal Impedance	102	°C/W

Pin Definitions

Pin#	Name	Pin Description
1	5VB	5 V REF
2	PWMS	PWM mode entry level setting.
3	FMIN	Minimum frequency setting pin.
4	FB	Output voltage sensing for feedback control.
5	COMP	Output of error amplifier.
6	SS	Soft-start time programming pin.
7	ICS	Current information integration pin for current mode control.
8	CS	Current sensing for over current protection.
9	RDT	Dead time programming pin for the primary side switches and secondary side SR switches.
10	SR1DS	SR1 Drain-to-source voltage detection.
11	SROUT2	Gate drive output for the secondary side SR MOSFET 2.
12	SROUT1	Gate drive output for the secondary side SR MOSFET 1.
13	PROUT2	Gate drive output 2 for the primary side switch.
14	PROUT1	Gate drive output 1 for the primary side switch.
15	VDD	IC Supply voltage.
16	GND	Ground.

Typical Application

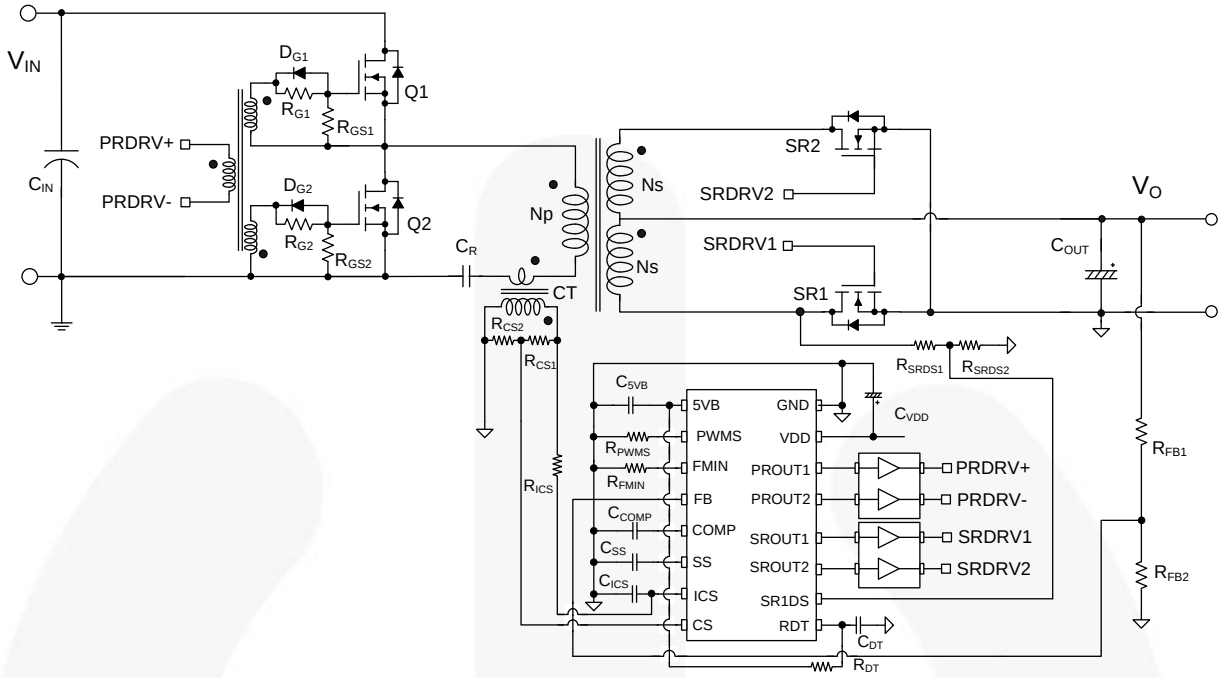


Figure 2. Typical Application

Block Diagram

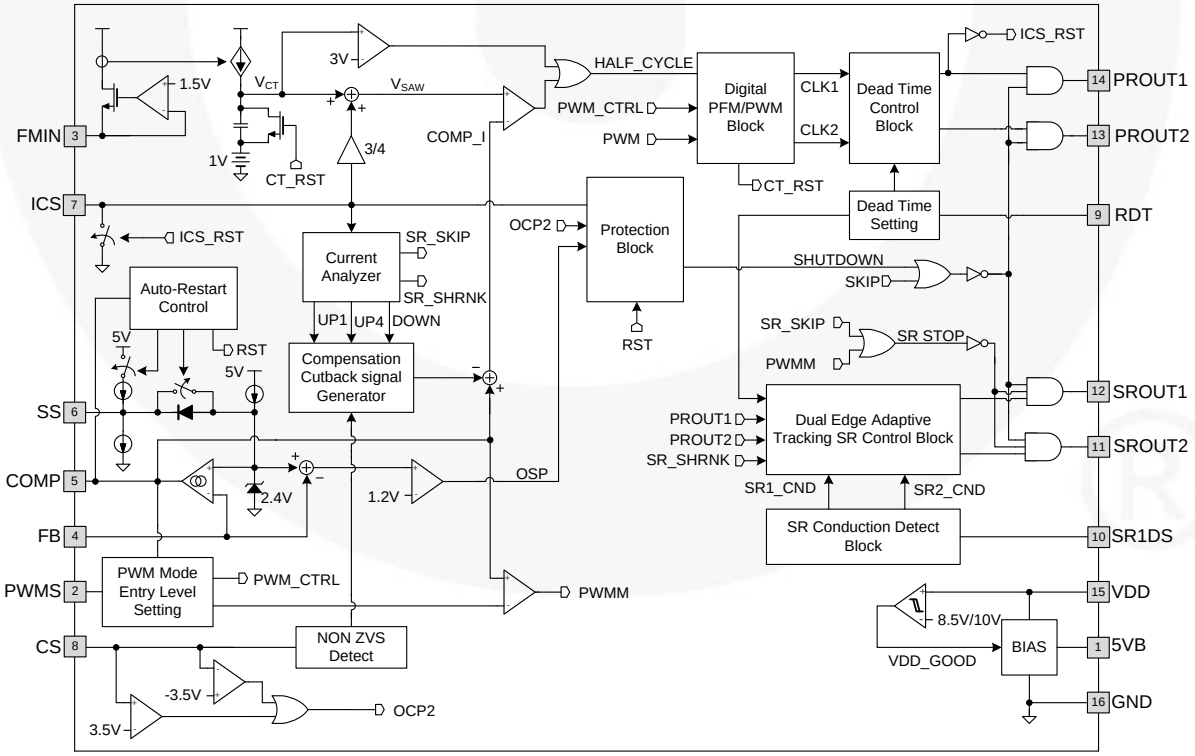


Figure 3. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	VDD Pin Supply Voltage to GND		-0.3	20.0	V
V_{5VB}	5VB Pin Voltage		-0.3	5.5	V
V_{PWMS}	PWMS Pin Voltage		-0.3	5.0	V
V_{FMIN}	FMIN Pin Voltage		-0.3	5.0	V
V_{FB}	FB Pin Voltage		-0.3	5.0	V
V_{COMP}	COMP Pin Voltage		-0.3	5.0	V
V_{SS}	SS Pin Voltage		-0.3	5.0	V
V_{ICS}	ICS Pin Voltage		-0.5	5.0	V
V_{CS}	CS Pin Voltage		-5.0	5.0	V
V_{RDT}	RDT Pin Voltage		-0.3	5.0	V
V_{SR1DS}	SR1DS Pin Voltage		-0.3	5.0	V
V_{PROUT1}	PROUT1 Pin Voltage		-0.3	V_{DD}	V
V_{PROUT2}	PROUT2 Pin Voltage		-0.3	V_{DD}	V
V_{SROUT1}	SROUT1 Pin Voltage		-0.3	V_{DD}	V
V_{SROUT2}	SROUT2 Pin Voltage		-0.3	V_{DD}	V
T_J	Junction Temperature		-40	+150	ºC
T_L	Lead Soldering Temperature (10 Seconds)			+260	ºC
T_{STG}	Storage Temperature		-65	+150	ºC
ESD	Electrostatic Discharge Capability	Human Body Model, JEDEC JESD22-A114		3	kV
		Charged Device Model, JEDEC JESD22-C101		2	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the data sheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	VDD Pin Supply Voltage to GND	0	18	V
V_{5VB}	5VB Pin Voltage	0	5	V
V_{INS}	Signal Input Voltage	0	5	V
T_A	Operating Ambient Temperature	-25	+105	ºC

Electrical Characteristics

Unless otherwise noted, V_{DD} = 12 V, C_{5VB} = 33 nF and T_J = -40°C to +125°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (VDD Pin)						
$I_{STARTUP}$	Startup Supply Current	V_{DD} = 9 V		80	115	µA
I_{DD}	Operating Current	V_{COMP} = 0.1 V		2.8		mA
I_{DD_DYM1}	Dynamic Operating Current	f_{SW} = 100 kHz; C_L=1 nF, with PR Operation Only		10		mA
I_{DD_DYM2}	Dynamic Operating Current	f_{SW} = 100 kHz; C_L = 1 nF, with PR & SR Operation		13		mA
$V_{DD.ON}$	VDD ON Voltage (VDD Rising)		9	10	11	V
$V_{DD.OFF}$	VDD OFF Voltage (VDD Falling)			8.5		V
$V_{DD.HYS}$	UVLO Hysteresis		1	1.5	2	V
Reference Voltage						
V_{5VB}	5 V Reference	T_A = 25°C	4.94	5.00	5.06	V
		-40°C< T_A< 125°C	4.9	5.0	5.1	V
Error Amplifier (COMP Pin)						
$V_{SS.CLMP}$	Voltage Feedback Reference	T_J = 25°C	2.37	2.40	2.43	V
		-40°C< T_J< 125°C	2.35	2.40	2.45	V
gM	Error Amplifier Gain Transconductance		210	300	390	µmho
I_{COMP1}	Error Amplifier Maximum Output Current (Sourcing)	V_{FB} = 1.8 V, VCOMP = 2.5 V	70	90	110	µA
I_{COMP2}	Error Amplifier Maximum Output Current (Sinking)	V_{FB} = 3.0 V, VCOMP = 2.5 V	70	90	110	µA
$V_{COMP.CLMP1}$	Error Amplifier Output High Clamping Voltage	V_{FB} = 1.8 V	4.2	4.4	4.6	V
$V_{COMP.PWM}$	V_{COMP} Internal Clamping Voltage for PWM Operation	RPWM = Open	1.35	1.50	1.65	V
		RPWM = 200 k	1.45	1.60	1.75	V
		RPWM = 50 k	1.75	1.90	2.05	V
V_{PWMS}	PWMS Pin Voltage	RPWM = 200 k	1.9	2.0	2.1	V
$V_{COMP.SKP}$	VCOMP Threshold for Entering Skip Cycle Operation		1.15	1.25	1.35	V
$V_{COMP.SKP.HYS}$	VCOMP Threshold Hysteresis for Entering Skip Cycle Operation			50		mV
Dead Time (DT Pin)						
I_{DT}	Dead-Time Programming Current	V_{RDT} = 1.2 V	140	150	160	µA
V_{THDT1}	First Threshold for Dead-Time Detection		0.9	1.0	1.1	V
V_{THDT2}	Second Threshold for Dead-Time Detection		2.8	3.0	3.2	V
$V_{RDT.ON}$	$V_{RDT\ ON}$ Voltage (VRDT Rising)		1.2	1.4	1.6	V

Electrical Characteristics (Continued)

Unless otherwise noted, V_{DD} = 12 V, C_{5VB} = 33 nF and T_J = -40°C to +125°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Soft-Start (SS Pin)						
$I_{SS.T}$	Total Soft-Start Current (Including $I_{SS.UP}$)	V_{SS} = 1 V	32	40	48	µA
V_{OLP}	Overload Protection Threshold		3.45	3.60	3.75	V
$I_{SS.UP}$	Soft-Start Capacitor Charge Current for Delayed Shutdown	V_{SS} = 3 V	8.4	10.5	12.6	µA
$I_{SS.DN}$	Soft-Start Capacitor Discharge Current	V_{SS} = 3 V	8.4	10.5	12.6	µA
$V_{SS.MAX}$	SS Capacitor Maximum Charging Voltage		4.5	4.7	4.9	V
$V_{SS.INIT}$	SS Capacitor Initialization Voltage		0.05	0.10	0.20	V
Feedback (FB Pin)						
$V_{FB.OVP1}$	VFB Threshold for Entering Skip Cycle Operation	V_{COMP} = 3 V	2.53	2.65	2.77	V
$V_{FB.OVP2}$	VFB Threshold for Exiting Skip Cycle Operation	V_{COMP} = 3 V	2.18	2.30	2.42	V
$V_{ERR.OSP}$	Error Voltage to Enable Output Short Protection (OSP)	V_{SS} = 2.4 V	1.0	1.2	1.4	V
Oscillator						
V_{FMIN}	FMIN Pin Voltage	R_{FIMN} = 10 kΩ,	1.4	1.5	1.6	V
f_{OSC}	PROUT Switching Frequency	R_{MINF} = 10 kΩ, V_{CS} = 1 V V_{COMP} = 4.0 V, V_{ICS} = 0 V	96	100	104	kHz
$f_{OSC.min}$	Minimum PROUT Switching Frequency (40 MHz/1024)	R_{MINF} = 40 kΩ, V_{CS} = 1 V V_{COMP} = 4.0 V, V_{ICS} = 0 V	36	39	42	kHz
$f_{OSC.max}$	Maximum PROUT Switching Frequency (40 MHz/58)	R_{MINF} = 2 kΩ, V_{CS} = 1 V V_{COMP} = 2.0 V, V_{ICS} = 0 V	635	690	735	kHz
D	PROUT Duty Cycle in PFM Mode	R_{MINF} = 20 kΩ, V_{CS} = 1 V V_{COMP} = 4.0 V		50		%
Integrated Current Sensing (ICS Pin):						
$V_{ICS.CLMP}$	ICS Pin Signal Clamping Voltage	I_{CS} = 400 µA		10	50	mV
$R_{DS-ON.ICS}$	ICS Pin Clamping MOSFET R_{DS-ON}	I_{CS} = 1.5 mA		20		Ω
V_{TH1}	SR_SHRNK Enable Threshold	V_{COMP} = 2.4 V	0.15	0.20	0.25	V
$V_{TH1.HYS}$	SR_SHRNK Disable Hysteresis	V_{COMP} = 2.4 V		50		mV
V_{TH2}	SR_SKIP Disable Threshold	V_{COMP} = 2.4 V	0.10	0.15	0.20	V
V_{TH3}	SR_SKIP Enable Threshold	V_{COMP} = 2.4 V	0.025	0.075	0.125	V
V_{OCL1}	Over-Current Limit First Threshold	V_{COMP} = 2.4 V	1.12	1.20	1.28	V
V_{OCL2}	Over-Current Limit Second Threshold	V_{COMP} = 2.4 V	1.34	1.45	1.56	V
$V_{OCL1.BR}$	Over-Current Limit First Threshold in Deep Below Resonance Operation	V_{COMP} = 2.4 V	1.34	1.45	1.56	V
$V_{OCL2.BR}$	Over-Current Limit Second Threshold in Deep Below Resonance Operation	V_{COMP} = 2.4 V	1.59	1.70	1.81	V
V_{OCP1}	Over-Current Protection Threshold	V_{COMP} = 2.4 V	1.77	1.90	2.03	V
$V_{OCP1.BR}$	Over-Current Protection Threshold Below Resonance Operation	V_{COMP} = 2.4 V	2.02	2.15	2.28	V
$T_{OCP1.DLY}$[1]	Debounce Time for Over-Current Protection 1			150		ns

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise noted, V_{DD} = 12 V, C_{5VB} = 33 nF and T_J = -40°C to +125°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current Sensing (CS Pin)						
V_{OCP2P}	Over-Current Protection Threshold		3.3	3.5	3.7	V
$T_{OCP2.DLY}$[1]	Debounce Time for Over-Current Protection 2			150		ns
V_{OCP2N}	Over-Current Protection Threshold		-4.0	-3.5	-3.0	V
$V_{CS.NZVS}$	CS Signal Threshold for Non-ZVS Detection	V_{COMP} = 3.5 V	0.24	0.30	0.36	V
$V_{COMP.NZVS}$	COMP Threshold for Non-ZVS Detection	V_{CS} = 0.1 V	2.7	3.0	3.3	V
Gate drive (PROUT1 and PROUT2)						
I_{SINK}	PROUT Sinking Current	V_{PROUT1} & V_{PROUT2} = 6 V		140		mA
I_{SOURCE}	PROUT Sourcing Current	V_{PROUT1} & V_{PROUT2} = 6 V		150		mA
$t_{PR.RISE}$	Rise Time	V_{DD} = 12 V, C_L = 1 nF, 10% to 90%		100		ns
$t_{PR.FALL}$	Fall Time	V_{DD} = 12 V, C_L = 1 nF, 90% to 10%		85		ns
TSD[1]	Thermal Shutdown Temperature		120	135	150	ºC
Synchronous Rectification (SR) Control						
T_{RC_SRCD}[(2)]	Internal RC Time Constant SR Conduction Detection		50	100	150	ns
$V_{SRCD.OFFSET1}$[(2)]	Internal Comparator Offset Rising Edge Detection		0.15	0.25	0.35	V
$V_{SRCD.OFFSET2}$[(2)]	Internal Comparator Offset Falling Edge Detection		0.10	0.20	0.30	V
$V_{SRCD.LOW}$	SR Conduction Detect threshold		0.4	0.5	0.6	V
$T_{DLY.CMP.SR}$	SR Conduction Detect Comparator Delay			65		ns
$V_{FB.SR.ON}$	SR Enable FB Voltage		1.6	1.8	2.0	V
$V_{FB.SR.OFF}$	SR Disable FB Voltage		1.0	1.2	1.4	V
SR Output (SROUT1 and SROUT2)						
$I_{SR.SINK}$	PROUT Sinking Current	V_{SROUT1} & V_{SROUT2} = 6 V		140		mA
$I_{SR.SOURCE}$	PROUT Sourcing Current	V_{SROUT1} & V_{SROUT2} = 6 V		150		mA
$t_{SR.RISE}$	Rise Time	V_{DD} = 12 V, C_L = 1 nF, 10% to 90%		100		ns
$t_{SR.FALL}$	Fall Time	V_{DD} =12 V, C_L = 1 nF, 90% to 10%		85		ns

Note:

2. These parameters, although guaranteed by design, are not production tested

Typical Performance Characteristics

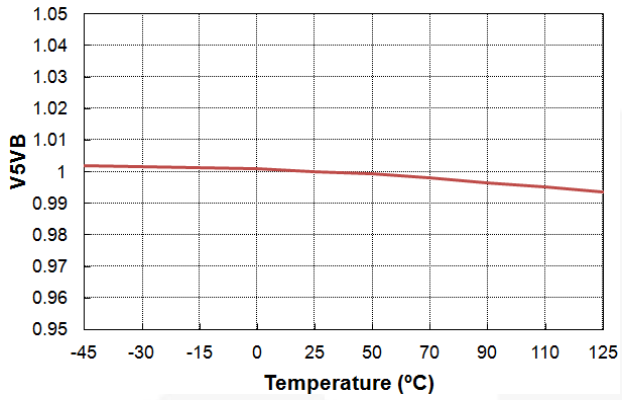


Figure 4. V5VB vs. Temperature

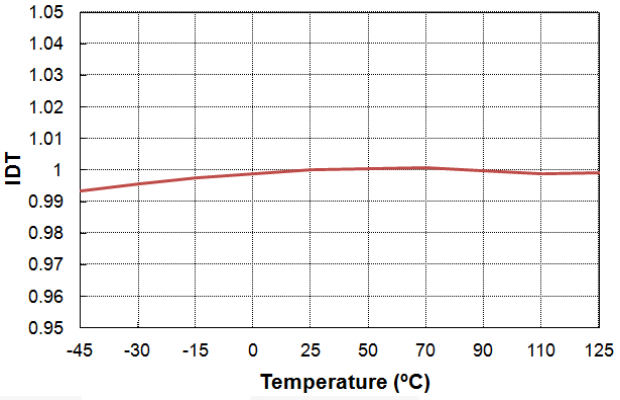


Figure 5. IDT vs. Temperature

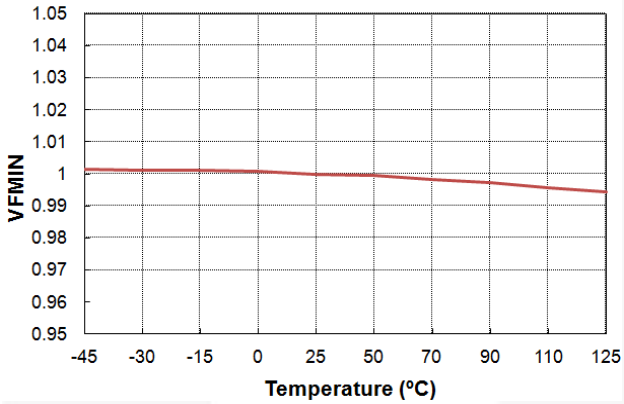


Figure 6. VFMIN vs. Temperature

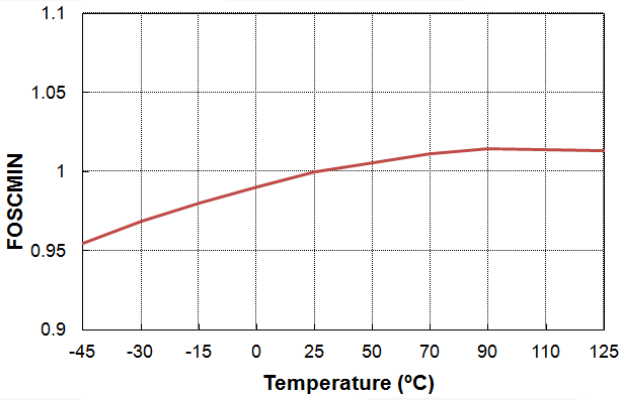


Figure 7. FOSCMIN vs. Temperature

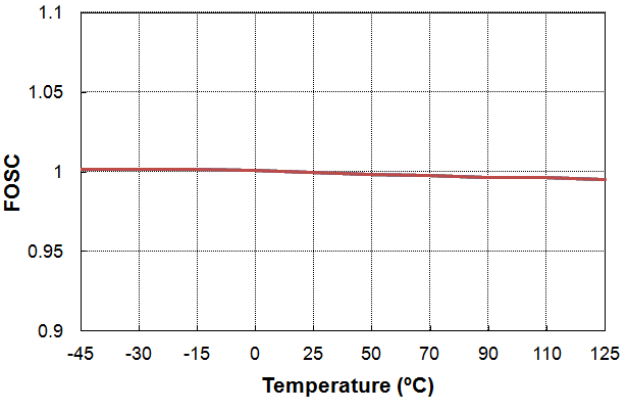


Figure 8. FOCS vs. Temperature

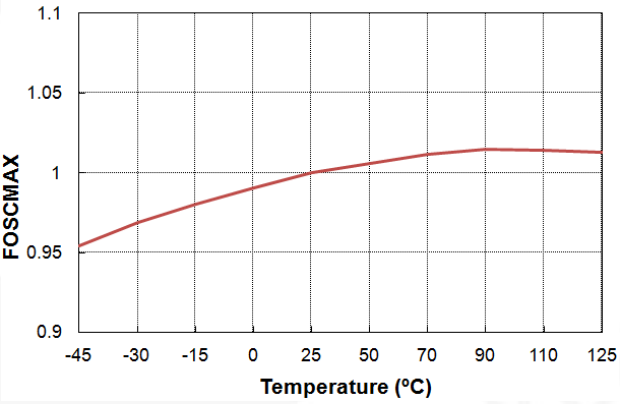


Figure 9. FOSCMAX vs. Temperature

Typical Performance Characteristics

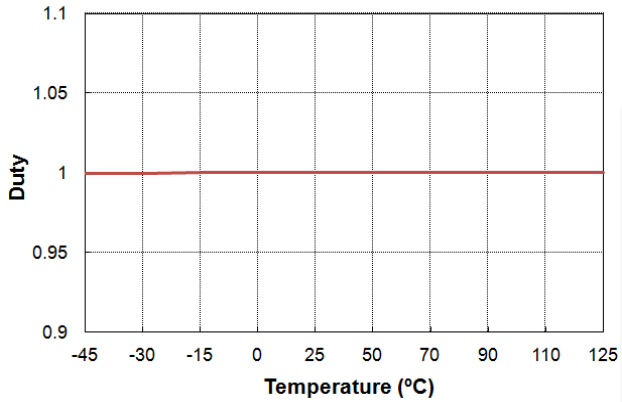


Figure 10. DUTY CYCLE vs. Temperature

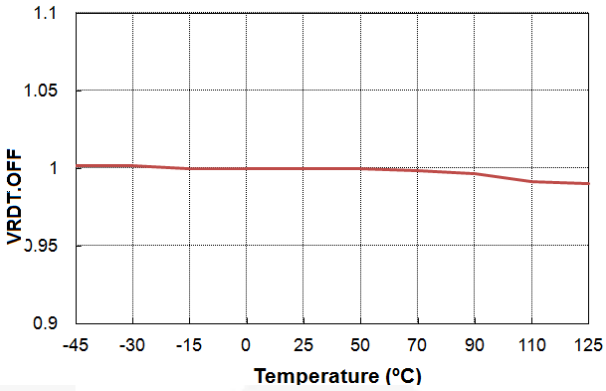


Figure 11. VRDT.OFF vs. Temperature

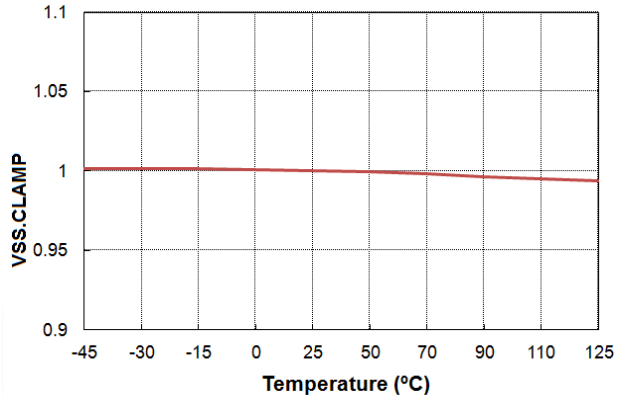


Figure 12. VSS.CLAMP vs. Temperature

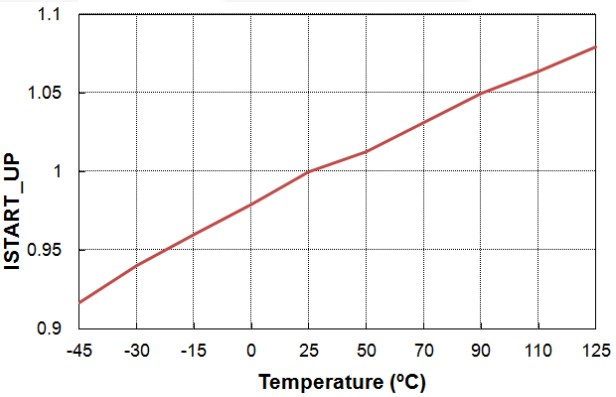


Figure 13. ISTART_UP vs. Temperature

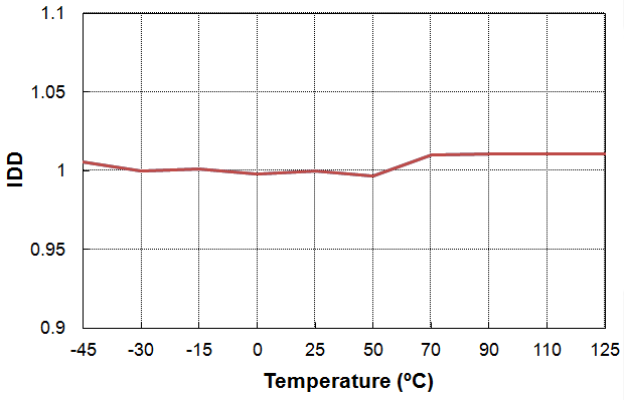


Figure 14. IDD vs. Temperature

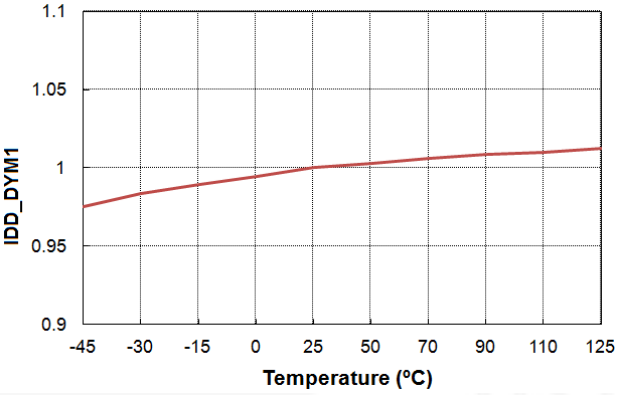


Figure 15. IDD_DYM1 vs. Temperature

Typical Performance Characteristics

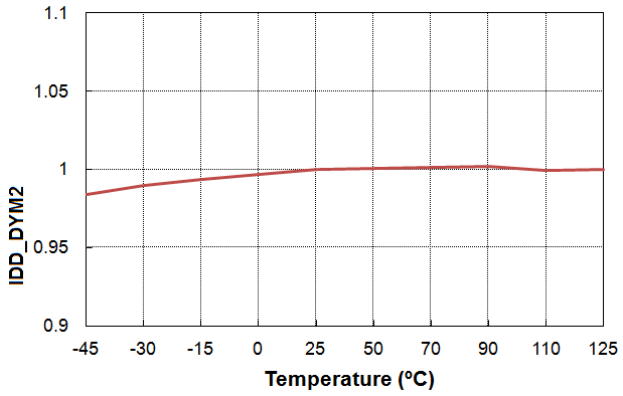


Figure 16. IDD_DYM2 vs. Temperature

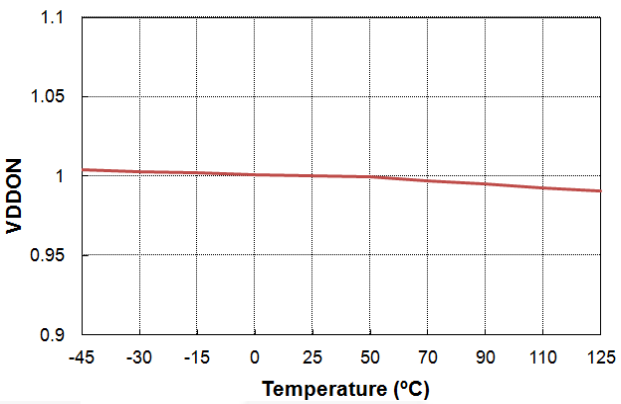


Figure 17. VDDON vs. Temperature

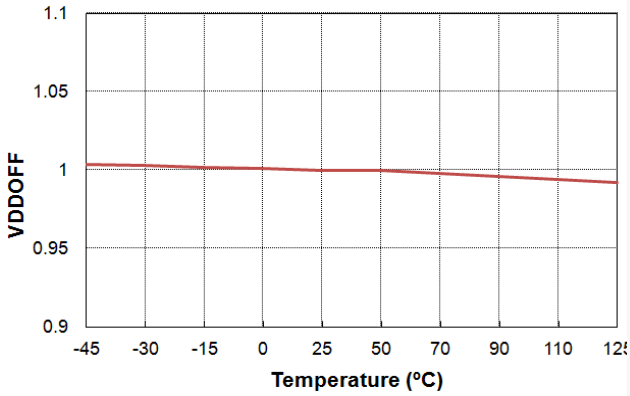


Figure 18. VDDOFF vs. Temperature

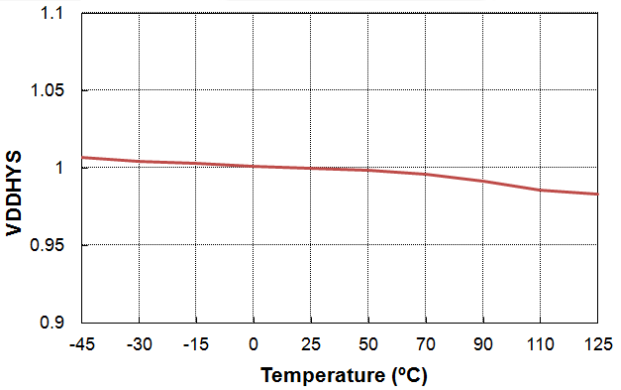


Figure 19. VDDHYS vs. Temperature

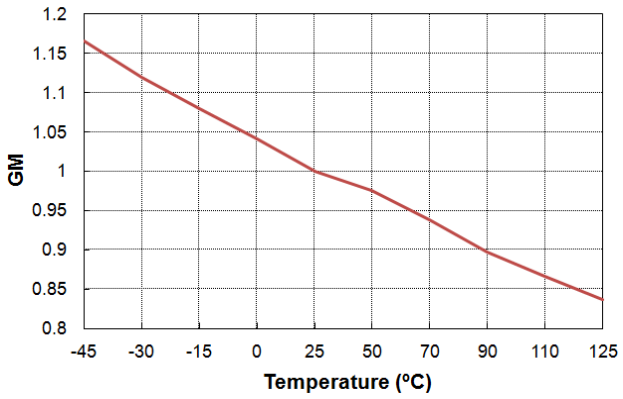


Figure 20. GM vs. Temperature

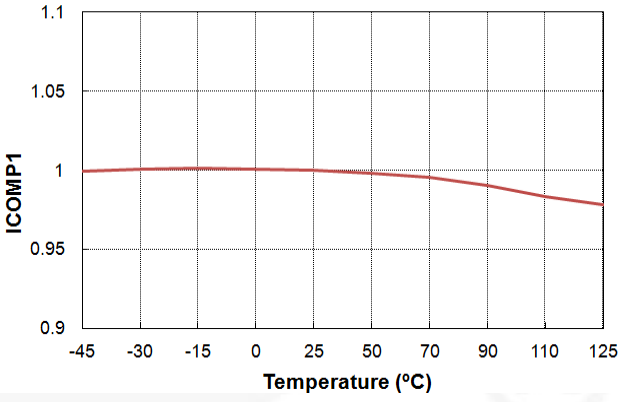


Figure 21. ICOMP1 vs. Temperature

Typical Performance Characteristics vs. Temperature

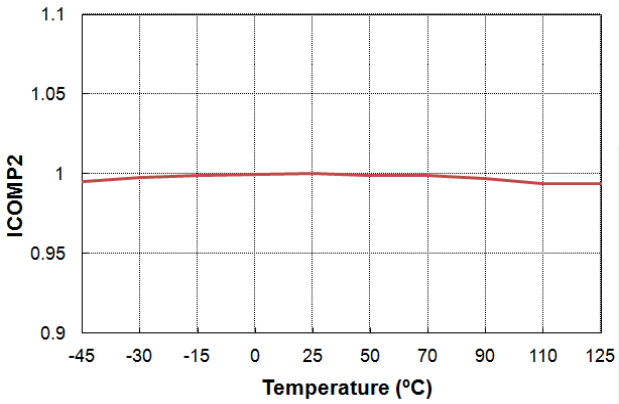


Figure 22. ICOMP2 vs. Temperature

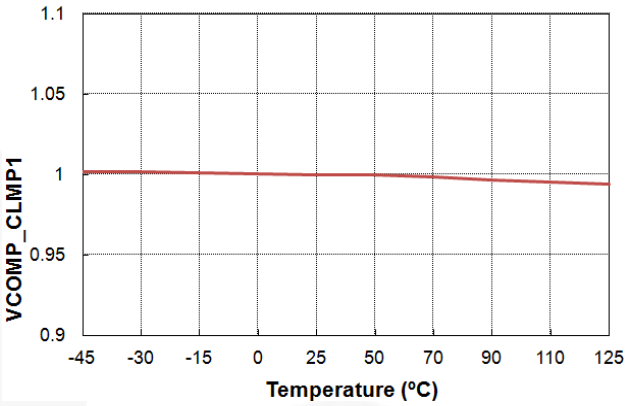


Figure 23. VCOMP_CLMP1 vs. Temperature

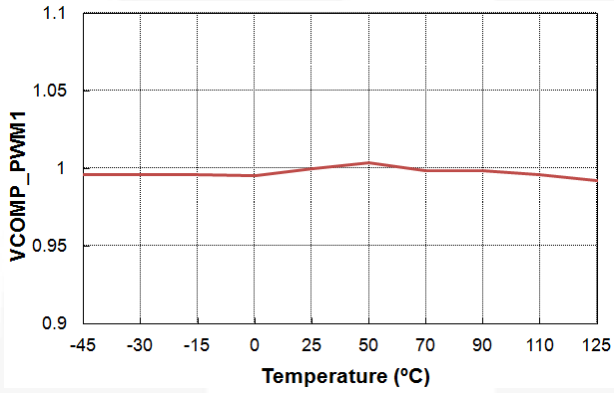


Figure 24. VCOMP_PWM vs. Temperature

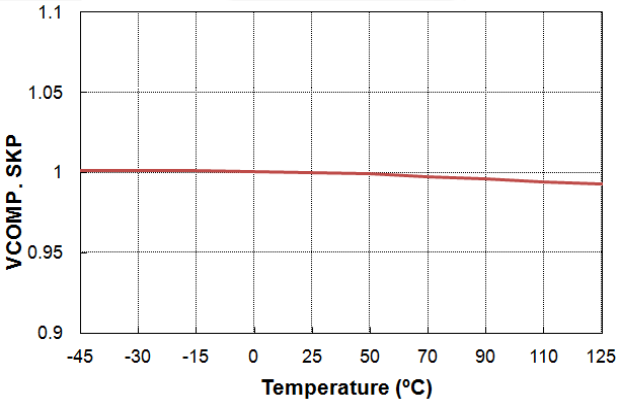


Figure 25. VCOMP.SKIP vs. Temperature

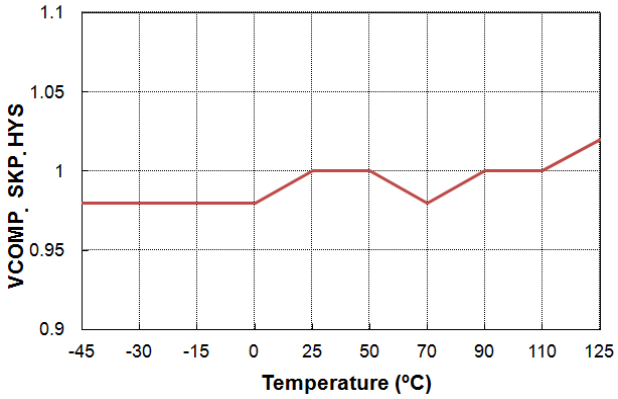


Figure 26. VCOMP.SKIP.HYS vs. Temperature

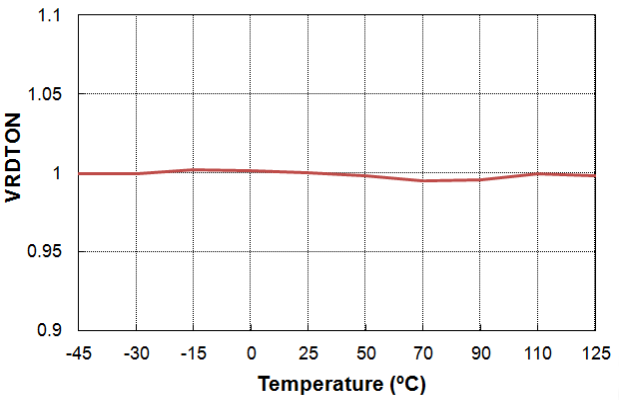


Figure 27. VRDTON vs. Temperature

Typical Performance Characteristics vs. Temperature

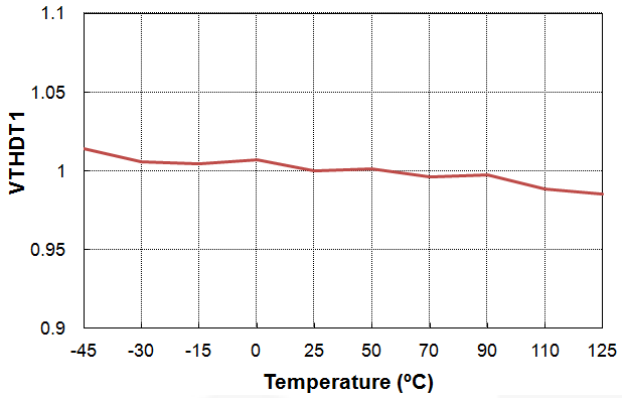


Figure 28. VTHDT1 vs. Temperature

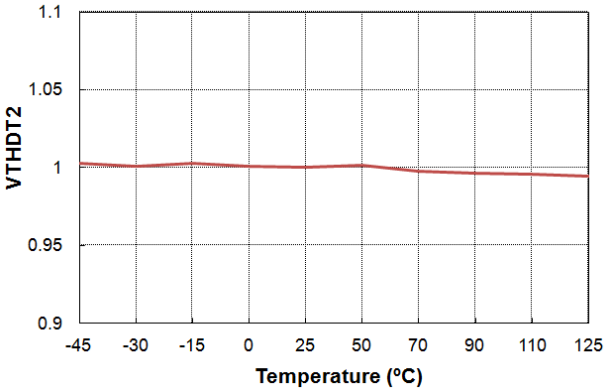


Figure 29. VTHDT2 vs. Temperature

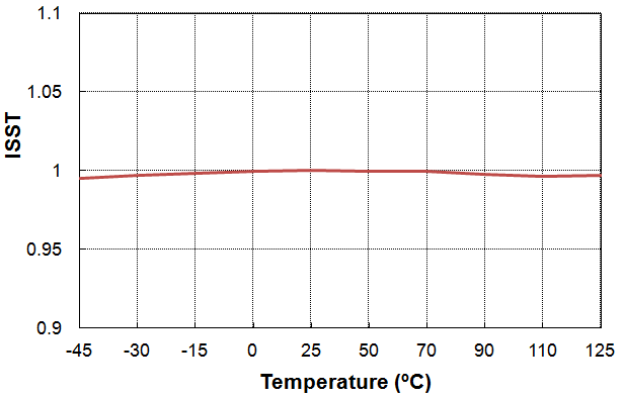


Figure 30. ISST vs. Temperature

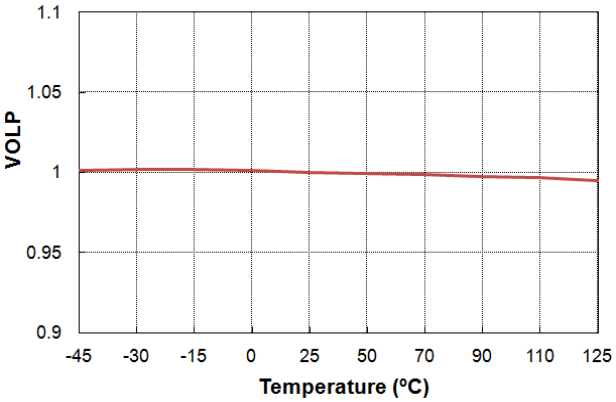


Figure 31. VOLP vs. Temperature

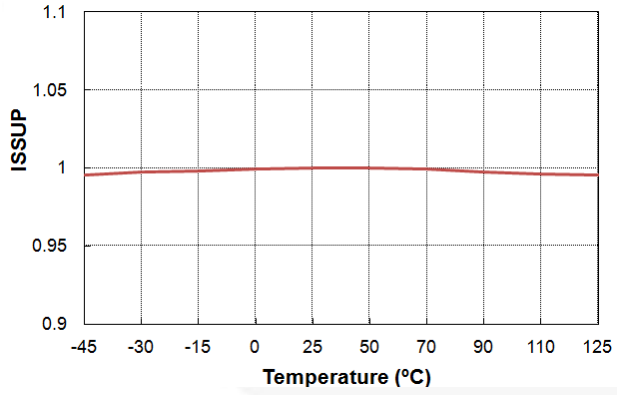


Figure 32. ISSUP vs. Temperature

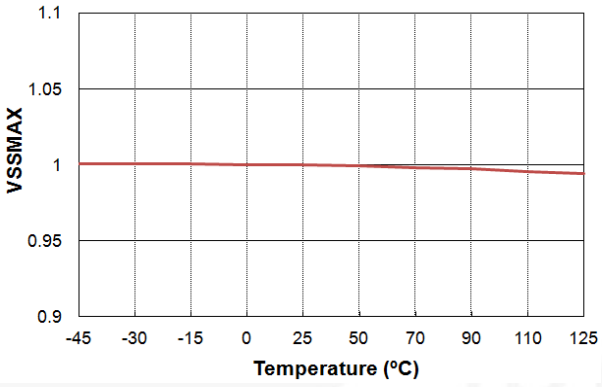


Figure 33. VSSMAX vs. Temperature

Typical Performance Characteristics vs. Temperature

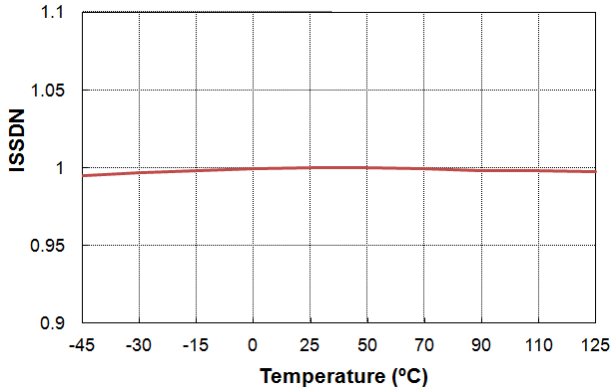


Figure 34. ISSDN vs. Temperature

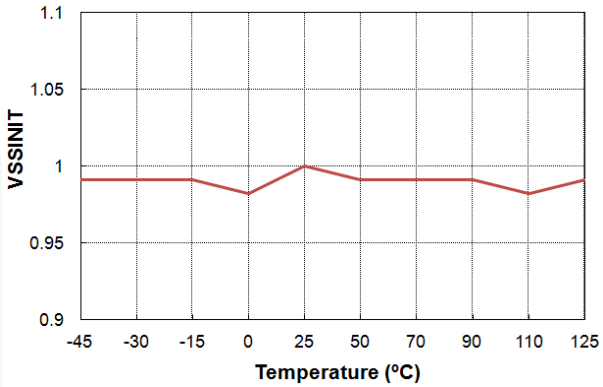


Figure 35. VSSINIT vs. Temperature

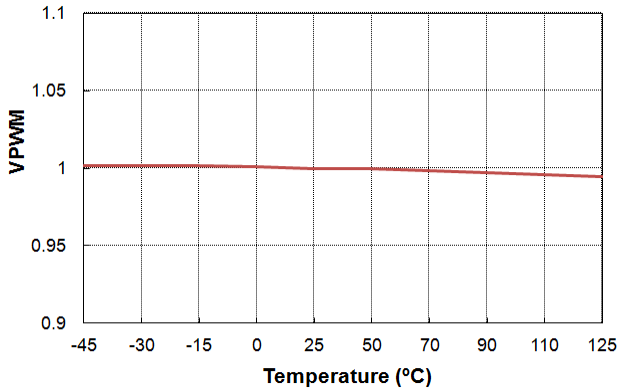


Figure 36. VPWM vs. Temperature

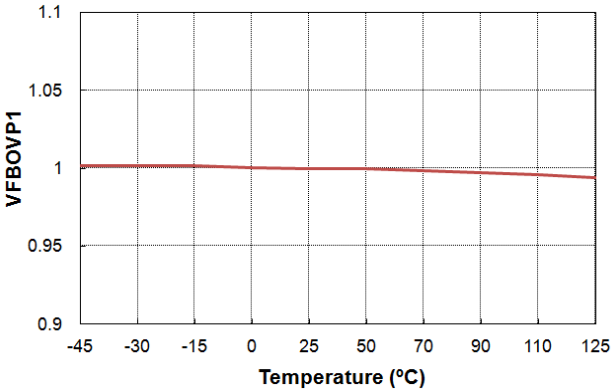


Figure 37. VFBOVP1 vs. Temperature

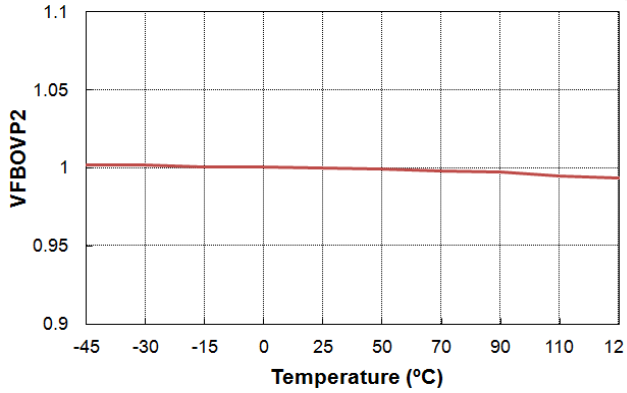


Figure 38. VFBOVP2 vs. Temperature

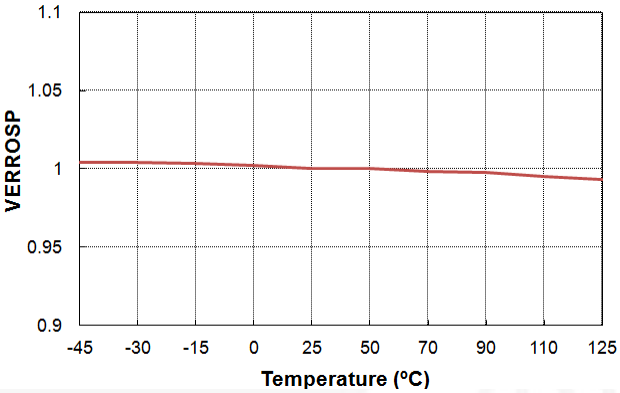


Figure 39. VERROSP vs. Temperature

Typical Performance Characteristics vs. Temperature

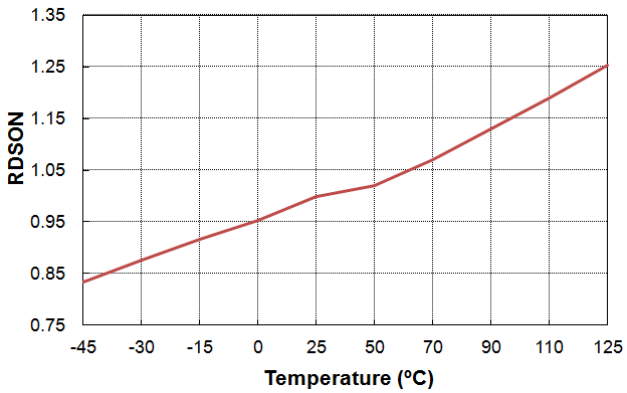


Figure 40. RDSON vs. Temperature

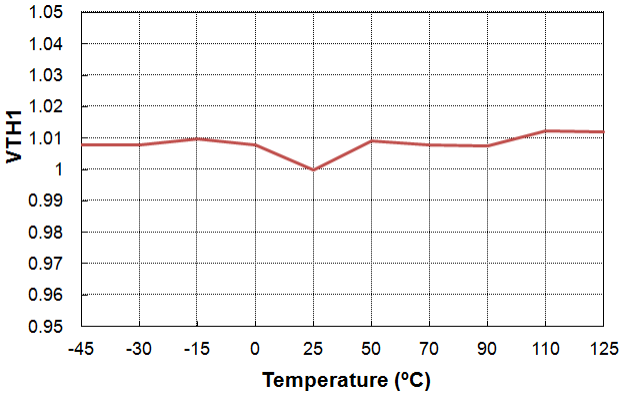


Figure 41. VTH1 vs. Temperature

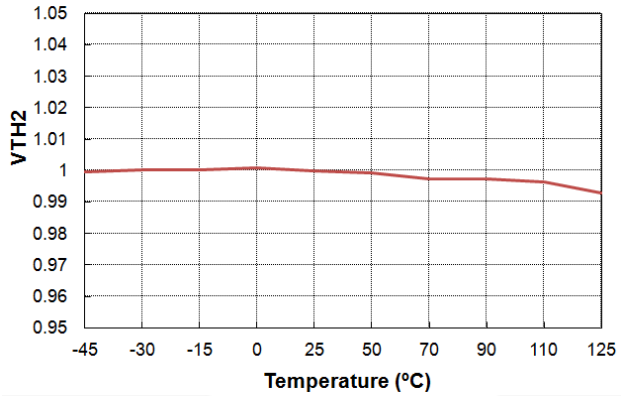


Figure 42. VTH2 vs. Temperature

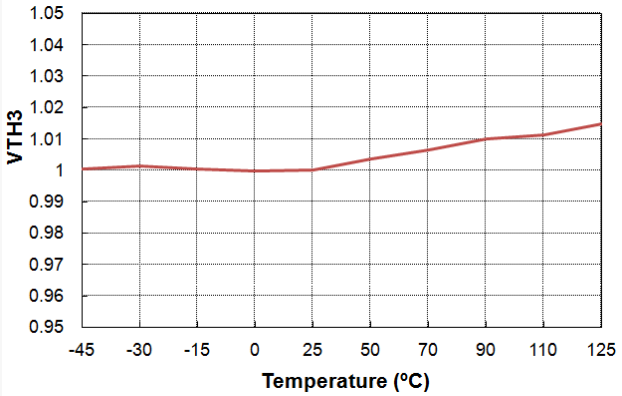


Figure 43. VTH3 vs. Temperature

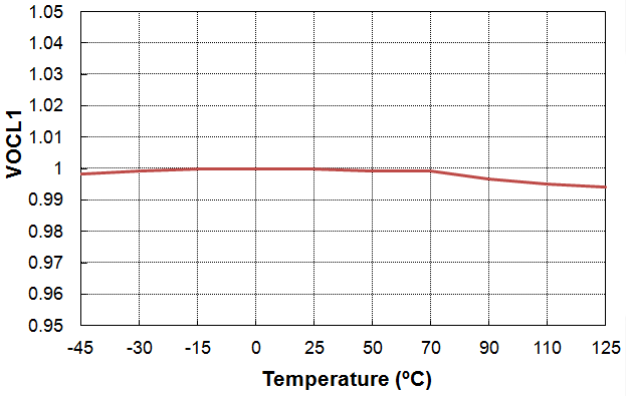


Figure 44. VOCL1 vs. Temperature

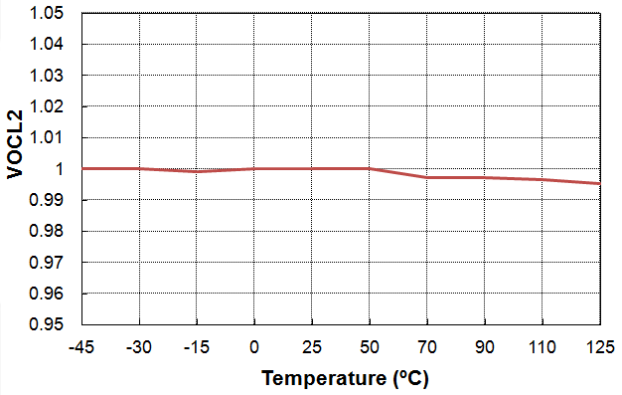


Figure 45. VOCL2 vs. Temperature

Typical Performance Characteristics vs. Temperature

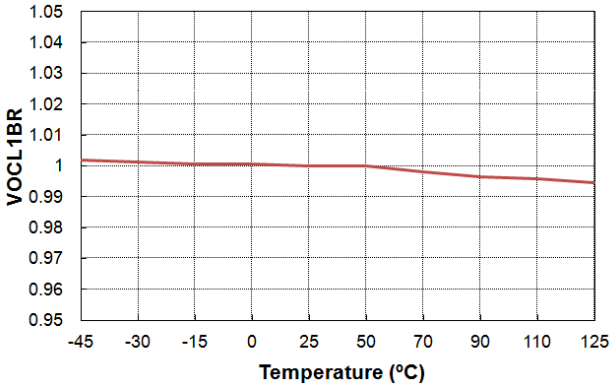


Figure 46. VOCL1BR vs. Temperature

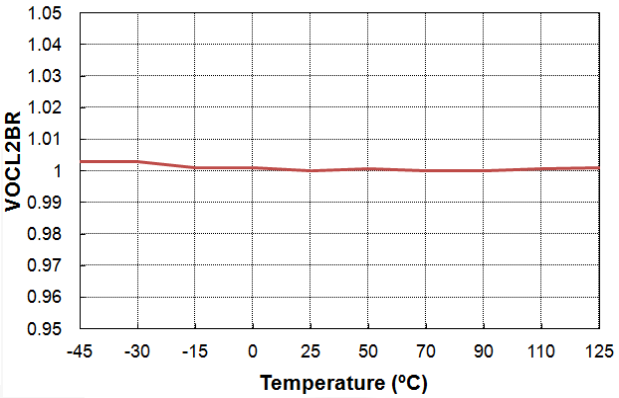


Figure 47. VOCL2BR vs. Temperature

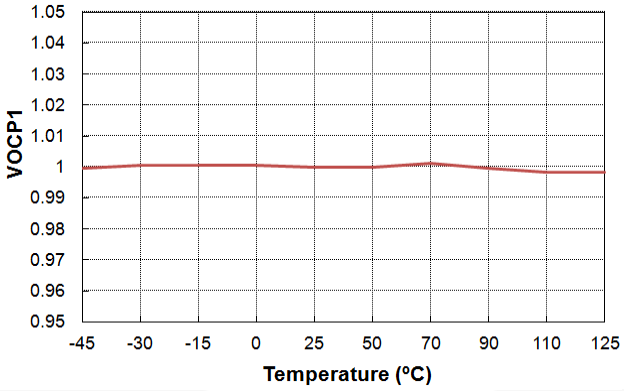


Figure 48. VOCP1 vs. Temperature

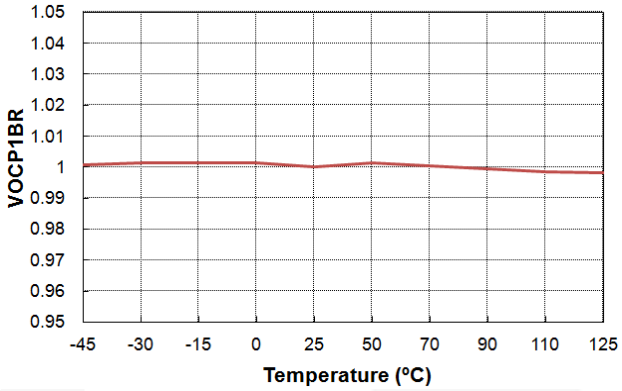


Figure 49. VOCP1BR vs. Temperature

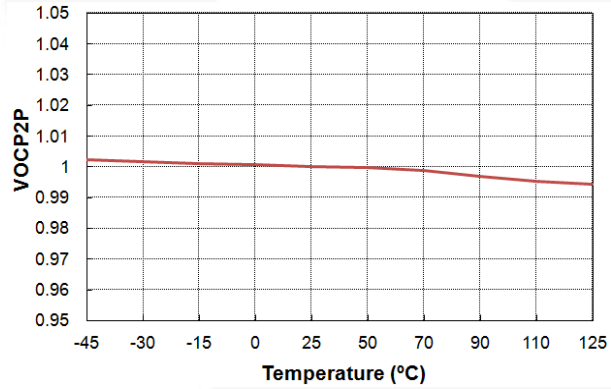


Figure 50. VOCP2P vs. Temperature

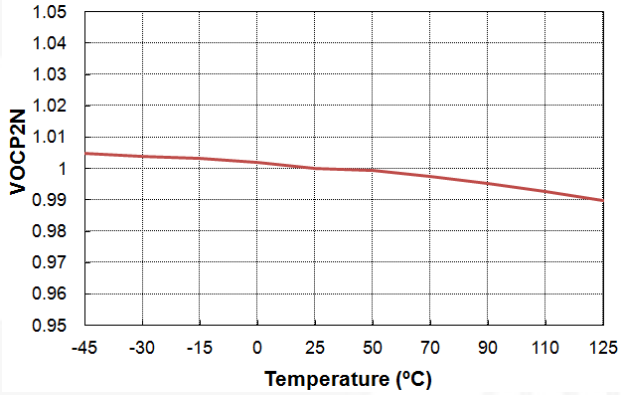


Figure 51. VOCP2N vs. Temperature

Typical Performance Characteristics vs. Temperature

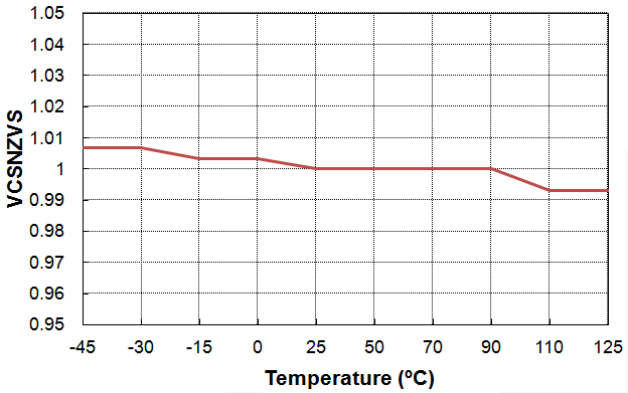


Figure 52. VCSNZVS vs. Temperature

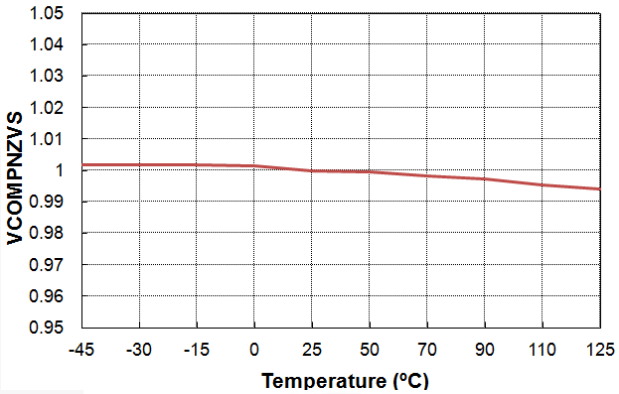


Figure 53. VCOMPNZVS vs. Temperature

Functional Description

Operation Principle of Charge Current Control

The LLC resonant converter has been widely used for many applications because it has many advantages. It can regulate the output over entire load variations with a relatively small variation of switching frequency. It can achieve Zero Voltage Switching (ZVS) for the primary side switches and Zero Current Switching (ZCS) for the secondary side rectifiers over the entire operating range and the resonant inductance can be integrated with the transformer into a single magnetic component. Figure 54 shows the simplified schematic of the LLC resonant converter where voltage mode control is employed. Voltage mode control is typically used for the LLC resonant converter where the error amplifier output voltage directly controls the switching frequency. However, the compensation network design of the LLC resonant converter is relatively challenging since the frequency response with voltage mode control includes four poles where the location of the poles changes with input voltage and load variations.

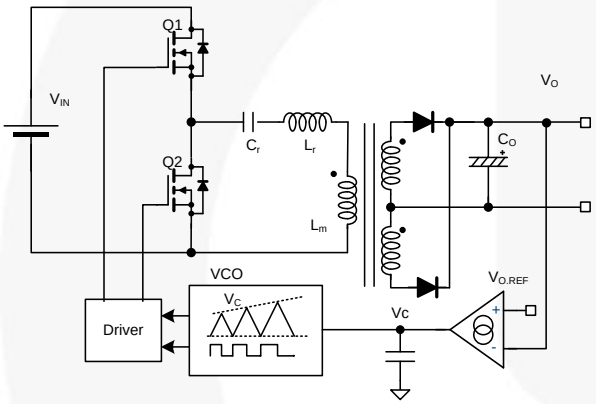


Figure 54. LLC Resonant Converter with Voltage Mode Control

FAN7688 employs charge current mode control to improve the dynamic response of the LLC resonant converter. Figure 55 shows the simplified schematic of a half-bridge LLC resonant converter using FAN7688, where Lm is the magnetizing inductance, Lr is the resonant inductor and Cr is the resonant capacitor. Typical key waveforms of the LLC resonant converter for heavy load and light load conditions are illustrated in Figure 56 and Figure 57, respectively. It is assumed that the operation frequency is same as the resonance frequency, as determined by the resonance between Lr and Cr. Since the primary-side switch current does not increase monotonically, the switch current itself cannot be used for pulse-frequency-modulation (PFM) for the output voltage regulation. Also, the peak value of the primary-side current does not reflect the load condition properly because the large circulating current (magnetizing current) is included in the primary-side switch current. However, the integral of the switch current (V_{ICS}) does increase monotonically and has a peak value similar to that used for peak current mode control, as shown in Figure 56 and Figure 57.

Thus, FAN7688 employs charge current control, which compares the total charge of the switch current (integral of switch current) to the control voltage to modulate the switching frequency. Since the charge of the switch current is proportional to the average input current over one switching cycle, charge control provides a fast inner loop and offers excellent transient response including inherent line feed-forward. The PFM block has an internal timing capacitor (CT) whose charging current is determined by the current flowing out of the FMIN pin. The FMIN pin voltage is regulated at 1.5 V. There is an upper limit (3 V) for the timing capacitor voltage, which determines the minimum switching frequency for a given resistor connected to the FMIN pin. The sawtooth waveform (V_{SAW}) is generated by adding the integral of the Q1 switch current (V_{ICS}) and the timing capacitor voltage (V_{CT}) of the oscillator. The sawtooth waveform (Vsaw) is then compared with the compensation voltage (V_{COMP}) to determine the switching frequency.

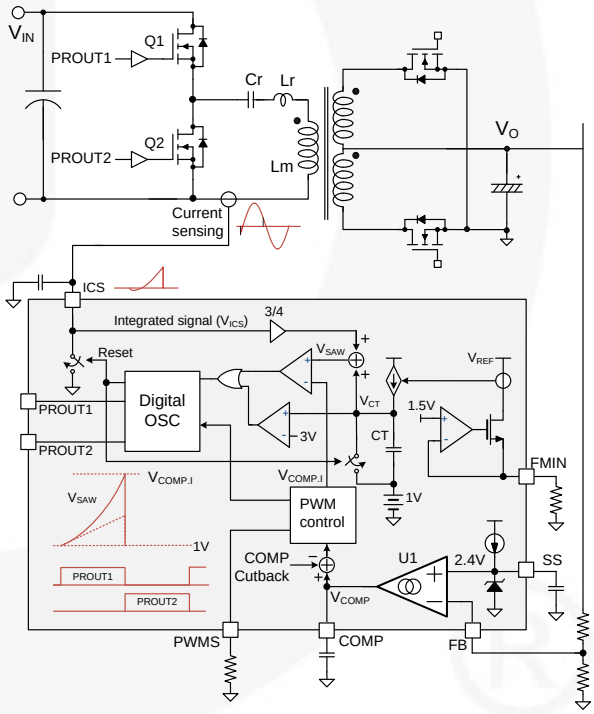


Figure 55. Schematic of LLC resonant Converter Power Stage Schematic

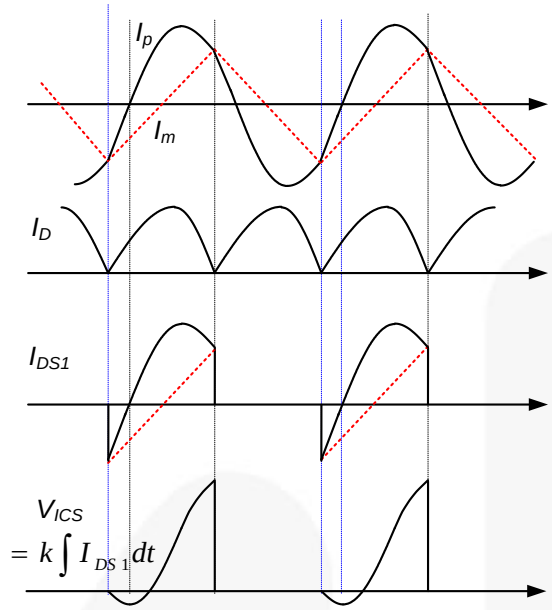


Figure 56. Typical Waveforms of the LLC Resonant Converter for Heavy Load Condition

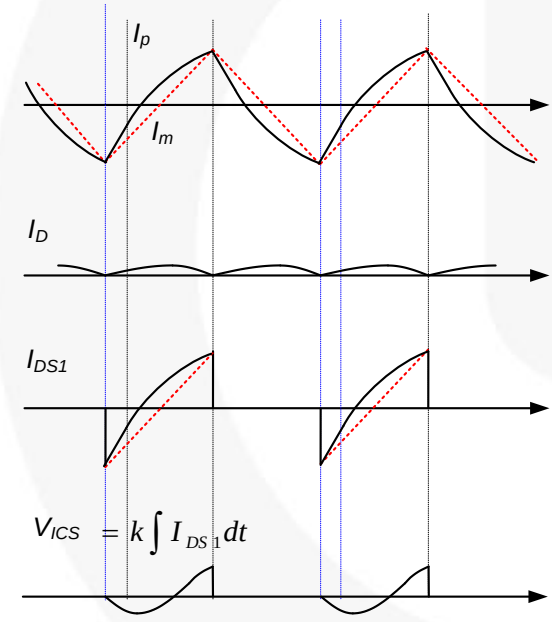


Figure 57. Typical Waveforms of LLC Resonant Converter for Light-Load Condition

Hybrid Control (PWM+PFM)

The conventional PFM control method modulates only the switching frequency with a fixed duty cycle of 50%, which typically results in relatively poor light load efficiency due to the large circulating primary side current. To improve the light load efficiency, FAN7688 employs hybrid control where the PFM is switched to pulse width modulation (PWM) mode at light load as illustrated in Figure 58. The typical waveforms for PFM mode and PWM mode are shown in Figure 59 and Figure 60, respectively. When the error amplifier voltage (VCOMP) is below the PWM mode threshold, the internal COMP signal is clamped at the threshold level and the PFM operation switches to PWM mode. In PWM mode, the switching frequency is fixed by the clamped internal COMP voltage (VCOMPI) and the duty cycle is determined by the difference between COMP voltage and the PWM mode threshold voltage. Thus, the duty cycle decreases as VCOMP drops below the PWM mode threshold, which limits the switching frequency at light load condition as illustrated in Figure 58. The PWM mode threshold can be programmed between 1.5 V and 1.9 V using a resistor on the PWMS pin.

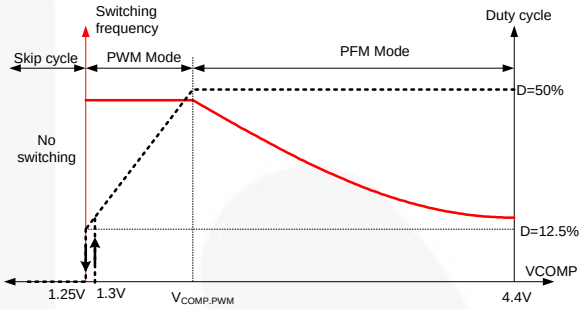


Figure 58. Mode Change with COMP Voltage

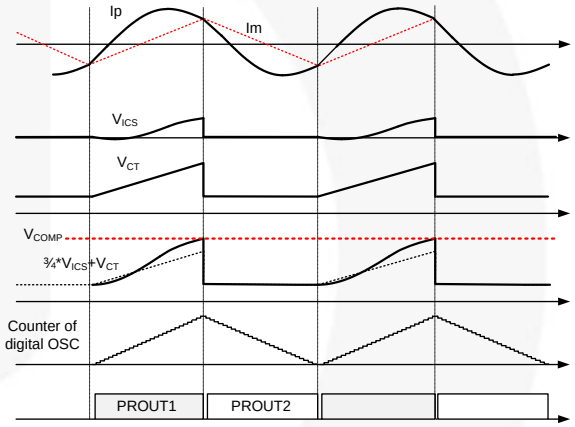


Figure 59. Key Waveforms of PFM Operation

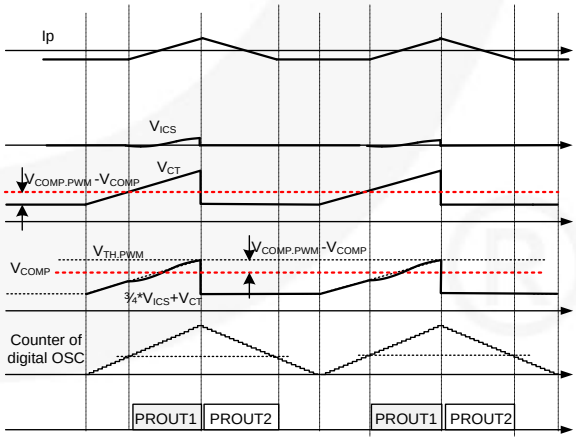


Figure 60. Key Waveforms of PWM Operation

Current Sensing

FAN7688 senses instantaneous switch current and the integral of the switch current as illustrated in Figure 61. Since FAN7688 is located in the secondary side, it is typical to use a current transformer for sensing the primary side current. While the PROUT1 is LOW, the ICS pin is clamped at 0 V with an internal reset MOSFET. Conversely, while PROUT1 is high, the ICS pin is not clamped and the integral capacitor (C_{ICS}) is charged and discharged by the voltage difference between the sensing resistor voltage (V_{SENSE}) and the ICS pin voltage. During normal operation, the voltage of the ICS pin is below 1.2 V since the power limit threshold is 1.2 V. The current sensing resistor and current transformer turns ratio should be designed such that the voltage across the current sensing resistor (V_{SENSE}) is greater than 4V at the full load condition. Therefore the current charging and discharging C_{ICS} should be almost proportional to the voltage across the current sensing resistor (V_{SENSE}). Figure 62 compares the VICS signal and the ideal integral signal when the amplitude of V_{SENSE} is 4 V. As can be seen, there is about 10% error in the VICS signal compared to the ideal integral signal, which is acceptable for most designs. If more accuracy of the VICS is required, the amplitude of V_{SENSE} should be increased.

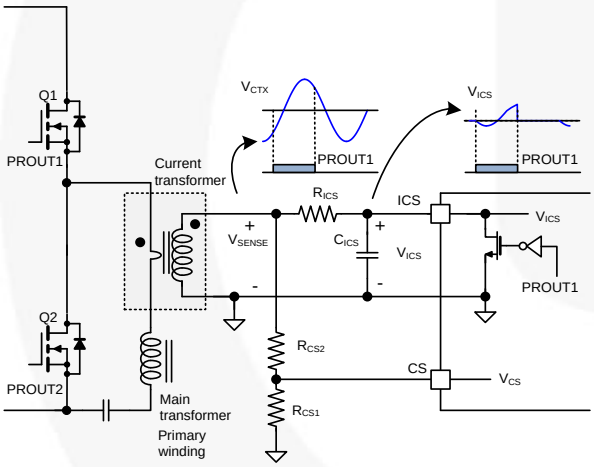


Figure 61. Current Sensing of FAN7688

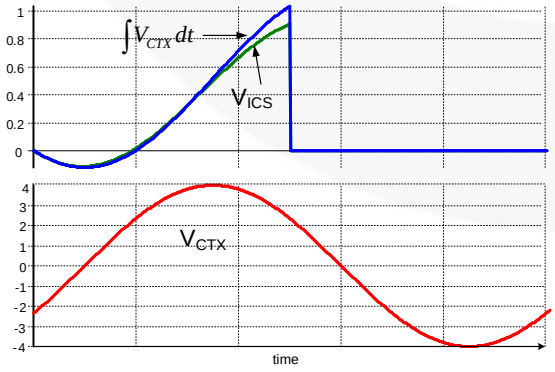


Figure 62. Generating the Integral Signal (V_{ICS}) from V_{SENSE}

Since the peak value of the integral of the current sensing voltage (VICS) is proportional to the average input current of the LLC resonant converter, it is used for four main functions, listed and shown in Figure 63.

(1) SR Gate Shrink: To guarantee stable SR operation during light load operation, the SR dead time (both of turn-on and turn-off transitions) is increased resulting in SR gate shrink when V_{ICS} peak value drops below V_{TH1} (0.2 V). The SR dead time is reduced to the programmed value when V_{ICS} peak value rises above 0.25 V.

(2) SR Disable and Enable: During very light-load condition, the SR is disabled when the V_{ICS} peak value is smaller than V_{TH3} (0.075 V). When the V_{ICS} peak value increases above V_{TH2} (0.15 V), the SR is enabled.

(3) Over-Current Limit: The V_{ICS} peak value is also used for input current limit. As can be seen in Figure 63, there exist two different current limits (fast and slow). When the V_{ICS} peak value increases above the slow current limit level (V_{OCL1}) due to a mild overload condition, the internal feedback compensation voltage is slowly reduced to limit the input power. This continues until the V_{ICS} peak value drops below V_{OCL1}. During a more severe over load condition, the V_{ICS} peak value crosses the fast current limit threshold (V_{OCL2}) and the internal feedback compensation voltage is quickly reduced to limit the input power as shown in Figure 64. This continues until the V_{ICS} peak value drops below V_{OCL2}. The current limit threshold on the V_{ICS} peak value also changes as the output voltage sensing signal (V_{FB}) decreases such that output current is limited during overload condition as shown in Figure 65. These limit thresholds change to higher values ($V_{OCL1.BR}$ and $V_{OCL2.BR}$) when the converter operates in deep below resonance operation for a longer holdup time (refer to holdup time boost function).

(4) Over-Current Protection (OCP1): When the V_{ICS} peak value is larger than V_{OCP1} (1.9 V), the over current protection is triggered. 150 ns debounce time is added for over-current protection. These OCP threshold changes to a higher value ($V_{OCP1.BR}$) when the converter operates in deep below resonance operation for a longer holdup time (refer to holdup time boost function).

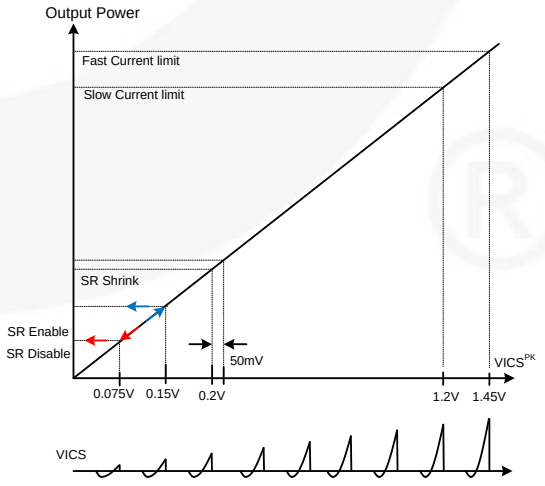


Figure 63. Functions Related to VICS Peak Voltage

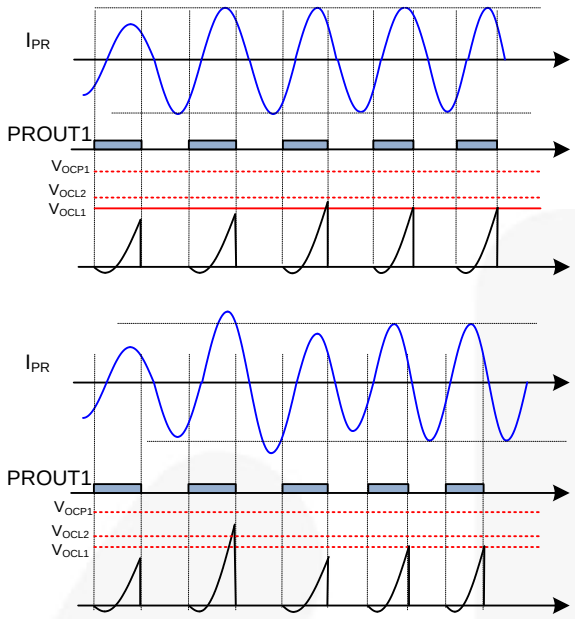


Figure 64. Current Limit of the ICS Pin by Frequency Shift (Compensation Cutback)

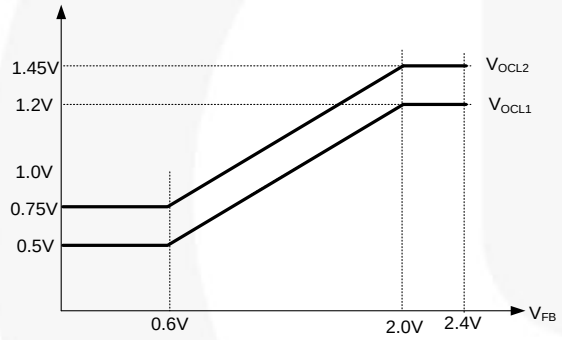


Figure 65. Current Limit Threshold Modulation as a Function of Feedback Voltage

The instantaneous switch current sensing on the CS pin is also used for the following functions.

(1) Non-ZVS Prevention: When the compensation voltage (V_{COMP}) is higher than 3 V and V_{CS} peak value is smaller than 0.3 V, non-ZVS condition is detected, which decreases the internal compensation signal to increase the switching frequency.

(2) Over-Current Protection (OCP2): When V_{CS} is higher than 3.5 V or lower than -3.5 V, over-current protection (OCP) is triggered. The instantaneous primary side current is also sensed on CS pin. Since the OCP thresholds on the CS pin are 3.5 V and -3.5 V as shown in Figure 66, the CS signal is typically obtained from V_{SENSE} by using a voltage divider as illustrated in Figure 61. 150 ns debounce time is added for OCP.

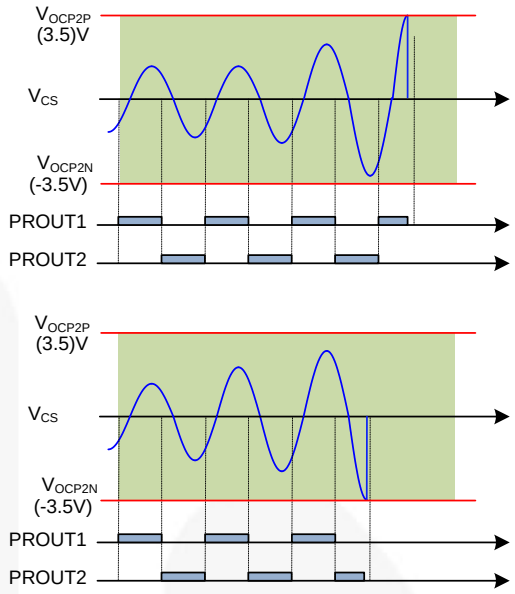


Figure 66. Over-Current Protection of the CS Pin

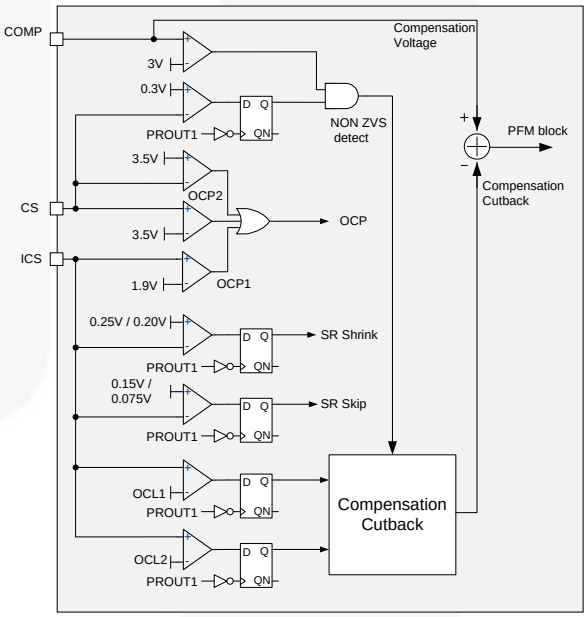


Figure 67. Utilization of Current Sensing Signal

Soft-Start and Output Voltage Regulation

Figure 68 shows the simplified circuit block for feedback control and closed loop soft-start. During normal, steady state operation, the Soft-Start (SS) pin is connected to the non-inverting input of the error amplifier which is clamped at 2.4 V. The feedback loop operates such that the sensed output voltage is same as the SS pin voltage. During startup, an internal current source ($I_{SS.T}$) charges the SS capacitor and SS pin voltage progressively increases. Therefore, the output voltage also rises monotonically as a result of closed loop SS control.

The SS capacitor is also used for the shutdown delay time during overload protection (OLP). Figure 69 shows the OLP waveform. During normal operation, the SS capacitor voltage is clamped at 2.4 V. When the output is over-loaded, V_{COMP} is saturated HIGH and the SS capacitor is decoupled from the clamping circuit through the SS control block. I_{SS} is blocked by D_{BLCK} and the SS capacitor is slowly charged up by the current source $I_{SS.UP}$. When the SS capacitor voltage reaches 3.6 V, OLP is triggered. The time required for the soft-start capacitor to be charged from 2.4 V to 3.6 V determines the shutdown delay time for overload protection.

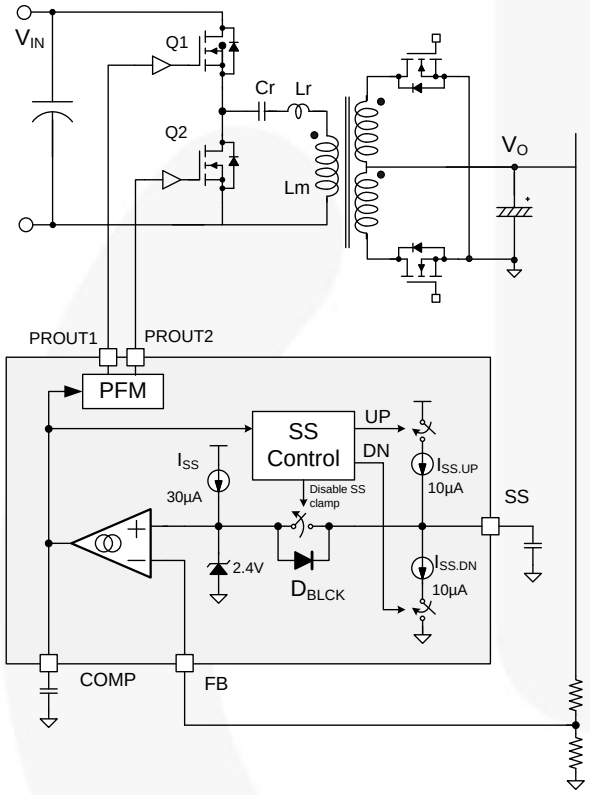


Figure 68. Schematic of Closed Loop Soft-Start

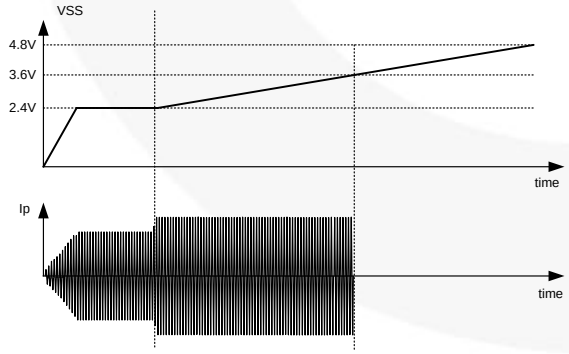


Figure 69. Delayed Shutdown with Soft-Start

Auto-Restart after Protection

All protections of FAN7688 are non-latching, auto-restart, where the delayed restart is implemented by charging and discharging the SS capacitor as illustrated in Figure 70. During normal operation, the SS capacitor voltage is clamped at 2.4 V. Once any protection is triggered, the SS clamping circuit is disabled. The SS capacitor is then charged up to 4.7 V by an internal current source ($I_{SS.UP}$). The SS capacitor is then discharged down to 0.1 V by another internal current ($I_{SS.DN}$). After charging and discharging the SS capacitor three more times, auto recovery is enabled.

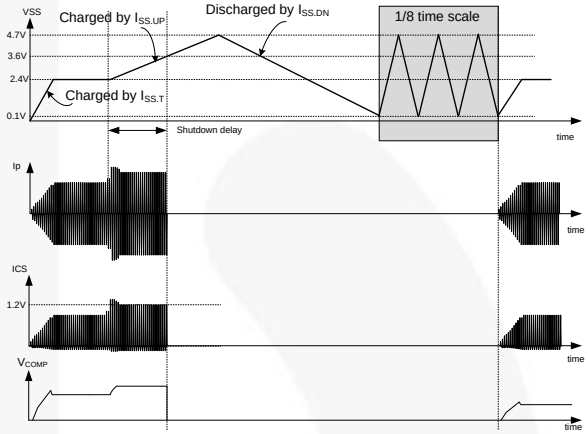


Figure 70. Auto Re-Start after Protection is Triggered

Output Short Protection

To minimize the power dissipation through the power stage during a severe fault condition, FAN7688 offers Output Short Protection (OSP). When the output is heavily over-loaded or short circuited, the feedback voltage (output voltage sensing) does not follow the reference voltage of the error amplifier (2.4 V). When the difference between the reference voltage of the error amplifier and the FB voltage is larger than 1.2 V, the OSP is triggered without waiting until the OLP is triggered as shown in Figure 71.

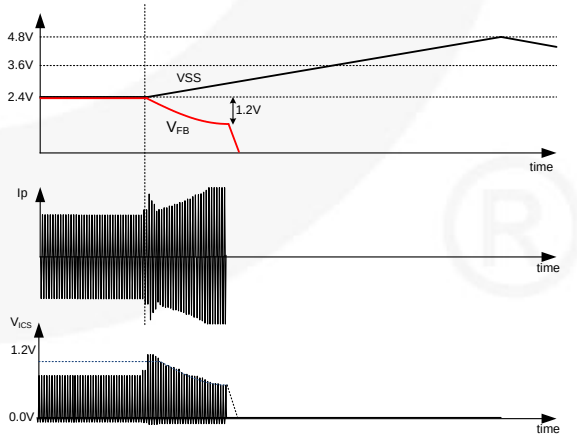


Figure 71. Output Short Protection

Dead-Time Setting

With a single pin (RDT pin), the dead times between the primary side gate drive signals (PROUT1 and PROUT2) and secondary side SR gate drive signal (SROUT1 and SROUT2) are programmed using a switched current source as shown in Figure 72 and Figure 73. Once the 5 V bias is enabled, the RDT pin voltage is pulled up. When the RDT pin voltage reaches 1.4 V, the voltage across C_{DT} is then discharged down to 1 V by an internal current source I_{DT}. I_{DT} is then disabled and the RDT pin voltage is charged up by the RDT resistor. As highlighted in Figure 73, 1/64 of the time required (T_{SET1}) for RDT pin voltage to rise from 1 V to 3 V determines the dead time between the secondary side SR gate drive signals.

The switched current source I_{DT} is then disabled and the RDT pin voltage is discharged. 1/32 of the time required (T_{SET2}) for the RDT pin voltage to drop from 3 V to 1 V determines the dead time between the primary side gate drive signals. After the RDT voltage drops to 1 V, the current source I_{DT} is disabled a second time, allowing the RDT voltage to be charged up to 5 V.

0 shows the dead times for SROUT and PROUT programmed with recommended R_{DT} and C_{DT} component values. Since the time is measured by an internal 40 MHz clock signal, the resolution of the dead time setting is 25 ns. The minimum and maximum dead times are therefore limited at 75 ns and 375 ns respectively. To assure stable SR operation while taking circuit parameter tolerance into account, 75 ns dead time is not recommended especially for the SR dead time.

When FAN7688 operates in PWM mode at light-load condition, the dead time is doubled to reduce the switching loss.

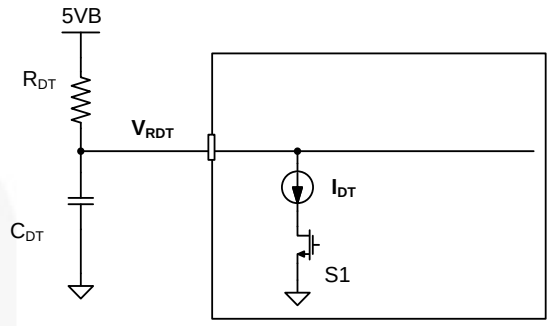


Figure 72. Internal Current Source for of RDT Pin

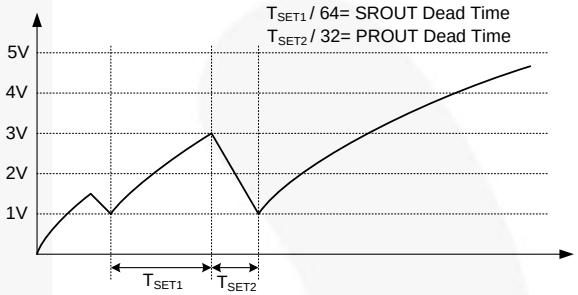


Figure 73. Multi-function Operation of RDT Pin

Table 1. Dead Time setting for PROUT and SROUT

	C_{DT}=180 pF		C_{DT}=220 pF		C_{DT}=270pF		C_{DT}=330 pF		C_{DT}=390 pF		C_{DT}=470 pF		C_{DT}=560 pF	
R_{DT}	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)
28 k	~~75~~	375	~~75~~	375	~~75~~	375	100	375	125	375	150	375	175	375
30 k	~~75~~	250	~~75~~	325	100	375	100	375	125	375	150	375	175	375
33 k	~~75~~	200	~~75~~	250	100	300	125	375	150	375	175	375	200	375
36 k	~~75~~	175	~~75~~	200	100	250	125	325	150	375	175	375	225	375
40 k	~~75~~	150	100	175	125	225	150	275	175	325	200	375	250	375
44 k	~~75~~	125	100	150	125	200	150	250	175	300	225	350	275	375
48 k	100	125	125	150	150	175	175	225	200	275	250	325	300	375
53 k	**100**	**100**	**125**	**125**	**150**	**175**	**200**	**200**	225	250	275	300	325	375
58 k	125	100	150	125	**175**	**150**	**200**	**200**	**250**	**250**	**300**	**300**	**350**	**350**
64 k	125	100	150	125	175	150	225	200	275	225	325	275	375	325
71 k	150	100	175	125	200	150	250	175	300	225	350	250	375	325
78 k	150	100	175	100	225	150	275	175	325	200	375	250	375	300
86 k	175	~~75~~	200	100	250	125	300	175	375	200	375	250	375	300
94 k	175	~~75~~	225	100	275	125	325	175	375	200	375	225	375	275
104 k	200	~~75~~	250	100	300	125	375	150	375	200	375	225	375	275
114 k	225	~~75~~	275	100	325	125	375	150	375	175	375	225	375	275
126 k	250	~~75~~	300	100	375	125	375	150	375	175	375	225	375	275
138 k	275	~~75~~	325	100	375	125	375	150	375	175	375	225	375	250
152 k	300	~~75~~	350	100	375	125	375	150	375	175	375	225	375	250

Minimum Frequency Setting

The minimum switching frequency is limited by comparing the timing capacitor voltage (V_{CT}) with an internal 3 V reference as shown in Figure 74. Since the rising slope of the timing capacitor voltage is determined by the resistor (R_{FMIN}) connected to FMIN pin, the minimum switching frequency is given as:

$$f_{SW.MIN} = 100kHz \times \frac{10k\Omega}{R_{FMIN}} \quad (1)$$

The minimum programmable switching frequency is limited by the digital counter running on an internal 40 MHz clock. Since a 10 bit counter is used, the minimum switching frequency given by the digital oscillator is 39 kHz (40 MHz/1024=39 kHz). Therefore, the maximum allowable value for RFMIN is 25.5 KΩ.

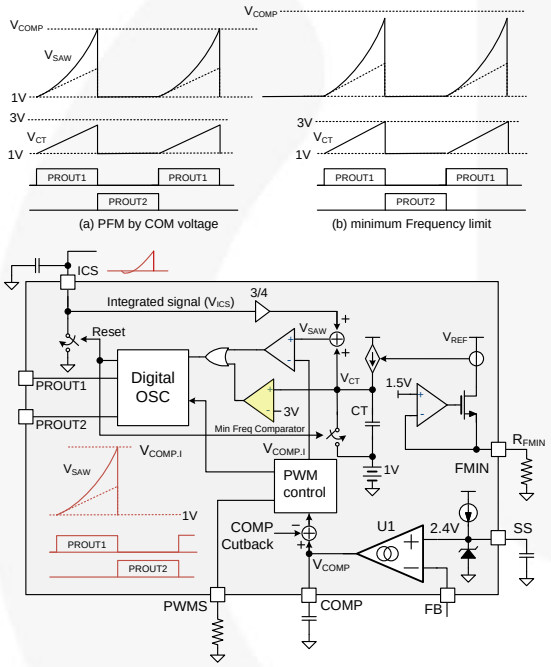


Figure 74. Minimum Switching Frequency Setting

PWM Mode Entry Level Setting

When the COMP voltage drops below $V_{COMP.PWM}$ as a result of decreasing load, the internal COMP signal is clamped at the threshold level and PFM operation switches to PWM Mode. The PWM entry level threshold is programmed between 1.5 V and 1.9 V using a resistor on the PWMS pin as shown in Figure 75. Once FAN7688 enters into PWM mode, the SR gate drives are disabled.

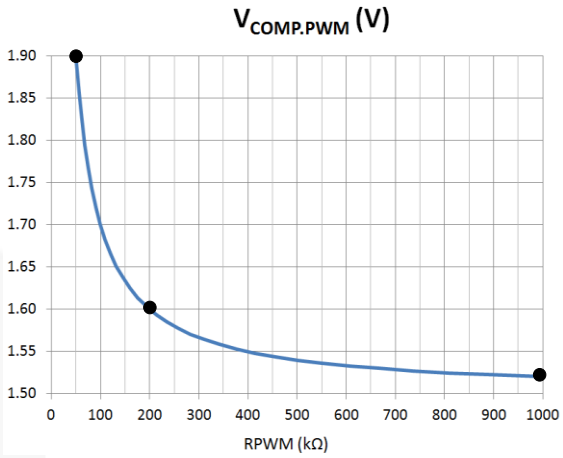


Figure 75. PWM Mode Entry Level Setting

Skip Cycle Operation

As illustrated in Figure 76, when the COMP voltage drops below $V_{COMP.SKIP}$ (1.25 V) as a result of decreasing load, skip cycle operation is employed to reduce switching losses. As the COMP voltage rises above 1.3 V, the switching operation is resumed. When the FB voltage rises above $V_{FB.OVP1}$ (2.65 V), the skip cycle operation is also enabled to limit the output voltage rising quickly. As the FB voltage drops below $V_{FB.OVP2}$ (2.3 V), the switching operation is resumed.

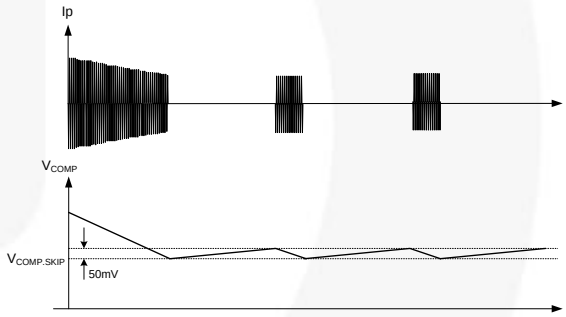


Figure 76. Skip Cycle Operation

Synchronous Rectification

FAN7688 uses a dual edge tracking adaptive gate drive method that anticipates the SR current zero crossing instant with respect to two different time references. Figure 77 and Figure 78 show the operational waveforms of the dual edge tracking adaptive SR drive method operating below and above resonance. To simplify the explanation, the SR dead time is assumed to be zero. The first tracking circuit measures SR conduction time (T_{SR_CNDCTN}) and uses this information to generate the first adaptive drive signal (V_{PRD_DRV1}) for the next switching cycle whose duration is the same as the SR conduction time of previous switching cycle. The second tracking circuit measures the turn-off extension time which is defined as time duration from the falling edge of the primary side drive to the corresponding SR turn-off instant (T_{EXT}). This information is then used to generate the second adaptive drive signal (V_{PRD_DRV2}) for the next switching cycle. When the turn-off of the primary side drive signal is after the turn-off of the corresponding SR for below resonance operation, the

second adaptive SR drive signal is the same as the corresponding primary side gate drive signal. However, when the turn-off of the primary side drive signal is before the turn-off instant of the corresponding SR for above resonance operation, the second adaptive SR drive signal is generated by extending the corresponding primary side gate drive signal by T_{EXT} of the previous switching cycle.

Since the turn off instant of the second adaptive gate drive signal is extended by T_{EXT} with respect to the falling edge of the primary side gate drive signal, the duration of this signal consequentially changes with switching frequency. By combining these two signals V_{PRD_DRV1} and V_{PRD_DRV2} with an AND gate, the optimal adaptive gate drive signal is obtained.

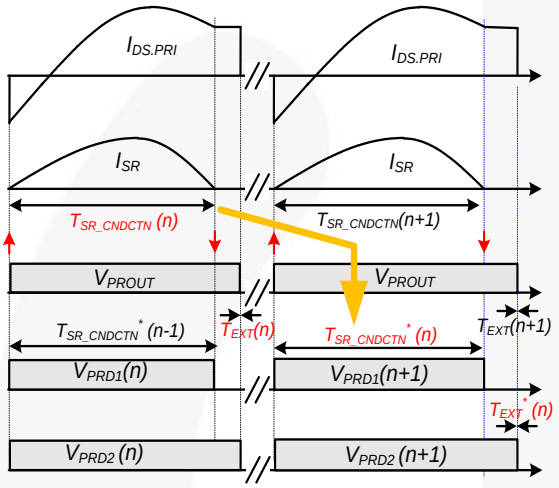


Figure 77. Operation of Dual Edge Tracking Adaptive SR Control (below Resonance)

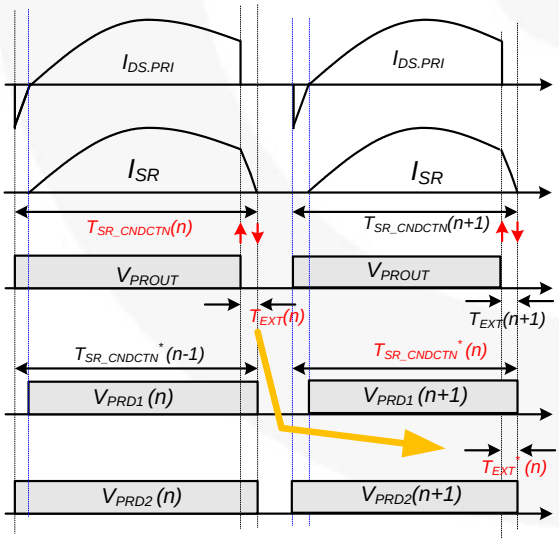


Figure 78. Operation of Dual Edge Tracking Adaptive SR Control (above Resonance)

The SR conduction times for SR1 and SR2 for each switching cycle are measured using a single pin (SR1DS pin). The SR1DS voltage and its delayed signal, resulting from a 100 ns RC time constant, are compared as shown in Figure 79. When the SR is conducting, the SR1DS voltage is clamped to either ground or the high voltage rail (2 times the output voltage) as illustrated in Figure 80. Whereas, SR1DS voltage changes fast when there is a switching transition. When both of the SR MOSFETs are turned off, the SR1DS voltage oscillates. When the SR1DS voltage changes faster than 0.25 V/100 ns on the rising edge and 0.2 V/100 ns on the falling edge the switching transition of the SR conduction state is detected. Based on the detected switching transition, FAN7688 predicts the SR current zero-crossing instant for the next switching cycle. The 100 ns detection delay caused by the RC time constant is compensated in the internal timing detection circuit for a correct gate drive for SR.

Figure 80 and Figure 81 show the typical waveforms of SR1DS pin voltage together with other key waveforms. Since the voltage rating of SR1DS pin is 4 V, the voltage divider should be properly designed such that no over-voltage is applied to this pin. Additional bypass capacitor (C_{DS}) can be connected to SR1DS pin to improve noise immunity. However, the equivalent time constant generated from the bypass capacitor and voltage divider resistors should be smaller than the internal RC time constant (100 ns) of the detection circuit for proper SR current zero crossing detection.

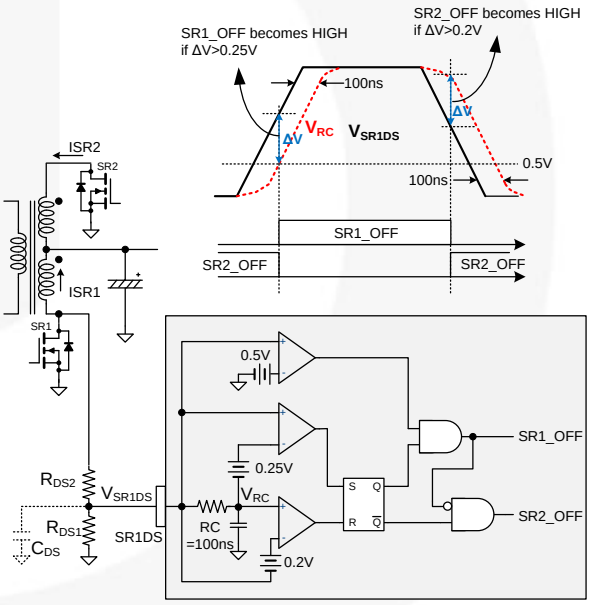


Figure 79. SR Conduction Detection with Single Pin (SR1DS Pin)

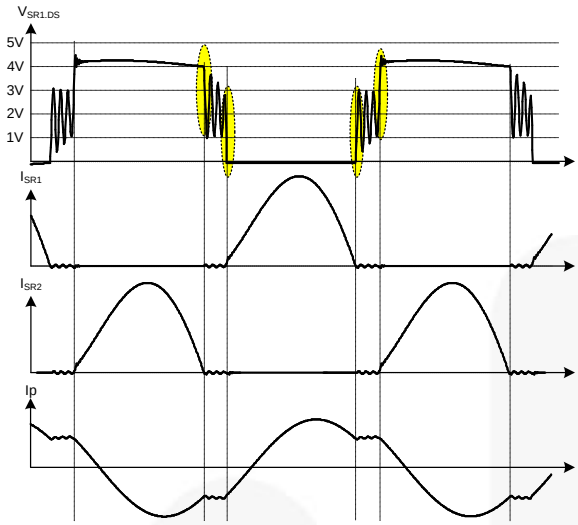


Figure 80. SR Conduction Detection Waveform at below Resonance Operation

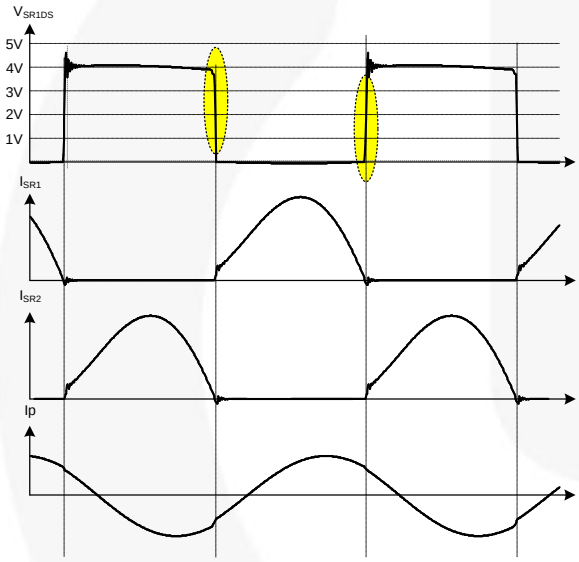


Figure 81. SR Conduction Detection Waveform at above Resonance Operation

Holdup Time Boost Function

The holdup time of an off-line supply is defined as the time required for the output voltage to remain within regulation after the AC input voltage is removed. Since the input bulk capacitor voltage drops during the holdup time, more current is taken from the bulk capacitor to deliver the same power to the load. With a fixed power limit level of power supply designed for nominal input voltage, the holdup time tends to be limited due to the increased input current of the power supply.

FAN7688 has a holdup time boost function which increases the current limit threshold on the ICS pin voltage when the LLC resonant converter operates in deep below resonance operation during the holdup time. This holdup time boost operation is enabled when the SR conduction time is smaller than 94% of the half switching cycle for longer than 1.6 ms. The current limit level on ICS pin is recovered to normal value when the SR conduction time is larger than 98% of the half switching cycle for longer than 3.2 ms.

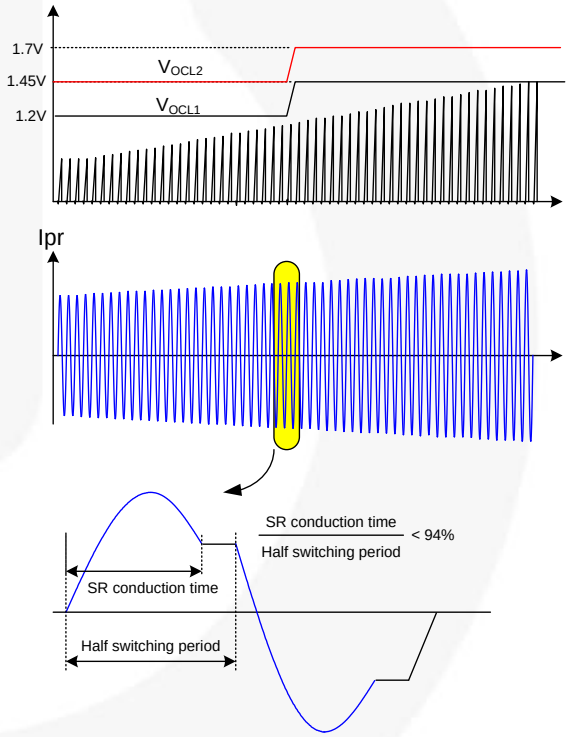


Figure 82. Holdup Time Boost Function Operation

Quick Setup Guideline for Current Sensing and Soft-Start

Assuming the switching frequency is the same as the resonance frequency, the peak v of the secondary side voltage of current transformer (V_{SENSE}) is given as:

$$V_{SENSE}^{PK} = I_O \cdot \frac{\pi}{2} \cdot \frac{N_S}{N_P} \cdot \frac{1}{n_{CT}} \times (R_{CS1} + R_{CS2})$$

[example] I_O=20 A, N_P=35, N_S=2, n_{CT}=50, R_{CS1}+R_{CS2}=100 Ω → V_{SENSE}^{PK}=3.59 V in nominal load condition.

The voltage divider on the CS pin should be selected such that OCP is not triggered during normal operation.

$$V_{CS}^{PK} = I_O \cdot \frac{\pi}{2} \cdot \frac{N_S}{N_P} \cdot \frac{1}{n_{CT}} \times \frac{R_{CS1}}{R_{CS1} + R_{CS2}} < 3.5V$$

[example] I_O=21 A, N_P=35, N_S=2, n_{CT}=50, R_{CS1}=30 Ω, R_{CS2}=70 Ω → V_{CS}^{PK}=1.07 V in nominal load condition.

The resistor and capacitor on the ICS pin should be selected such that the current limit is not triggered during normal operation.

$$V_{ICS}^{PK} = I_O \cdot \frac{N_S}{N_P} \cdot \frac{1}{n_{CT}} \times \frac{R_{CS1} + R_{CS2}}{R_{ICS}} \frac{1}{C_{ICS}} \cdot \frac{1}{2 f_{SW}} < 1.2V$$

[example] Io=20 A, N_P=35, N_S=2, n_{CT}=50, R_{CS1}=30 Ω, R_{CS2}=70 Ω, R_{ICS}=10 kΩ, C_{ICS}=1 nF, f_S=100 kHz.

→ V_{ICS}^{PK}=1.14 V in nominal load condition (actual V_{ICS}^{PK} is lower by about 10% as shown in Figure 62 due to a quasi integral effect).

Assuming the actual V_{ICS}^{PK} (V_{ICS}^{PKA}) is 1 V, the soft-start capacitor should be selected such that the overload protection is not triggered during startup with full load condition.

$$T_{SS} = \frac{C_{SS} \times 2.4V}{I_{SS}} > \frac{C_{OUT} \cdot V_O}{\frac{1.2 - V_{ICS}^{PKA}}{V_{ICS}^{PKA}} I_O}$$

[example] I_O=20 A, C_{SS}=680 nF, I_{SS}=40 μA, C_{OUT}=7,200 μF, V_{ICS}^{PKA}=1 V, V_O=12.5 V.

$$T_{SS} = \frac{C_{SS} \times 2.4V}{I_{SS}} = 40.8ms > \frac{C_{OUT} \cdot V_O}{\frac{1.2 - V_{ICS}^{PK}}{V_{ICS}^{PK}} I_O} = 22.5ms$$

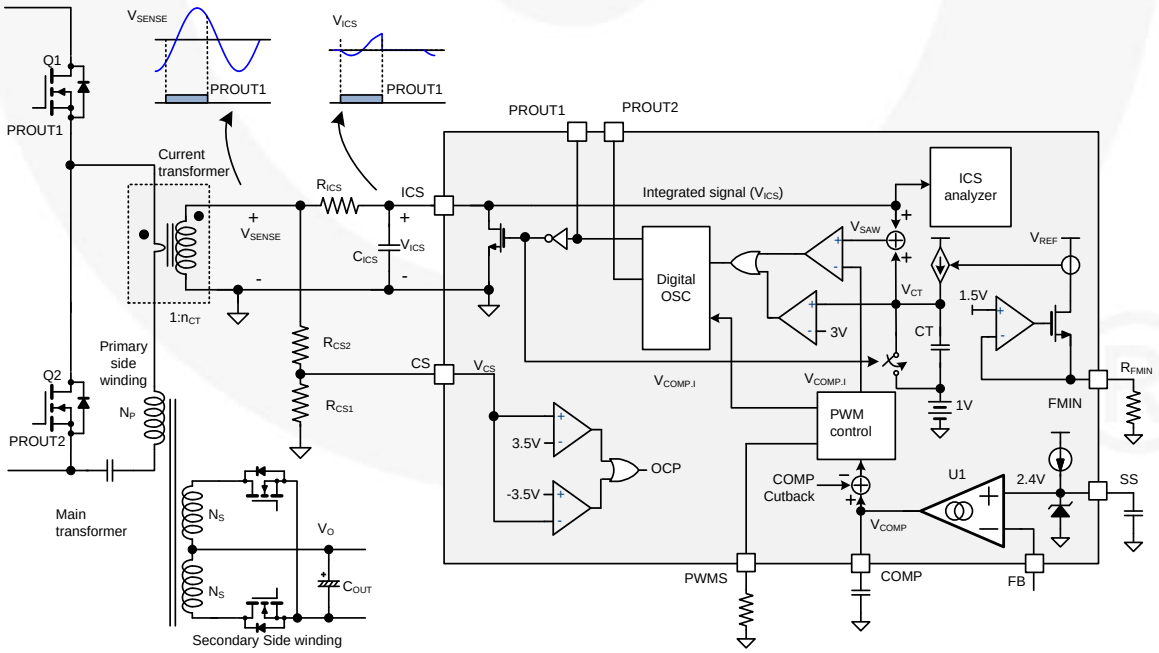


Figure 84. Basic Application Circuit for Current Sensing and Soft-Start

Typical Application Circuit (LLC Resonant Converter)

Application	Fairchild Device	Input Voltage Range	Output
PC Power	FAN7688	350~400 V_{DC}	12 V/21 A (252 W)

Features

- 4% Efficiency Improvement over Schottky Diode Rectification.
- 96.7% Peak Efficiency at 50% Load.
- 96.0% Peak Efficiency at 100% Load.
- 95% Efficiency at 20% Load.
- 89.7% Efficiency at 10% Load.
- Light-Load Efficiency (<15% Load) can be Improved by Adding a Low V_F Schottky Rectifier Parallel with each SR.

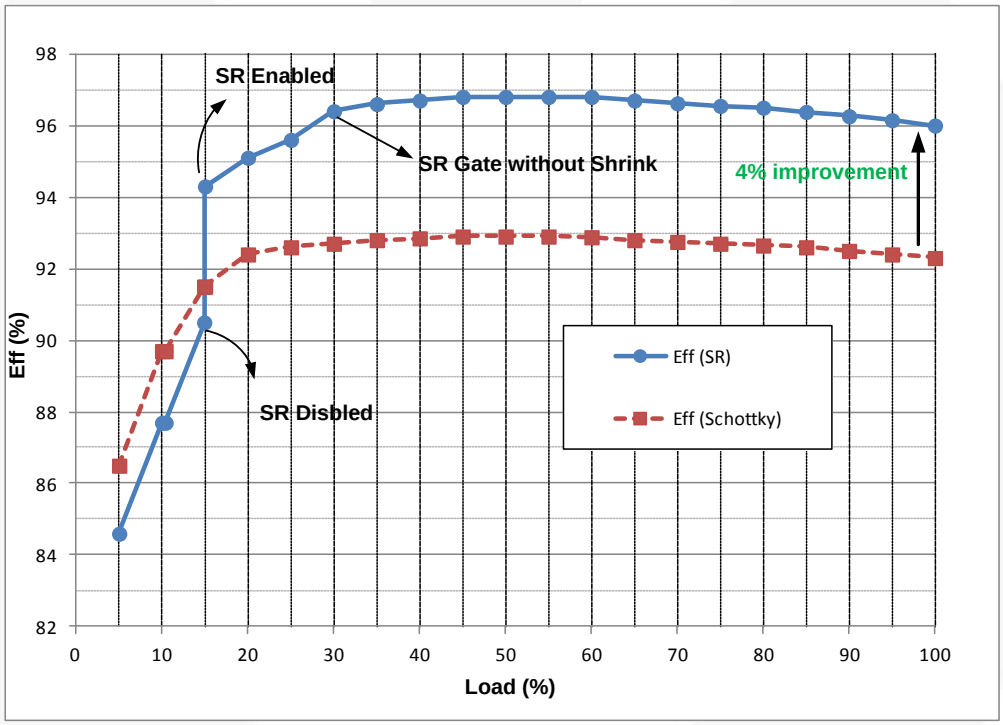


Figure 85. Evaluation Board (EVB) Measured Efficiency

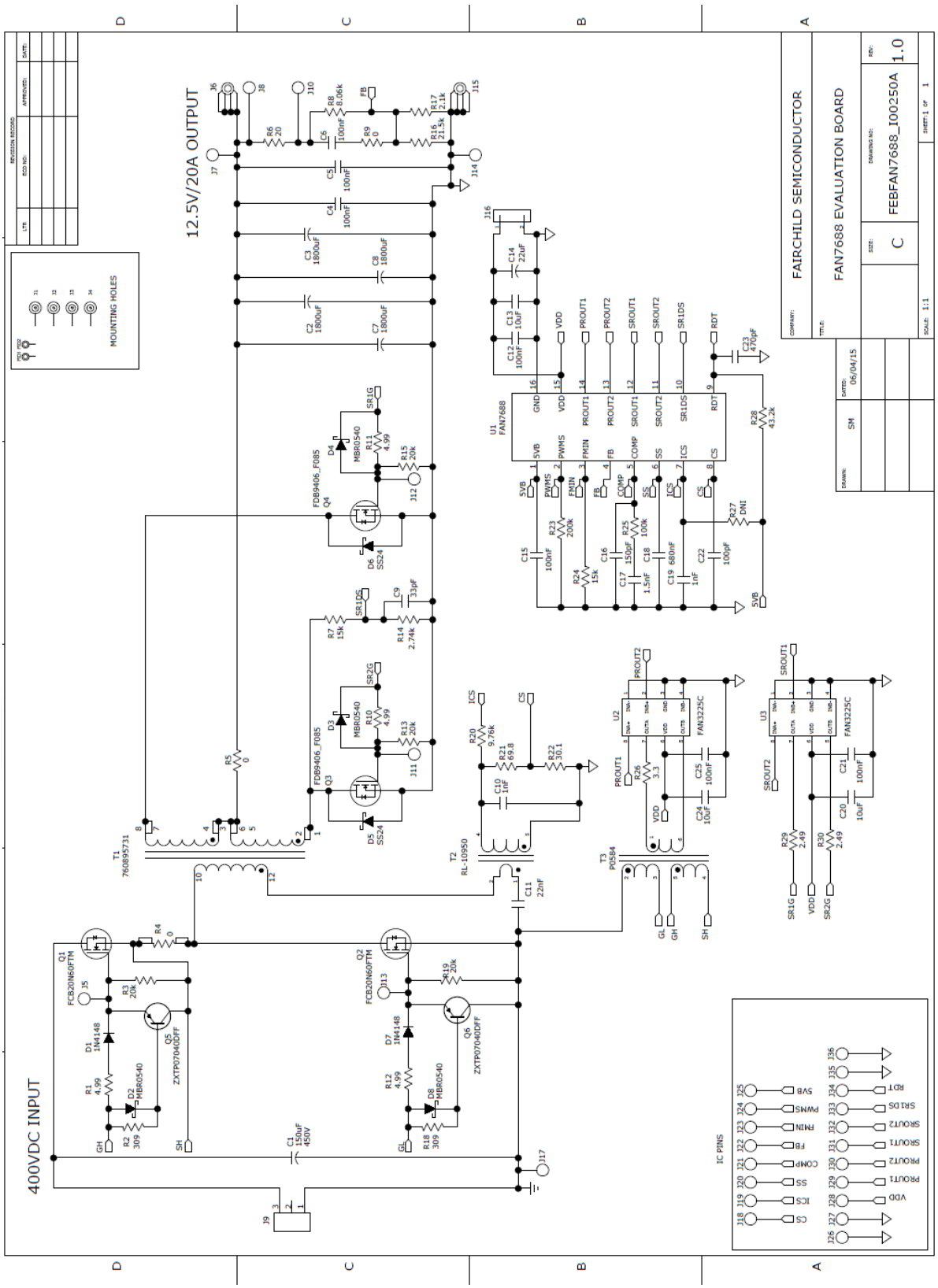
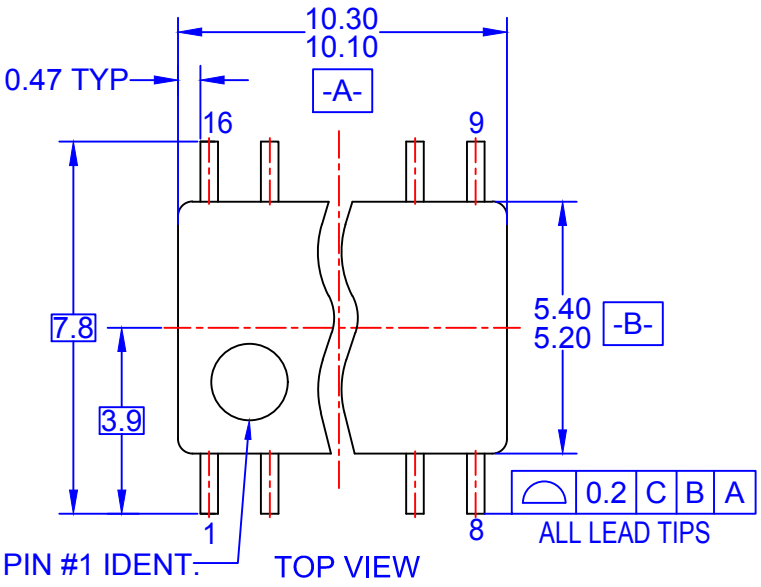
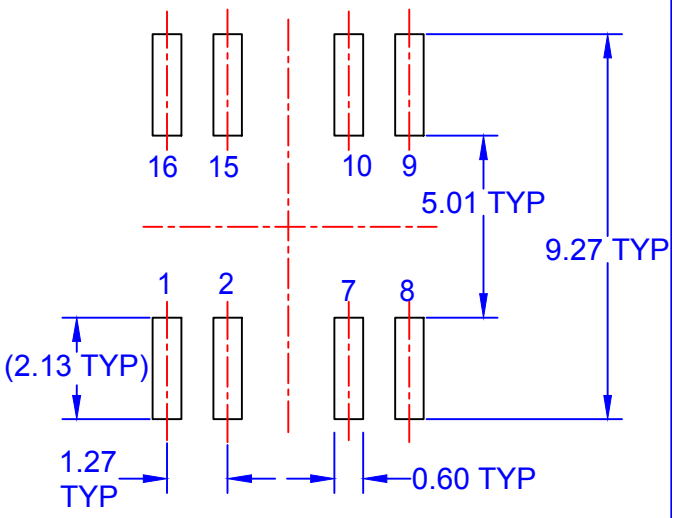
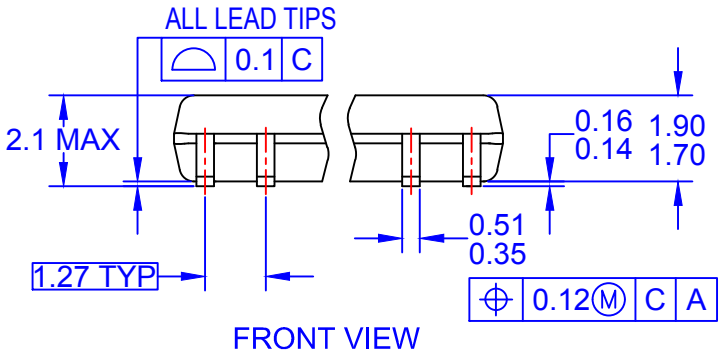


Figure 86. Schematic of Typical Application Circuit

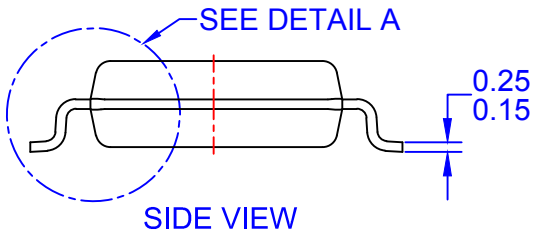




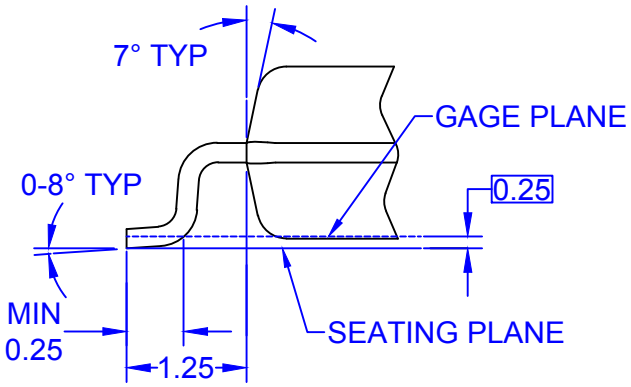
LAND PATTERN RECOMMENDATION



FRONT VIEW



SIDE VIEW



DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
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