LM11C, CL

Precision Operational Amplifiers

The LM11C is a precision, low drift operational amplifier providing the best features of existing FET and Bipolar op amps. Implementation of super gain transistors allows reduction of input bias currents by an order of magnitude over earlier devices such as the LM308A. Offset voltage and drift have also been reduced. Although bandwidth and slew rate are not as great as FET devices, input offset voltage, drift and bias current are inherently lower, particularly over temperature. Power consumption is also much lower, eliminating warm–up stabilization time in critical applications.

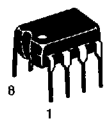
Offset balancing is provided, with the range determined by an external low resistance potentiometer. Compensation is provided internally, but external compensation can be added for improved stability when driving capacitive loads.

The precision characteristics of the LM11C make this device ideal for applications such as charge integrators, analog memories, electrometers, active filters, light meters and logarithmic amplifiers.

- Low Input Offset Voltage: 100 µV
- Low Input Bias Current: 17 pA
- Low Input Offset Current: 0.5 pA
- Low Input Offset Voltage Drift: 1.0 µV/°C
- Long–Term Stability: 10 µV/year
- High Common Mode Rejection: 130 dB

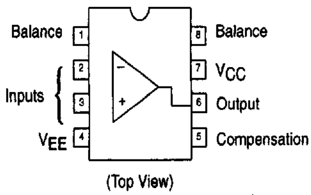
PRECISION OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

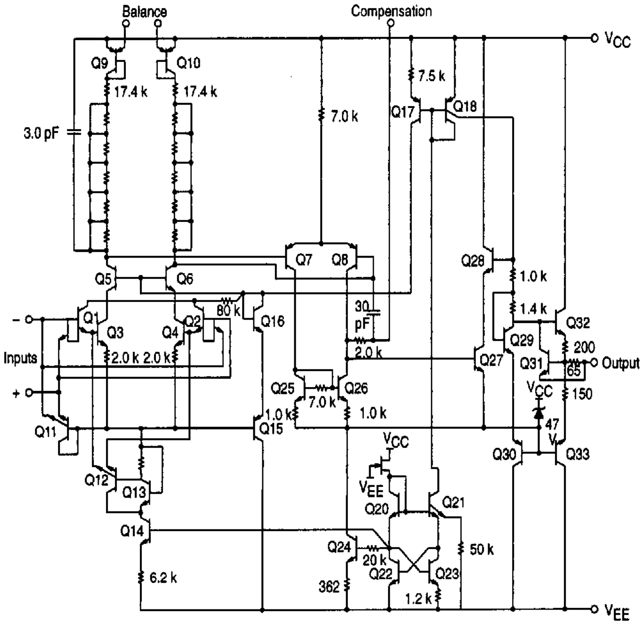


N SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS



Representative Schematic Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM11CN,CLN	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} to V_{EE}	40	Vdc
Differential Input Current (Note 1)	I_{ID}	±10	mA
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	
Power Dissipation (Note 3)	P_D	500	mW
Operating Junction Temperature	T_J	85	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted [Note 4] .)

Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	0.2	0.6	–	0.5	5.0	mV
T_{low} to T_{high}		–	–	0.8	–	–	6.0	
Input Offset Current	I_{IO}	–	1.0	10	–	4.0	25	pA
T_{low} to T_{high}		–	–	20	–	–	50	
Input Bias Current	I_{IB}	–	17	100	–	17	200	pA
T_{low} to T_{high}		–	–	150	–	–	300	
Input Resistance	r_i	–	10^{11}	–	–	10^{11}	–	Ω
Input Offset Voltage Drift T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	–	2.0	5.0	–	3.0	–	µV/°C
Input Offset Current Drift T_{low} to T_{high}	$\Delta I_{IO}/\Delta T$	–	10	–	–	50	–	fA/°C
Input Bias Current Drift T_{low} to T_{high}	$\Delta I_{IB}/\Delta T$	–	0.8	3.0	–	1.4	–	pA/°C
Large Signal Voltage Gain	A_{VOL}							V/mV
V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±2.0 mA		100	300	–	25	300	–	
T_{low} to T_{high} (Note 5)		50	–	–	15	–	–	
V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±0.5 mA		250	1200	–	50	800	–	
T_{low} to T_{high}		100	–	–	30	–	–	
Common Mode Rejection	CMR							dB
V_S = ±15 V, –13 V ≤ V_{CM} ≤ 14 V		110	130	–	96	110	–	
V_S = ±15 V, –12.5 V ≤ V_{CM} ≤ 14 V, T_{low} to T_{high}		100	–	–	90	–	–	
Power Supply Rejection	PSR							dB
±2.5 V ≤ V_S ≤ ±20 V		100	118	–	84	100	–	
T_{low} to T_{high}		96	–	–	80	–	–	
Power Supply Current	I_D	–	0.3	0.8	–	0.3	0.8	mA
T_{low} to T_{high}		–	–	1.0	–	–	1.0	
Output Short Circuit Current T_J = 150°C, Output Shorted to Ground	I_{SC}	–	±10	–	–	±10	–	mA

NOTES:
1. The inputs are shunted by back–to–back diodes for over–voltage protection. Excessive current will flow if the input differential voltage is in excess of 1.0 V if no limiting resistance is used. Additionally, a 2.0 kΩ resistance in each input is suggested to prevent possible latch–up initiated by supply reversals.
2. The output is current limited when shorted to ground or any voltages less than the supplies. Continuous overloads will require package dissipation to be considered and heatsinking should be provided when necessary.
3. Devices must be derated based on package thermal resistance (see package outline dimensions).
4. These specifications apply for V_{EE} +2.0 V ≤ V_{CM} ≤ V_{CC} –1.0 V (V_{EE} +2.5 V ≤ V_{CM} ≤ V_{CC} –1.0 V for T_{low} to T_{high}) and ±2.5 V ≤ V_S ≤ ±20 V T_{low} to T_{high}: 0°C ≤ T_J ≤ +70°C for LM11C and LM11C.
5. V_{out} = ±11.5 V, all other conditions unchanged.

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Figure 1. Input Bias Current versus Case Temperature

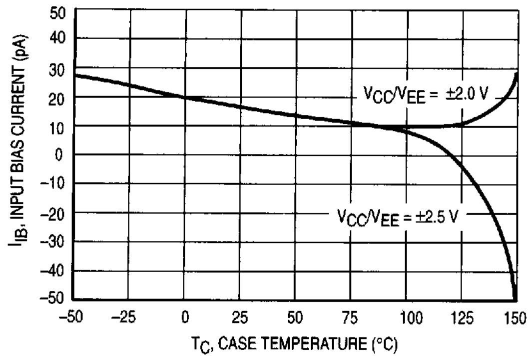


Figure 2. Input Offset Current versus Case Temperature

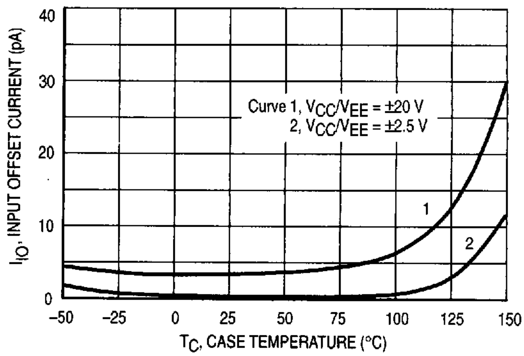


Figure 3. Temperature Coefficient of Input Offset Voltage versus Input Offset Voltage

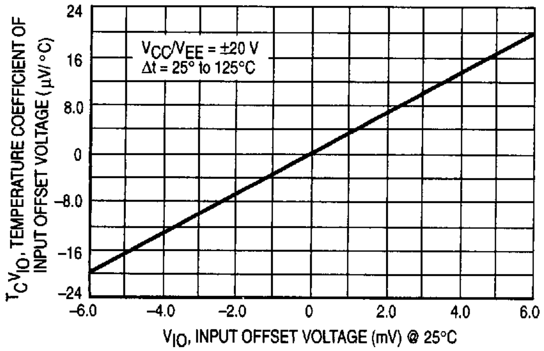


Figure 4. Spectral Noise Density

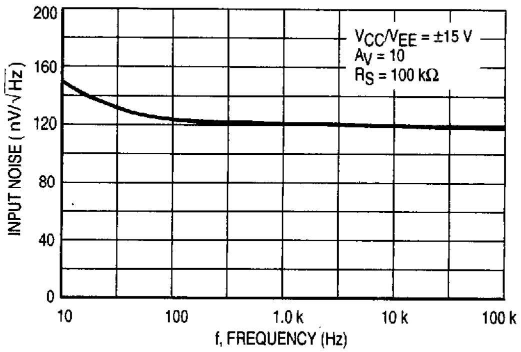


Figure 5. Common Mode Limits versus Temperature

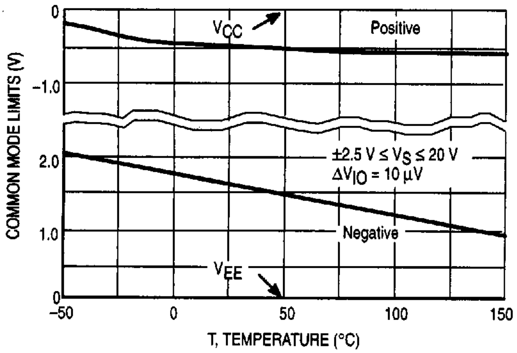


Figure 6. Common Mode Rejection and Slew Limit versus Frequency

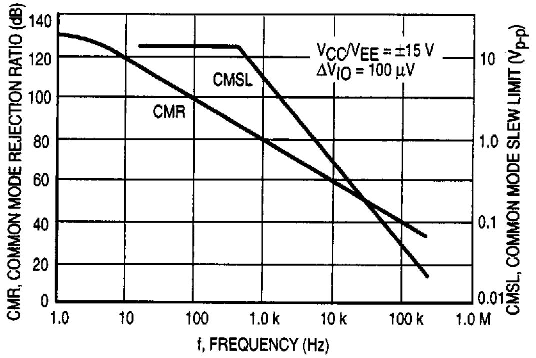


Figure 7. Open Loop Voltage Gain versus Supply Voltage

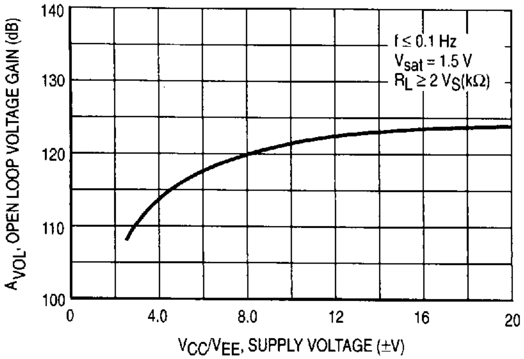


Figure 8. Output Saturation versus Load Current

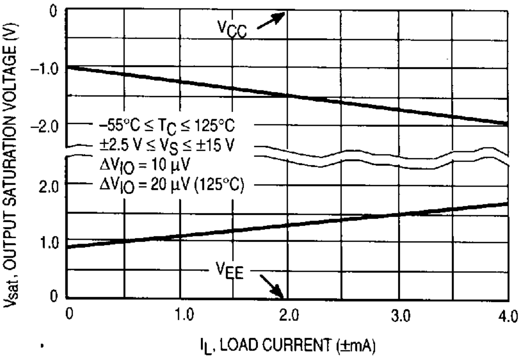


Figure 9. Power Supply Rejection Ratio versus Frequency

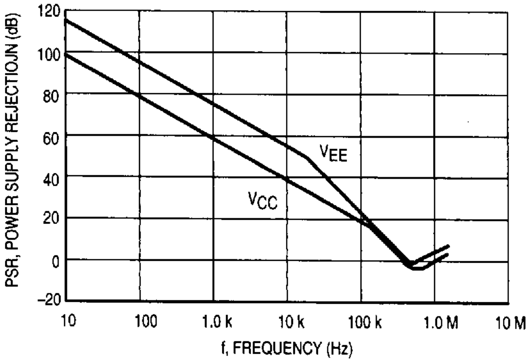


Figure 10. Supply Current versus Supply Voltage

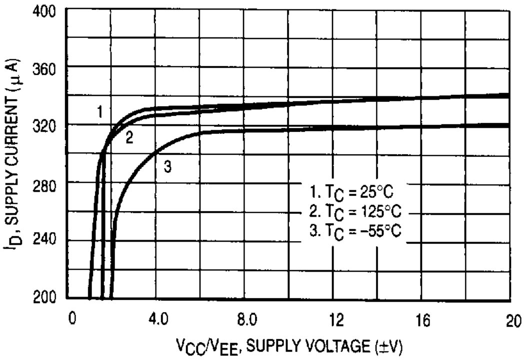


Figure 11. Open Loop Voltage Gain and Phase versus Frequency

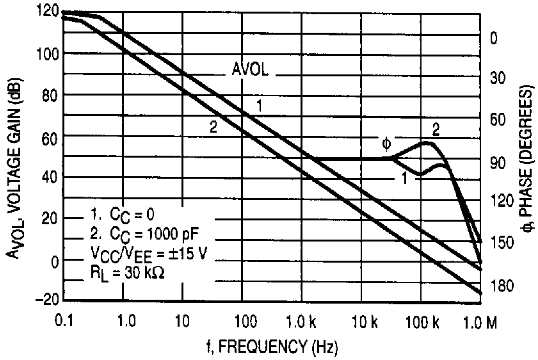


Figure 12. Slew Rate versus External Compensation Capacitor

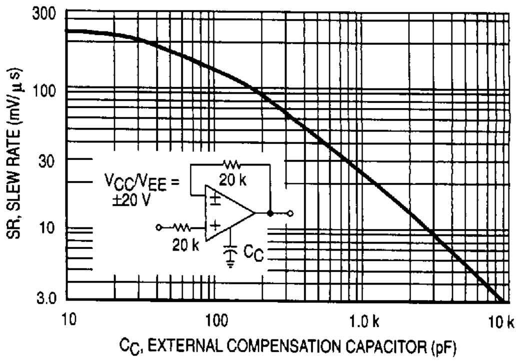
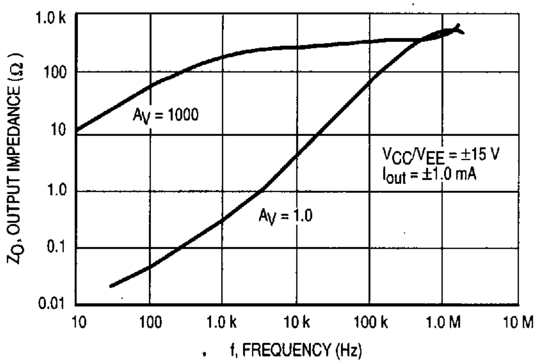


Figure 13. Closed Loop Output Impedance versus Frequency



APPLICATIONS INFORMATION

Due to the extremely low input bias currents of this device, it may be tempting to remove the bias current compensation resistor normally associated with a summing amplifier configuration. Direct connection of the inputs to a low impedance source or ground should be avoided when supply voltages greater than approximately 3.0 V are used. The potential problem involves reversal of one supply which can cause excessive current to flow in the second supply. Possible destruction of the IC could result if the second supply is not current limited to approximately 100 mA or if bypass capacitors greater than 1.0 μF are used in the supply bus.

Disconnecting one supply will generally cause reversal due to loading of the other supply within the IC and in external circuitry. Although the problem can usually be avoided by placing clamp diodes across the power supplies of each printed circuit board, a careful design will include sufficient resistance in the input leads to limit the current to 10 mA if the input leads are pulled to either supply by internal currents. This precaution is not limited only to the LM11C.

The LM11C is capable of resolving picoampere level signals. Leakage currents external to the IC can severely impair the performance of the device. It is important that high quality insulating materials such as teflon be employed. Proper cleaning to remove fluxes and other residues from printed circuit boards, sockets and the device package are necessary to minimize surface leakage.

When operating in high humidity environments or temperatures near 0°C, a surface coating is suggested to set up a moisture barrier.

Leakage effects on printed circuit boards can be reduced by encircling the inputs (both sides of pc board) with a conductive guard ring connected to a low impedance potential nearly the same as that of the inputs.

Guard ring electrical connections for common operational amplifier configurations are illustrated in Figure 14. Electrostatic shielding is suggested in high impedance circuits.

Error voltages in external circuitry can be generated by thermocouple effects. Dissimilar metals along with temperature gradients can set up an error voltage ranging in the hundreds of microvolts. Some of the best thermocouples are junctions of dissimilar metals made up of IC package pins and printed circuit boards. Problems can be avoided by keeping low level circuitry away from heat generating elements.

The LM11C is internally compensated, but external compensation can be added to improve stability, particularly when driving capacitive loads.

Figure 14. Guard Ring Electrical Connections for Common Amplifier Configurations

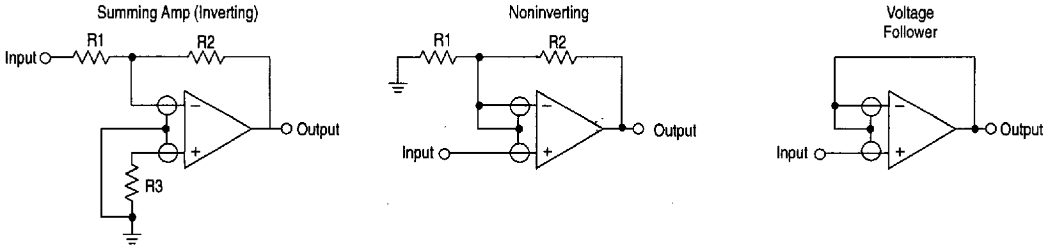


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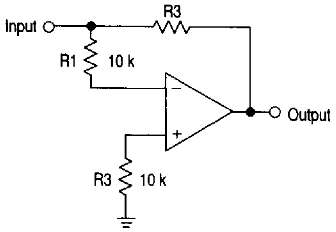
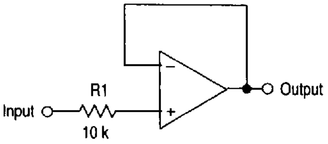
Figure 15. Input Protection for Summing (Inverting) Amplifier



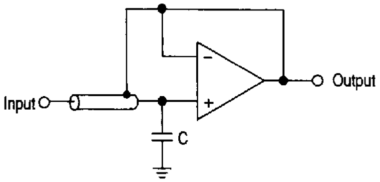
Current is limited by R1 in the event the input is connected to a low impedance source outside the common mode range of the device. Current is controlled by R2 if one supply reverses. R1 and R2 do not affect normal operation.

Figure 16. Input Protection for a Voltage Follower

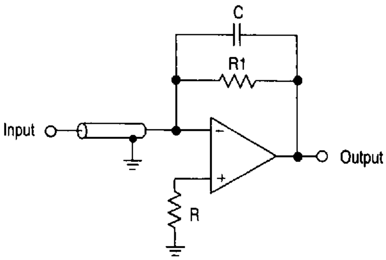


Input current is limited by R1 when the input exceeds supply voltage, power supply is turned off, or output is shorted.

Figure 17. Cable Bootstrapping and Input Shields

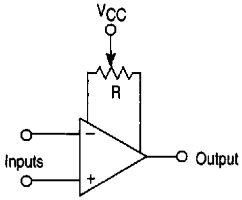


An input shield bootstrapped in a voltage follower reduces input capacitance, leakage, and spurious voltages from cable flexing. A small capacitor from the input to ground will prevent any instability.



In a summing amplifier the input is at virtual ground. Therefore the shield can be grounded. A small feedback capacitor will insure stability.

Figure 18. Adjusting Input Offset Voltage with Balance Potentiometer



Minimum Adjustment Range (mV)	R (Ω)
±0.4	1.0 k
±1.0	3.0 k
±2.0	10 k
±5.0	100 k

Input offset voltage adjustment range is a function of the Balance Potentiometer Resistance as indicated by the table above. The potentiometer is connected between the two "Balance" pins.