150-mA, ULTRA-LOW QUIESCENT CURRENT, 1-µA I_Q LOW-DROPOUT LINEAR REGULATOR

Check for Samples: TPS78225-Q1 TPS78227-Q1 TPS78228-Q1 TPS78230-Q1

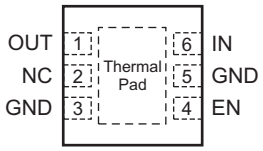
FEATURES

- **Qualified for Automotive Applications**
- **Low I_Q: 1 µA**
- **150-mA Low-Dropout Regulator**
- **Low Dropout at 25°C: 130 mV at 150 mA**
- **Low Dropout at 85°C: 175 mV at 150 mA**
- **4% Accuracy Over Load/Line/Temperature**
- **Available in Fixed Voltage Options (2.5 V, 2.7 V, 2.8 V, and 3 V) Using Innovative Factory EEPROM Programming**
- **Stable with a 1-µF Ceramic Capacitor**
- **Thermal Shutdown and Overcurrent Protection**
- **CMOS Logic Level Compatible Enable Pin**
- **Available in DDC (TSOT23-5) or DRV (2-mm x 2-mm SON-6) Packages**

APPLICATIONS

- **TI MSP430 Attach Applications**
- **Power Rails with Programming Mode**

DRV PACKAGE
2mm x 2mm SON-6
(TOP VIEW)



NC – No connection

DESCRIPTION

The TPS782xx family of low-dropout regulators (LDOs) offers the benefits of ultra-low power (I_Q = 1 µA), and miniaturized packaging (2-mm×2-mm SON).

This LDO is designed specifically for battery-powered applications where ultra-low quiescent current is a critical parameter. The TPS782, with ultra-low I_Q (1 µA), is ideal for microprocessors, memory cards, and smoke detectors.

The ultra-low power and miniaturized packaging allow designers to customize power consumption for specific applications. Consult with your local factory representative for exact voltage options and ordering information; minimum order quantities may apply.

The TPS782xx family is designed to be compatible with the TI MSP430 and other similar products. The enable pin (EN) is compatible with standard CMOS logic. This LDO is stable with any output capacitor greater than 1.0 µF. Therefore, this device requires minimal board space because of miniaturized packaging and a potentially small output capacitor. The TPS782xx series also features thermal shutdown and current limit to protect the device during fault conditions. The devices have an operating temperature range of T_J = –40°C to 125°C. For high-performance applications that require a dual-level voltage option, consider the TPS780 series, with an I_Q of 500 nA and dynamic voltage scaling.

ORDERING INFORMATION(1)

T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SON – DRV	Reel of 3000	TPS78225QDRVRQ1	NSY
			TPS78227QDRVRQ1	OFH
			TPS78228QDRVRQ1	OFI
			TPS78230QDRVRQ1	OFJ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to 125°C, unless otherwise noted. All voltages are with respect to GND.

		TPS782xx	UNIT
Input voltage range, V_{IN}		–0.3 to +6.0	V
Enable		–0.3 to V_{IN} + 0.3V	V
Output voltage range, V_{OUT}		–0.3 to V_{IN} + 0.3V	V
Maximum output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See the Dissipation Ratings table	
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V
Operating junction temperature range, T_J		–40 to 125	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
High-K(1)	DRV	20°C/W	65°C/W	15.4 mW/°C	1540 mW	84 5mW	615 mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

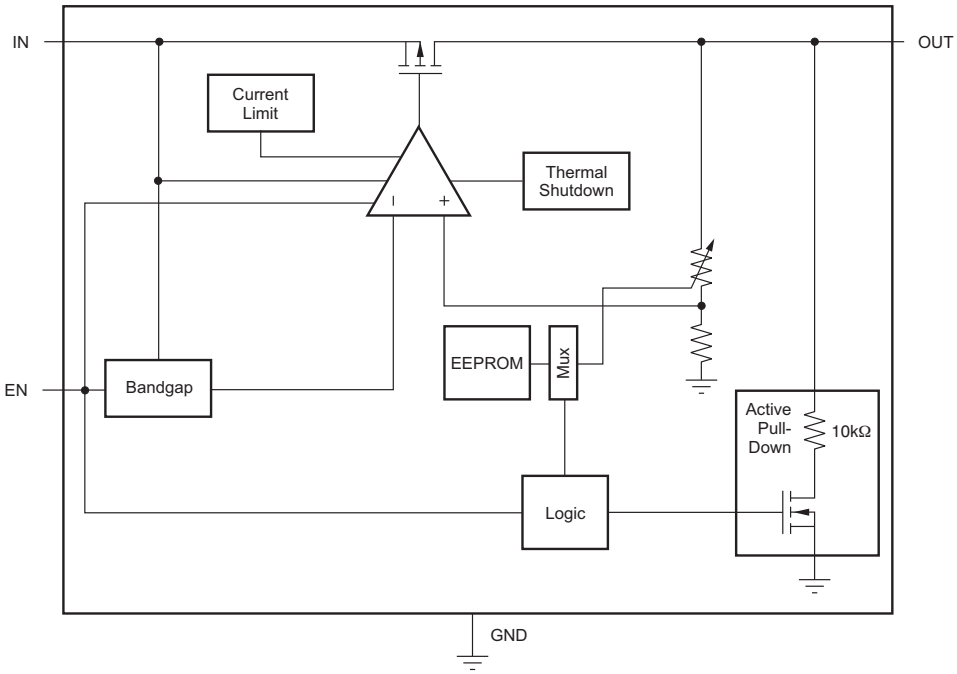
ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, fixed V_{OUT} test conditions (unless otherwise noted). Typical values at T_J = 25°C.

PARAMETER			TEST CONDITIONS		TPS782xx MIN	TPS782xx TYP	TPS782xx MAX	UNIT
V_{IN}	Input voltage range				2.2		5.5	V
V_{OUT}	DC output accuracy	Nominal	T_J = 25°C		–2	±1	+2	%
		Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V, 5 mA ≤ I_{OUT} ≤ 150 mA		–4	±2	+4	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation		$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 5 mA			±1		%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		0 mA ≤ I_{OUT} ≤ 150 mA			±2		%
V_{DO}	Dropout voltage(1)		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 150 mA			130	250	mV
V_N	Output noise voltage		BW = 100 Hz to 100 kHz, V_{IN} = 2.2 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA			86		μV_{RMS}
I_{CL}	Output current limit		V_{OUT} = 0.90 × $V_{OUT(NOM)}$		150	230	400	mA
I_{GND}	Ground pin current		I_{OUT} = 0 mA			1	1.4	µA
			I_{OUT} = 150 mA			8		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4 V, 2.2 V ≤ V_{IN} < 5.5 V, T_J = 25°C			18	130	nA
I_{EN}	EN pin current		V_{EN} = 5.5 V, T_J = 25°C				40	nA
PSRR	Power-supply rejection ratio		V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 150 mA	f = 10 Hz		40		dB
				f = 100 Hz		20		dB
				f = 1 kHz		15		dB
t_{STR}	Startup time(2)		C_{OUT} = 1.0 µF, V_{OUT} = 10% $V_{OUT(NOM)}$ to V_{OUT} = 90% $V_{OUT(NOM)}$			500		µs
t_{SHDN}	Shutdown time(3)		I_{OUT} = 150 mA, C_{OUT} = 1.0 µF, V_{OUT} = 2.8 V, V_{OUT} = 90% $V_{OUT(NOM)}$ to V_{OUT} = 10% $V_{OUT(NOM)}$			500(4)		µs
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing			160		°C
			Reset, temperature decreasing			140		°C
T_J	Operating junction temperature				–40		125	°C

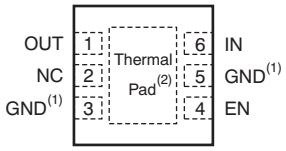
(1) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ ≤ 2.3 V, because minimum V_{IN} = 2.2 V.
(2) Time from V_{EN} = 1.2 V to V_{OUT} = 90% ($V_{OUT(NOM)}$).
(3) Time from V_{EN} = 0.4 V to V_{OUT} = 10% ($V_{OUT(NOM)}$).
(4) See *Shutdown* in the *Application Information* section for more details.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

DRV PACKAGE
2mm x 2mm SON-6
(TOP VIEW)



(1) All ground pins must be connected to ground for proper operation.

(2) It is recommended that the thermal pad be grounded.

Table 1. PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
OUT	1	Regulated output voltage pin. A small (1 µF) ceramic capacitor is needed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* in the Application Information section for more details.
NC	2	Not connected
EN	4	Driving the enable pin (EN) over 1.2 V turns ON the regulator. Driving this pin below 0.4 V puts the regulator into shutdown mode, reducing operating current to 18 nA typical.
GND	3, 5	ALL ground pins must be tied to ground for proper operation.
IN	6	Input pin. A small capacitor is needed from this pin to ground to assure stability. Typical input capacitor = 1.0 µF. Both input and output capacitor grounds should be tied back to the IC ground with no significant impedance between them.
Thermal pad	Thermal pad	It is recommended that the thermal pad on the SON-6 package be connected to ground.

TYPICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{IN} = 1 µF (unless otherwise noted)

LINE REGULATION
I_{OUT} = 5 mA, V_{OUT} = 2.7 V (typ)
TPS78227

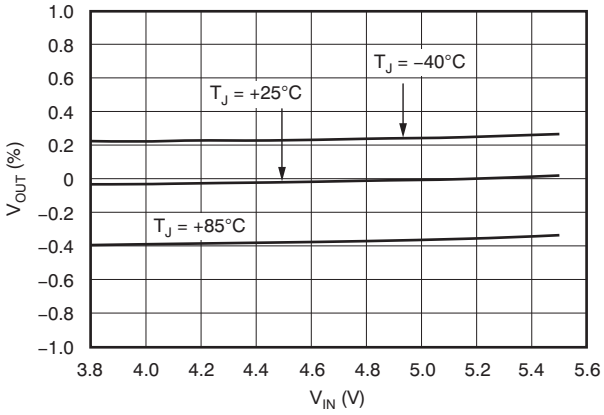


Figure 1.

LINE REGULATION
I_{OUT} = 150 mA, V_{OUT} = 2.7 V (typ)
TPS78227

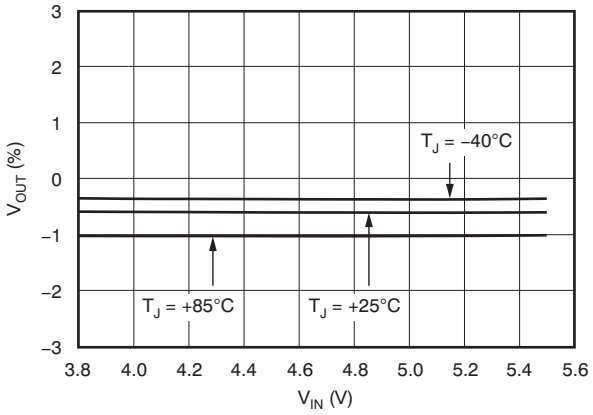


Figure 2.

LOAD REGULATION
V_{IN} = 3.8 V, V_{OUT} = 2.7 V
TPS78227

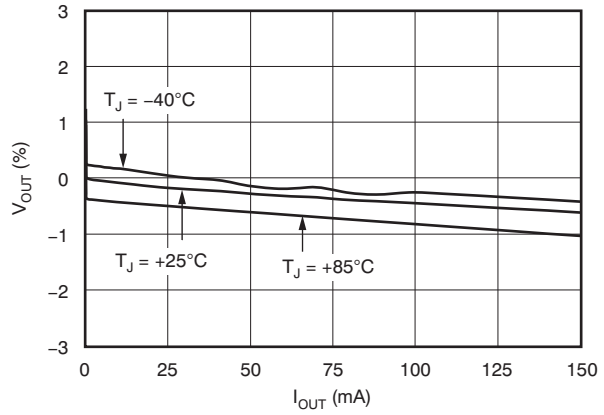


Figure 3.

DROPOUT VOLTAGE
vs
OUTPUT CURRENT
V_{OUT} = 2.7 V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS78227

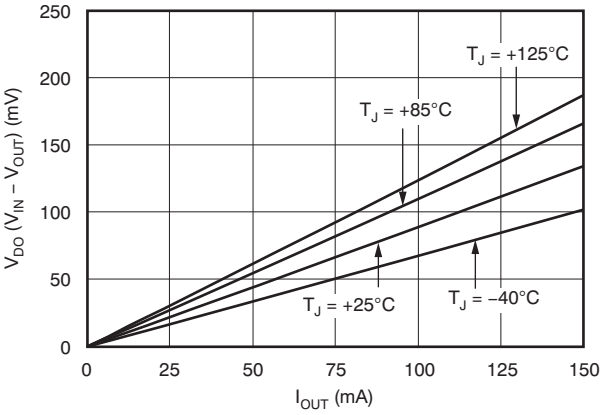


Figure 4.

TYPICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{IN} = 1 µF (unless otherwise noted)

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE
V_{OUT} = 2.7 V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS78227

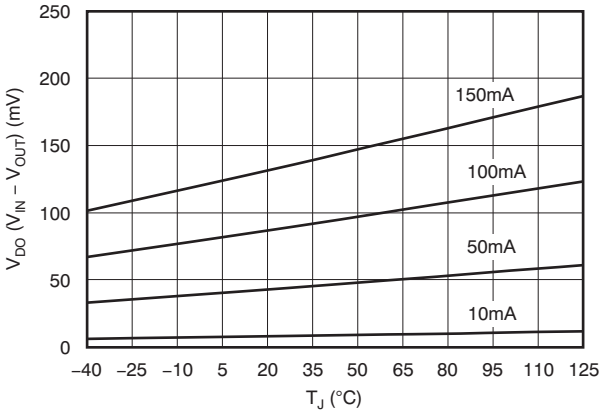


Figure 5.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 50 mA, V_{OUT} = 2.7 V
TPS78227

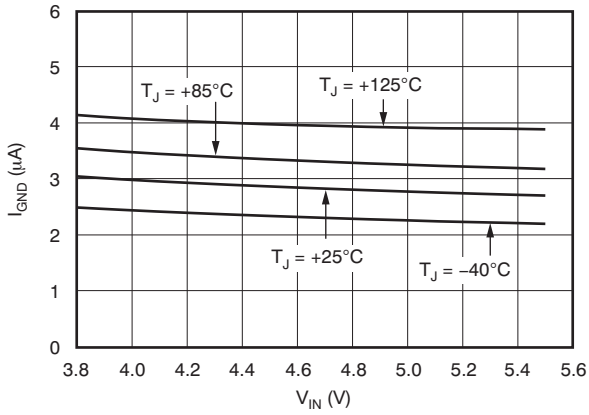


Figure 6.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 150 mA, V_{OUT} = 2.7 V
TPS78227

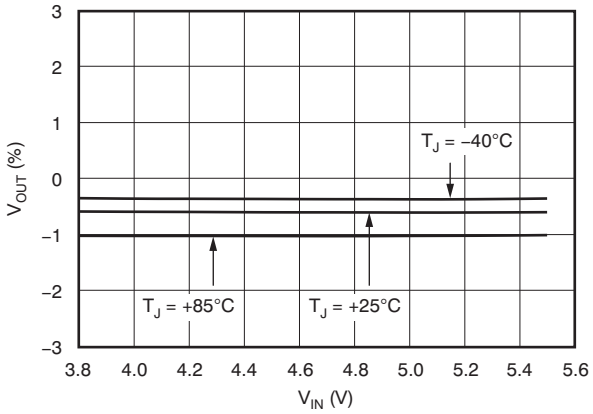


Figure 7.

CURRENT LIMIT vs INPUT VOLTAGE
V_{OUT} = 95% V_{OUT} (typ), V_{OUT} = 2.7 V (typ)
TPS78227

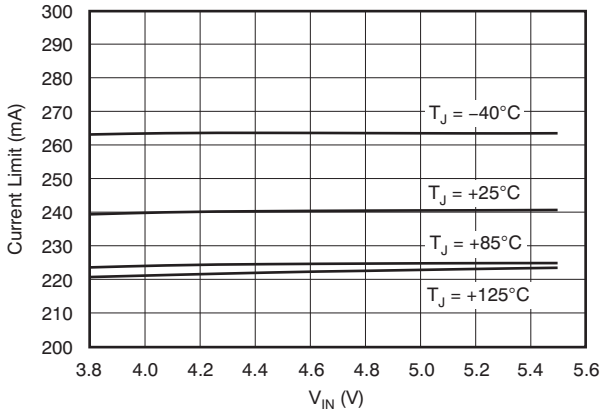


Figure 8.

TYPICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{IN} = 1 µF (unless otherwise noted)

ENABLE PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100 µA, V_{OUT} = 2.7 V
TPS78227

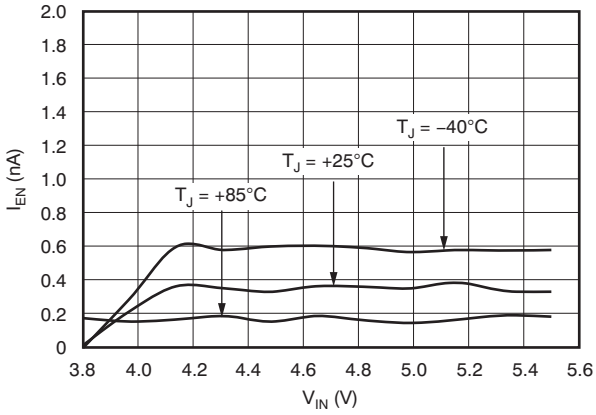


Figure 9.

ENABLE PIN HYSTERESIS vs JUNCTION TEMPERATURE
I_{OUT} = 1 mA, TPS78227

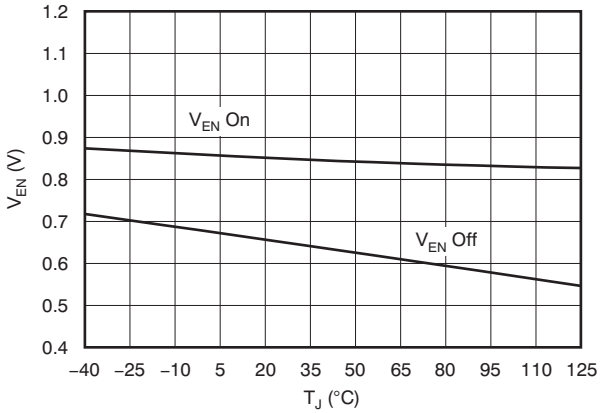


Figure 10.

$\%\Delta V_{OUT}$ vs JUNCTION TEMPERATURE
V_{IN} = 3.3 V, V_{OUT} = 2.7 V (typ)
TPS78227

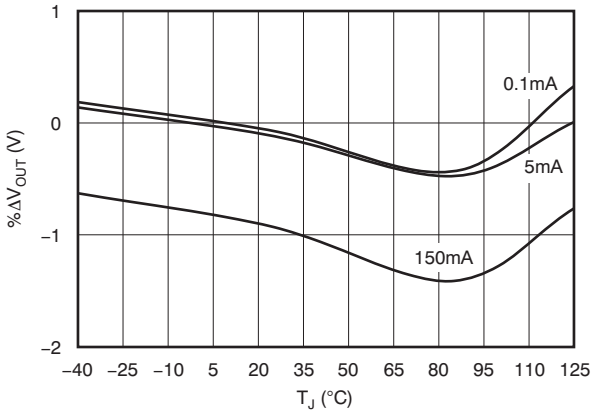


Figure 11.

$\%\Delta V_{OUT}$ vs JUNCTION TEMPERATURE
V_{IN} = 3.7 V, V_{OUT} = 2.7 V (typ)
TPS78227

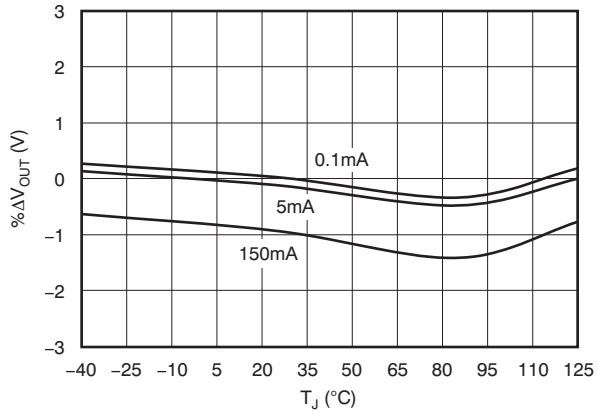


Figure 12.

TYPICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, C_{IN} = 1 µF (unless otherwise noted)

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY
C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{IN} = 3.2 V
TPS78227

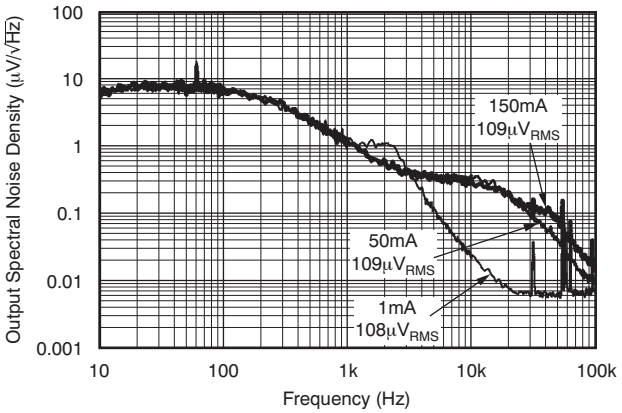


Figure 13.

RIPPLE REJECTION vs FREQUENCY
V_{IN} = 4.2 V, V_{OUT} = 2.7 V, C_{OUT} = 2.2 µF
TPS78227

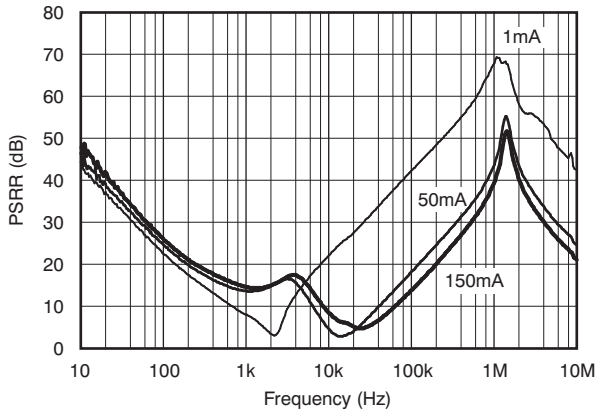


Figure 14.

APPLICATION INFORMATION

APPLICATION EXAMPLES

The TPS782xx family of LDOs is factory-programmable to have a fixed output. Note that during startup or steady-state conditions, it is important that the EN pin voltage never exceed V_{IN} + 0.3 V.

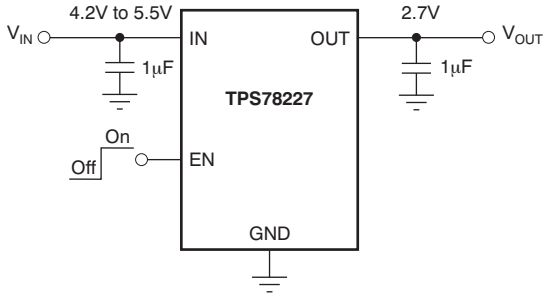


Figure 15. Typical Application Circuit

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS782xx series are designed to be stable with standard ceramic capacitors with values of 1.0 µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0 Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1 µF.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance (such as PSRR, output noise, and transient response), it is recommended that the printed circuit board (PCB) be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TPS782xx is internally current-limited to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS782xx series has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current may be appropriate.

SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low-voltage CMOS levels. When shutdown capability is not required, EN should be connected to the IN pin, as shown in Figure 16. The TPS782xx series, with internal active output pulldown circuitry, discharges the output to within 5% V_{OUT} with a time (*t*) shown in Equation 1:

$$t = 3 \left(\frac{10k\Omega \times R_L}{10k\Omega + R_L} \right) \times C_{OUT} \quad (1)$$

Where:

R_L = output load resistance

C_{OUT} = output capacitance

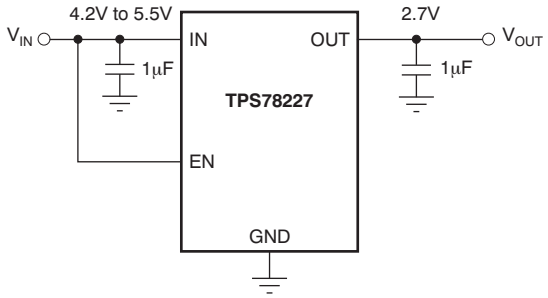


Figure 16. Circuit Showing EN Tied High when Shutdown Capability is Not Required

DROPOUT VOLTAGE

The TPS782xx series use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in the Typical Characteristics section. See the application report *Understanding LDO Dropout* (SLVA207) available for download from www.ti.com.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

ACTIVE V_{OUT} PULL-DOWN

In the TPS782xx series, the active pulldown discharges V_{OUT} when the device is off. However, the input voltage must be greater than 2.2 V for the active pulldown to work.

MINIMUM LOAD

The TPS782xx series are stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS782xx employs an innovative, low-current circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

THERMAL PROTECTION

Thermal protection disables the device output when the junction temperature rises to approximately 160°C, allowing the device to cool. Once the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS782xx series has been designed to protect against overload conditions. However, it is not intended to replace proper heatsinking. Continuously running the TPS782xx series into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the Dissipation Ratings table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS782xx series are available from the Texas Instruments web site at www.ti.com through the TPS782xx series product folders.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS78225QDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NSY	Samples
TPS78227QDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFH	Samples
TPS78228QDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFI	Samples
TPS78230QDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS782-Q1 :

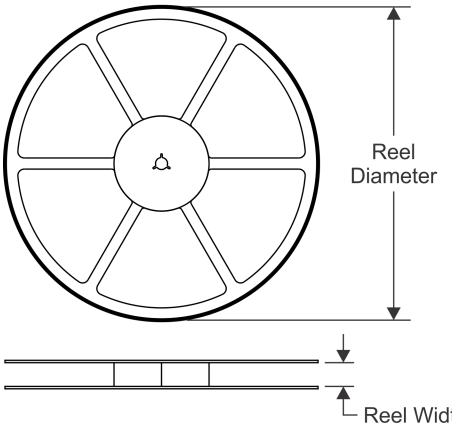
- Catalog: TPS782

NOTE: Qualified Version Definitions:

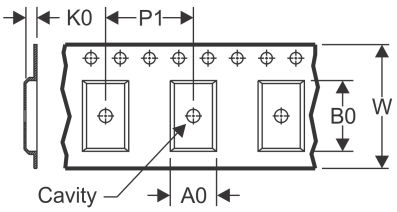
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

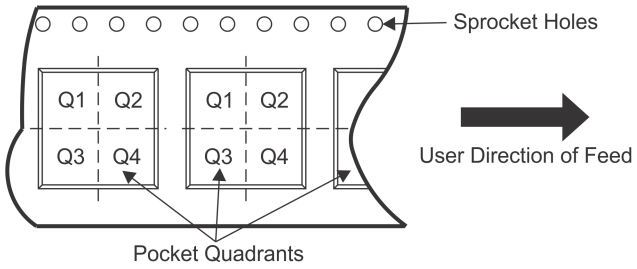


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

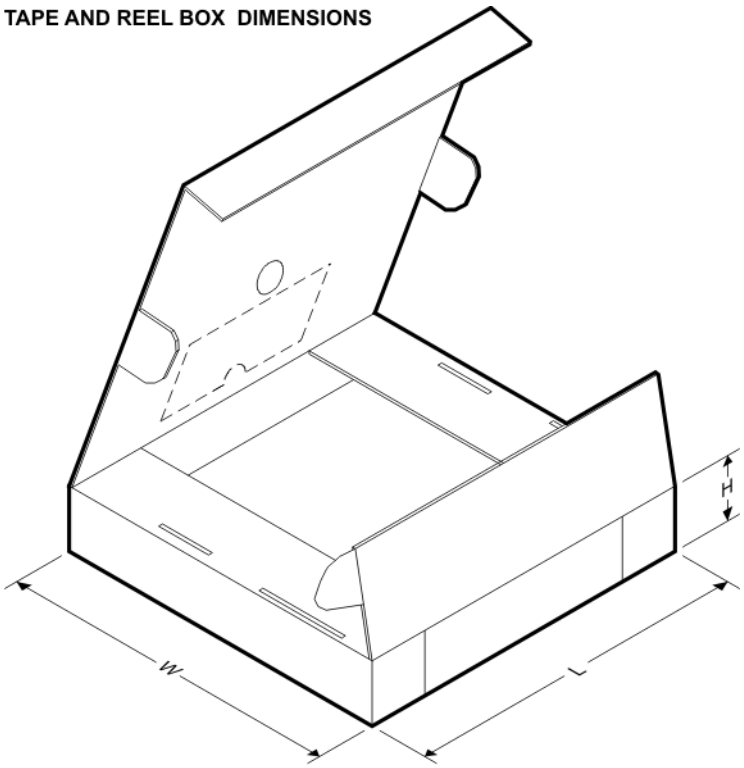
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78225QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78227QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78228QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS78230QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

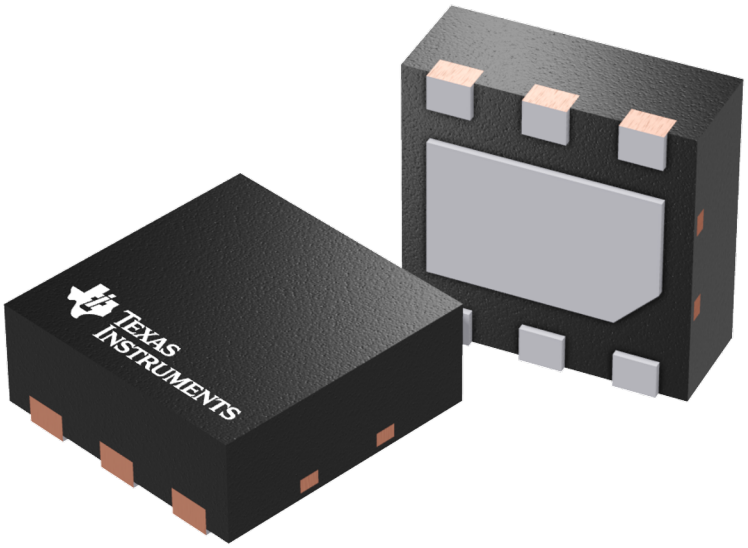


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78225QDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78227QDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78228QDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TPS78230QDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



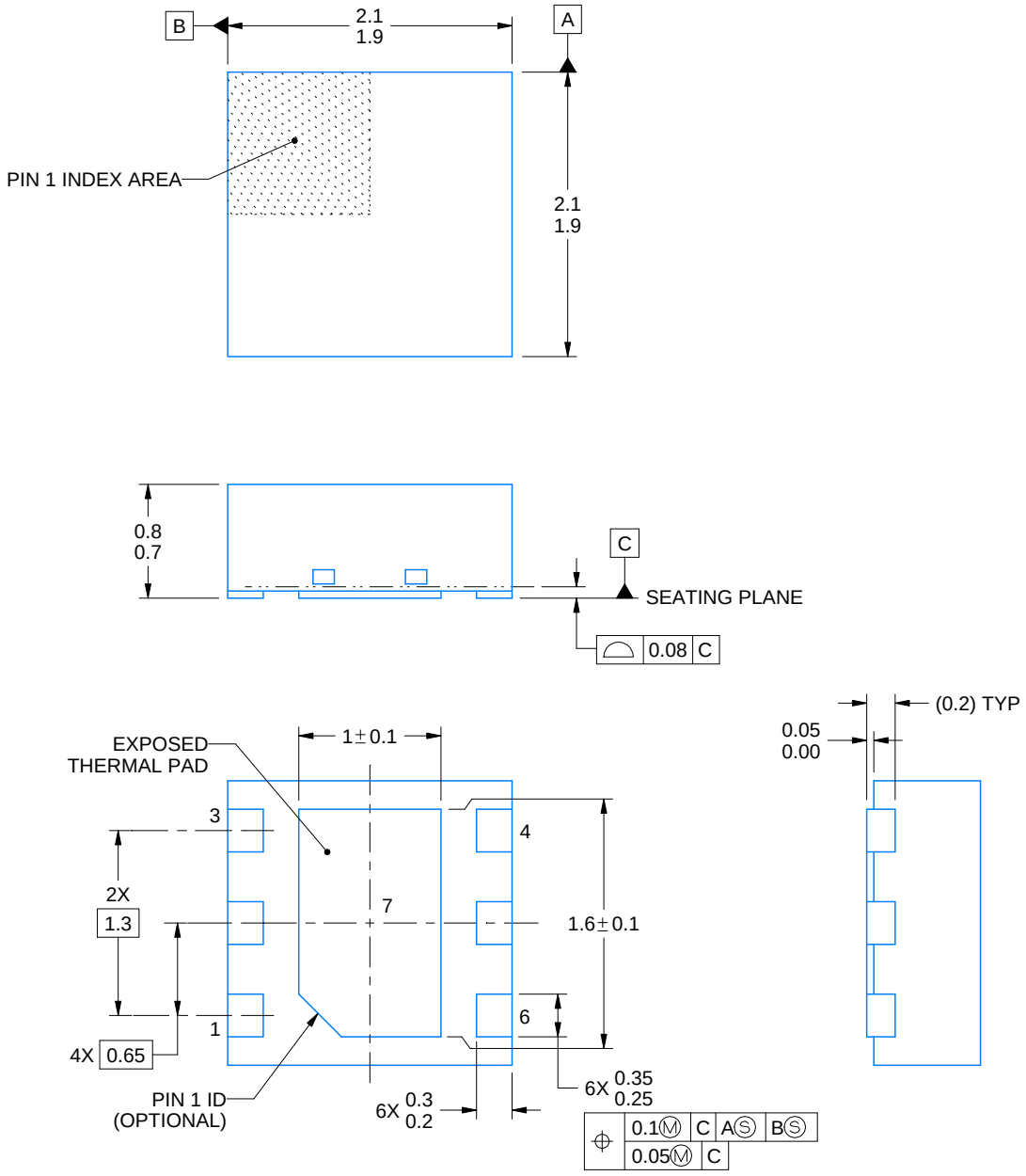
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

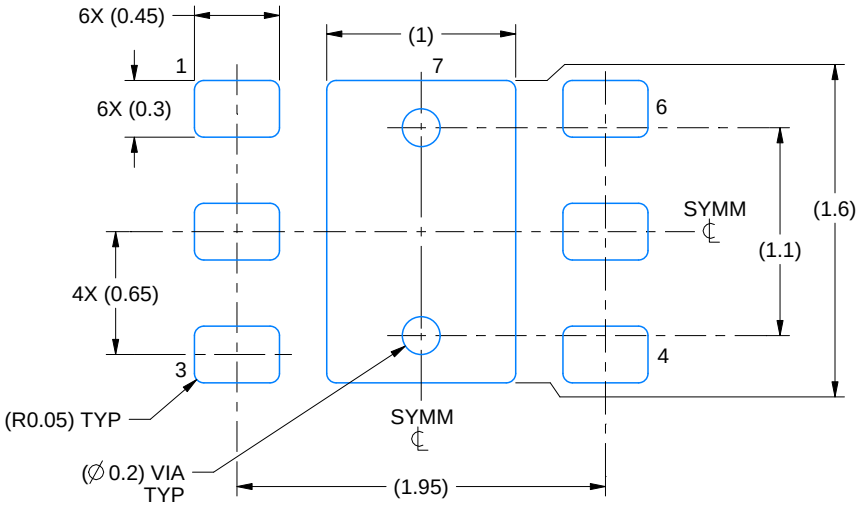
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

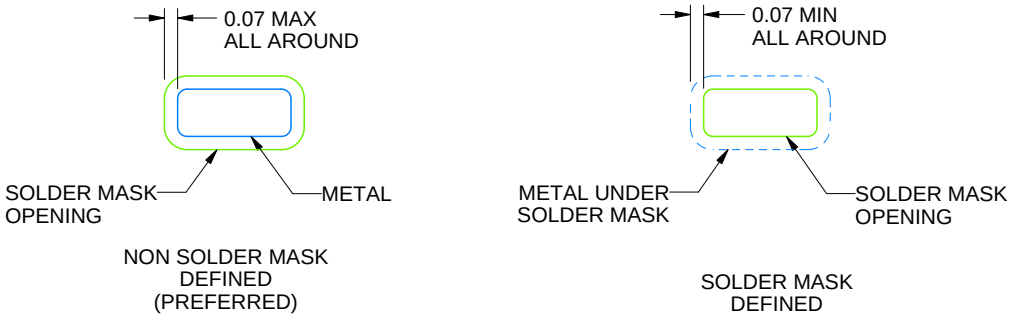


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

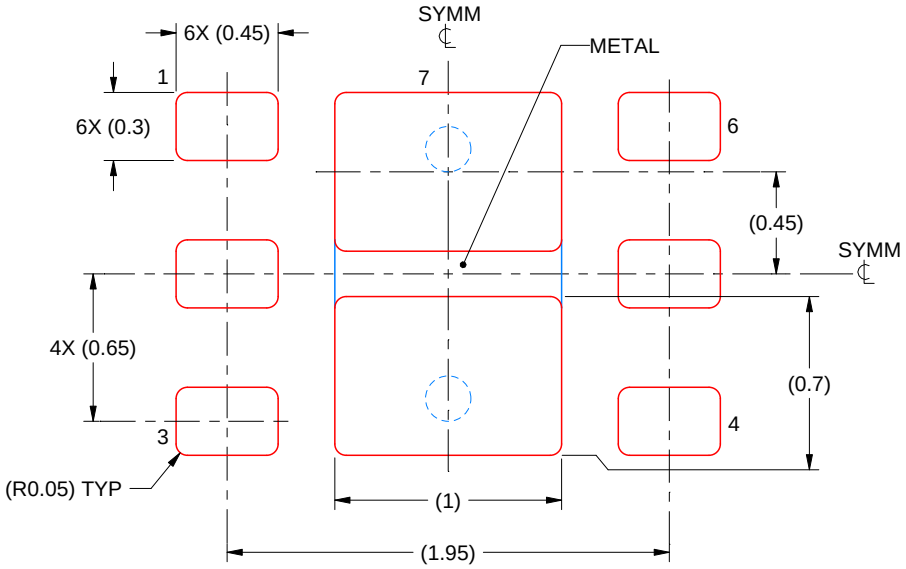
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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