

LMC6064 Precision CMOS Quad Micropower Operational Amplifier

Check for Samples: [LMC6064](#)

FEATURES

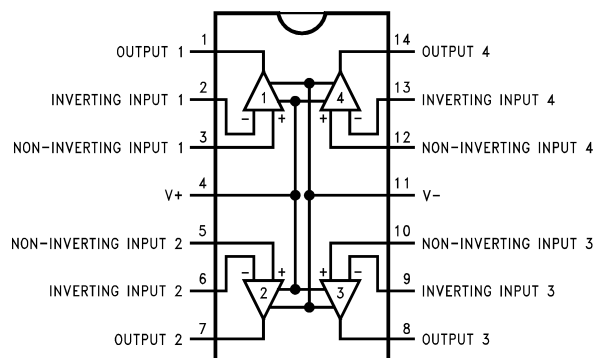
(Typical Unless Otherwise Noted)

- **Low Offset Voltage: 100 μ V**
- **Ultra Low Supply Current: 16 μ A/Amplifier**
- **Operates from 4.5V to 15V Single Supply**
- **Ultra Low Input Bias Current: 10 fA**
- **Output Swing within 10 mV of Supply Rail, 100k Load**
- **Input Common-Mode Range Includes V^-**
- **High Voltage Gain: 140 dB**
- **Improved Latchup Immunity**

APPLICATIONS

- **Instrumentation Amplifier**
- **Photodiode and Infrared Detector Preamplifier**
- **Transducer Amplifiers**
- **Hand-Held Analytic Instruments**
- **Medical Instrumentation**
- **D/A Converter**
- **Charge Amplifier for Piezoelectric Transducers**

Connection Diagram



**14-Pin PDIP/SOIC
Top View**

DESCRIPTION

The LMC6064 is a precision quad low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption make the LMC6064 ideally suited for battery powered applications.

Other applications using the LMC6064 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with TI's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6084 precision quad operational amplifier.

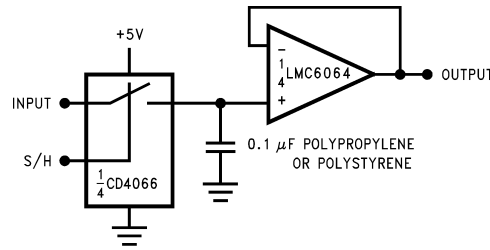
For single or dual operational amplifier with similar features, see the LMC6061 or LMC6062 respectively.

PATENT PENDING



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



Low-Leakage Sample and Hold



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V ⁺) +0.3V, (V ⁻) -0.3V
Supply Voltage (V ⁺ - V ⁻)	16V
Output Short Circuit to V ⁺	See (4)
Output Short Circuit to V ⁻	See (5)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	-65°C to +150°C
Junction Temperature	150°C
ESD Tolerance(6)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	See (7)

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) For ensured Military Temperature Range parameters see RETSMC6064X.
- (4) Do not connect output to V⁺, when V⁺ is greater than 13V or reliability will be adversely affected.
- (5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
- (6) Human body model, 1.5 kΩ in series with 100 pF.
- (7) The maximum power dissipation is a function of T_{J(Max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(Max)} - T_A)/θ_{JA}.

Operating Ratings (1)

Temperature Range	LMC6064AM	-55°C ≤ T _J ≤ +125°C
	LMC6064AI, LMC6064I	-40°C ≤ T _J ≤ +85°C
Supply Voltage		4.5V ≤ V ⁺ ≤ 15.5V
Thermal Resistance (θ _{JA}) ⁽²⁾	14-Pin PDIP	81°C/W
	14-Pin SOIC	126°C/W
Power Dissipation		See (3)

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
- (2) All numbers apply for packages soldered directly into a PC board.
- (3) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with P_D = (T_J-T_A)/θ_{JA}.

DC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	LMC6064AM Limit ⁽²⁾	LMC6064AI Limit ⁽²⁾	LMC6064I Limit ⁽²⁾	Units	
V_{OS}	Input Offset Voltage		100	350 1200	350 900	800 1300	μV Max	
TCV_{OS}	Input Offset Voltage Average Drift		1.0				$\mu\text{V}/^\circ\text{C}$	
I_B	Input Bias Current		0.010	100	4	4	pA Max	
I_{OS}	Input Offset Current		0.005	100	2	2	pA Max	
R_{IN}	Input Resistance		>10				Tera Ω	
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 12.0\text{V}$ $V^+ = 15\text{V}$	85	75 70	75 72	66 63	dB Min	
+PSRR	Positive Power Supply Rejection Ratio	$5\text{V} \leq V^+ \leq 15\text{V}$ $V_O = 2.5\text{V}$	85	75 70	75 72	66 63	dB Min	
-PSRR	Negative Power Supply Rejection Ratio	$0\text{V} \leq V^- \leq -10\text{V}$	100	84 70	84 81	74 71	dB Min	
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5\text{V}$ and 15V for CMRR $\geq 60\text{ dB}$	-0.4	-0.1 0	-0.1 0	-0.1 0	V Max	
			$V^+ - 1.9$	$V^+ - 2.3$ $V^+ - 2.6$	$V^+ - 2.3$ $V^+ - 2.5$	$V^+ - 2.3$ $V^+ - 2.5$	V Min	
A_V	Large Signal Voltage Gain	$R_L = 100\text{ k}\Omega^{(3)}$	Sourcing	4000	400 200	400 300	300 200	V/mV Min
			Sinking	3000	180 70	180 100	90 60	V/mV Min
		$R_L = 25\text{ k}\Omega^{(3)}$	Sourcing	3000	400 150	400 150	200 80	V/mV Min
			Sinking	2000	100 35	100 50	70 35	V/mV Min

(1) Typical values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	LMC6064AM Limit ⁽²⁾	LMC6064AI Limit ⁽²⁾	LMC6064I Limit ⁽²⁾	Units		
V_O	Output Swing	$V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to 2.5V	4.995	4.990 4.970	4.990 4.980	4.950 4.925	V Min		
			0.005	0.010 0.030	0.010 0.020	0.050 0.075	V Max		
			$V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to 2.5V	4.990	4.975 4.955	4.975 4.965	4.950 4.850	V Min	
				0.010	0.020 0.045	0.020 0.035	0.050 0.150	V Max	
			$V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to 7.5V	14.990	14.975 14.955	14.975 14.965	14.950 14.925	V Min	
				0.010	0.025 0.050	0.025 0.035	0.050 0.075	V Max	
		$V^+ = 15\text{V}$ $R_L = 25\text{ k}\Omega$ to 7.5V	14.965	14.900 14.800	14.900 14.850	14.850 14.800	V Min		
			0.025	0.050 0.200	0.050 0.150	0.100 0.200	V Max		
		I_O	Output Current $V^+ = 5\text{V}$	Sourcing, $V_O = 0\text{V}$	22	16 8	16 10	13 8	mA Min
					21	16 7	16 8	16 8	mA Min
				Sinking, $V_O = 5\text{V}$	25	15 9	15 10	15 10	mA Min
					26	20 7	20 8	20 8	mA Min
I_S	Supply Current	All Four Amplifiers $V^+ = +5\text{V}$, $V_O = 1.5\text{V}$	64	76 120	76 92	92 112	μA Max		
			80	94 140	94 110	114 132	μA Max		
		All Four Amplifiers $V^+ = +15\text{V}$, $V_O = 7.5\text{V}$	64	76 120	76 92	92 112	μA Max		
			80	94 140	94 110	114 132	μA Max		

(4) Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

AC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$, **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	LMC6064AM Limit ⁽²⁾	LMC6064AI Limit ⁽²⁾	LMC6064I Limit ⁽²⁾	Units
SR	Slew Rate	See ⁽³⁾	35	20 8	20 10	15 7	V/ms Min
GBW	Gain-Bandwidth Product		100				kHz
θ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	See ⁽⁴⁾	155				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83				nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/ $\sqrt{\text{Hz}}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\text{ k}\Omega$, $V_O = 2\text{ V}_{PP}$ $\pm 5\text{V}$ Supply	0.01				%

(1) Typical values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

(4) Input referred $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V. Each amp excited in turn with 100 Hz to produce $V_O = 12\text{ V}_{PP}$.

Typical Performance Characteristics

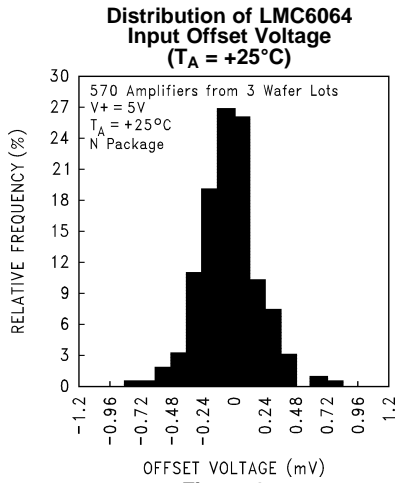


Figure 1.

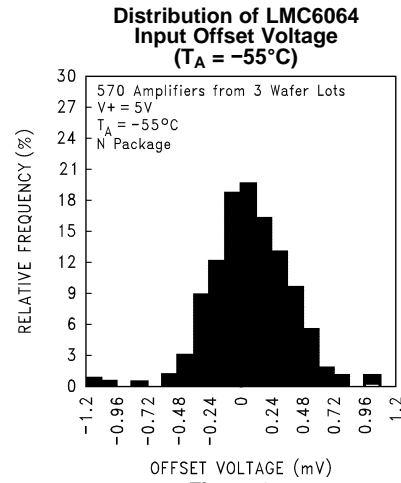


Figure 2.

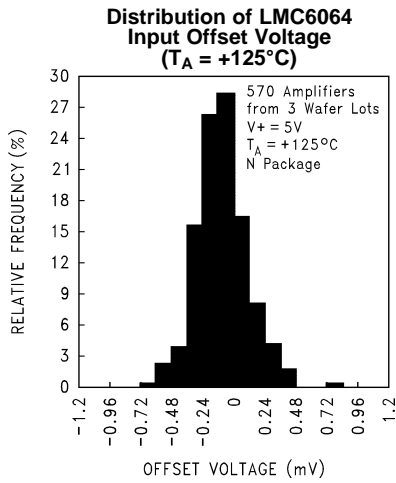


Figure 3.

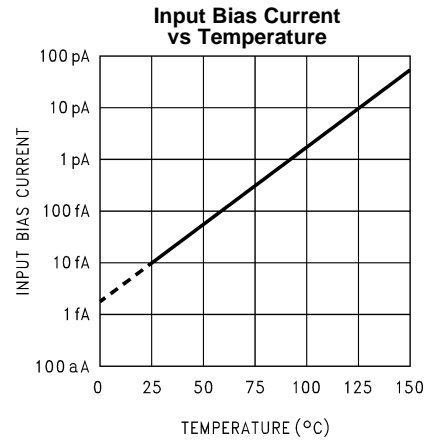


Figure 4.

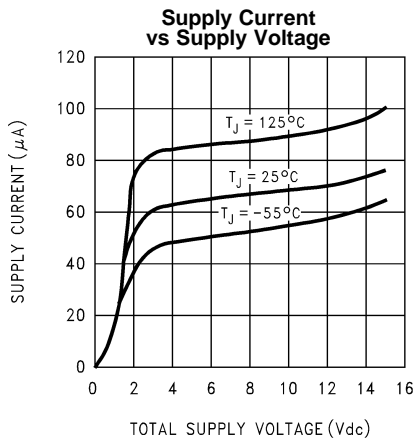


Figure 5.

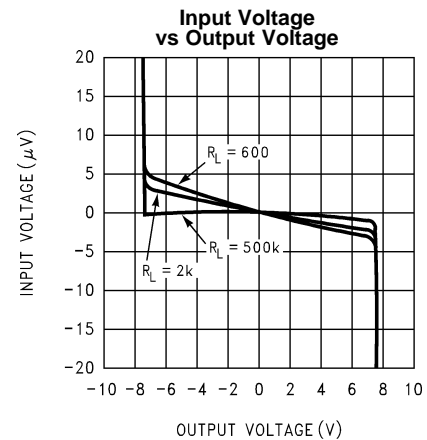


Figure 6.

Typical Performance Characteristics (continued)

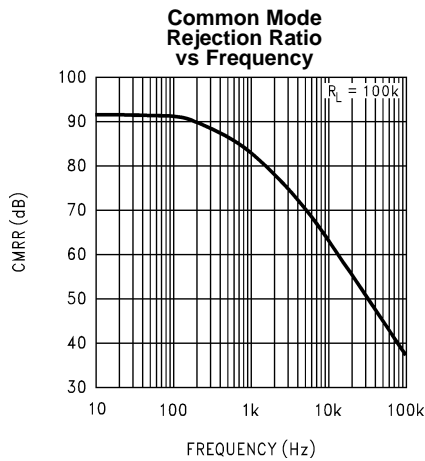


Figure 7.

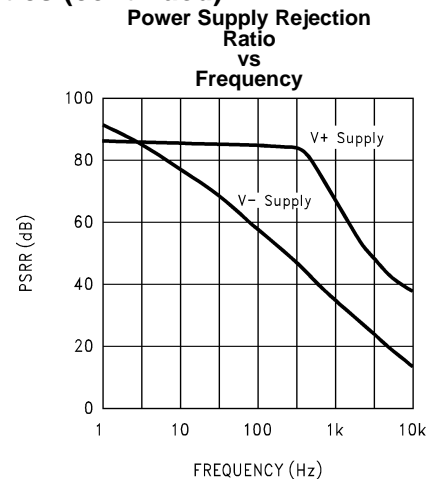


Figure 8.

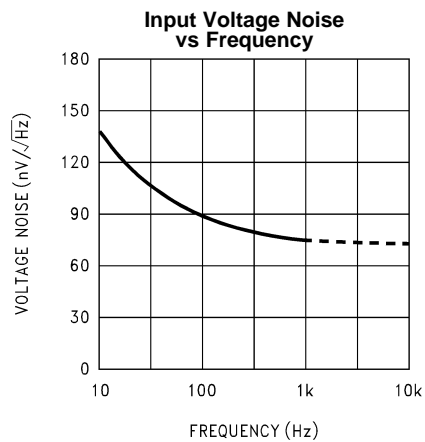


Figure 9.

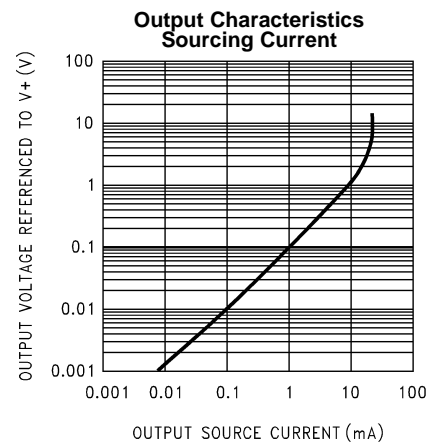


Figure 10.

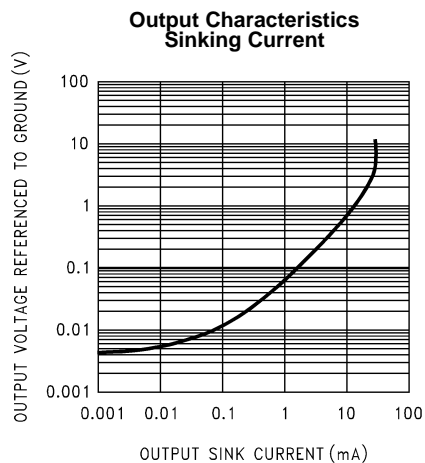


Figure 11.

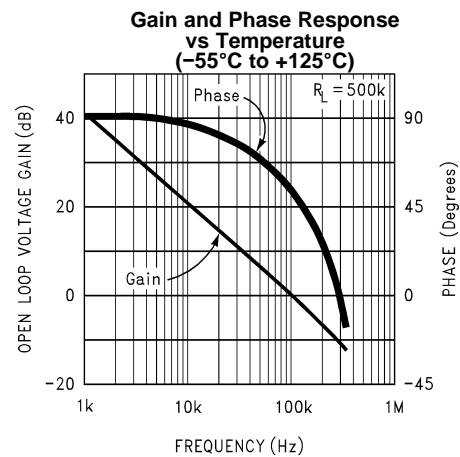


Figure 12.

Typical Performance Characteristics (continued)

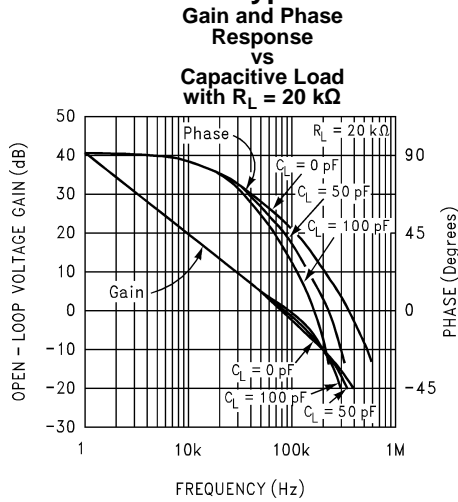


Figure 13.

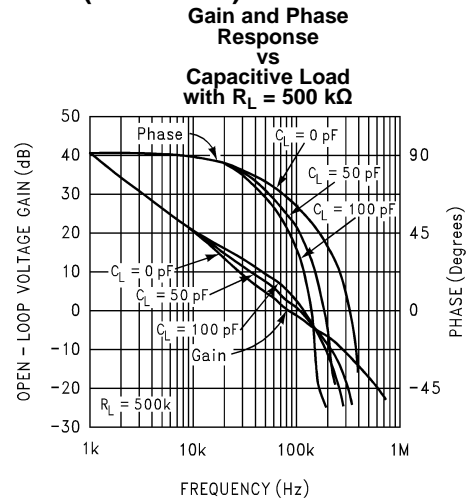


Figure 14.

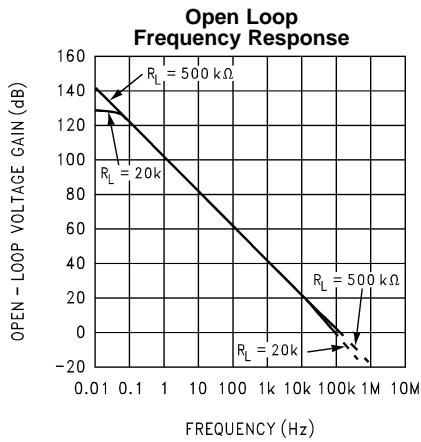


Figure 15.

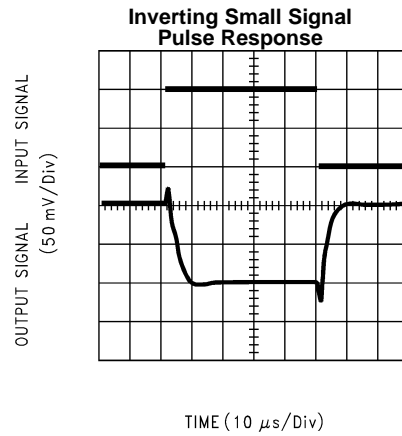


Figure 16.

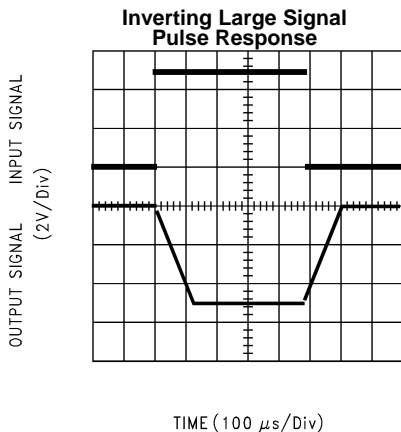


Figure 17.

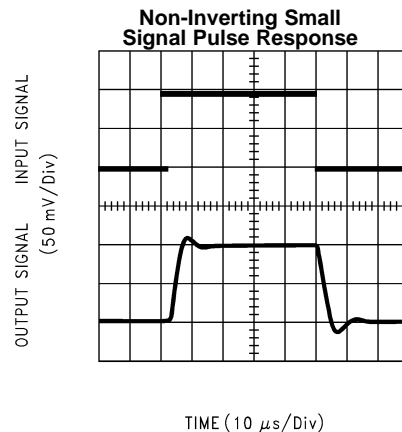


Figure 18.

Typical Performance Characteristics (continued)

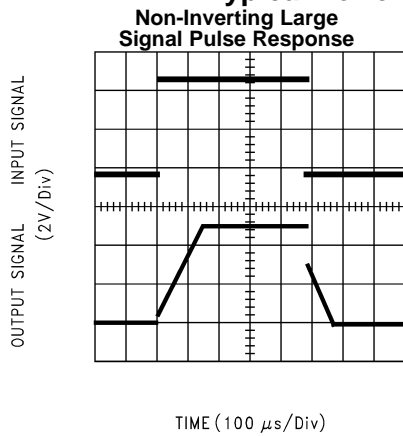


Figure 19.

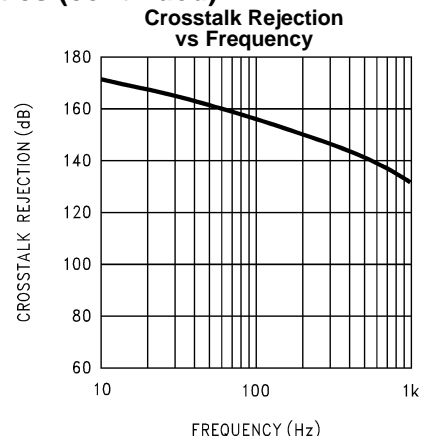


Figure 20.

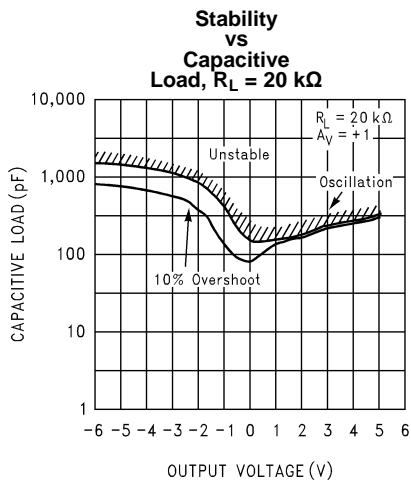


Figure 21.

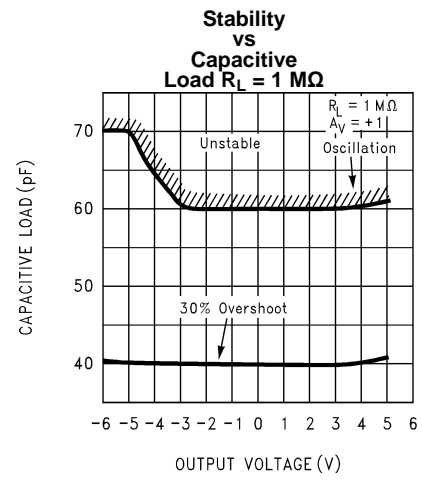


Figure 22.

APPLICATIONS HINTS

AMPLIFIER TOPOLOGY

The LMC6064 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6064 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6064.

Although the LMC6064 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6064 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See [Printed-Circuit-Board Layout for High Impedance Work](#)).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f , around the feedback resistor (as in [Figure 23](#)) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

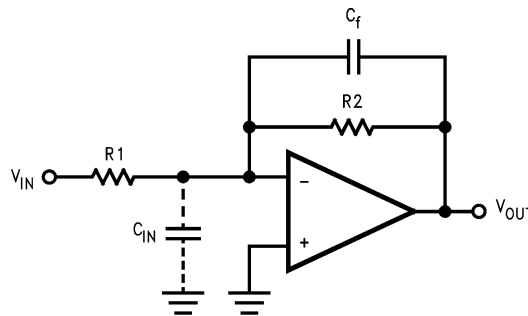


Figure 23. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see [typical curves](#)).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in [Figure 24](#).

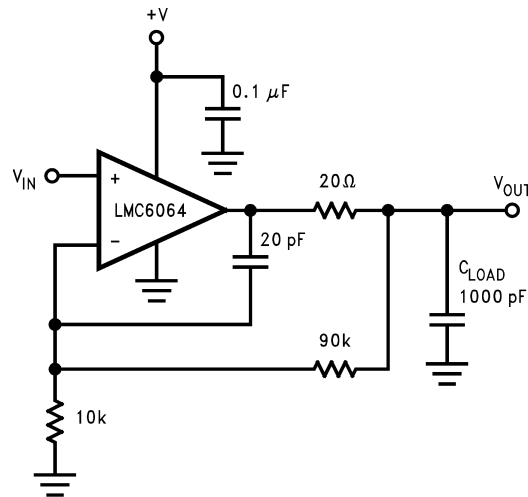


Figure 24. LMC6064 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of [Figure 24](#), R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V⁺ ([Figure 25](#)). Typically a pull up resistor conducting 10 μ A or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see [Electrical Characteristics](#)).

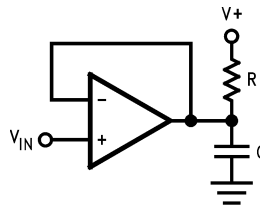


Figure 25. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6064, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6064's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in [Figure 26](#). To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6064's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See [Figure 27](#) for typical connections of guard rings for standard op-amp configurations.

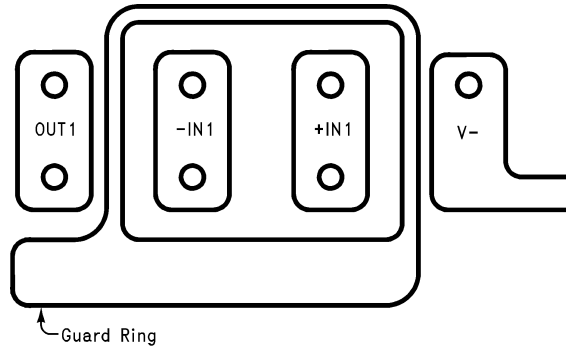


Figure 26. Example of Guard Ring in P.C. Board Layout

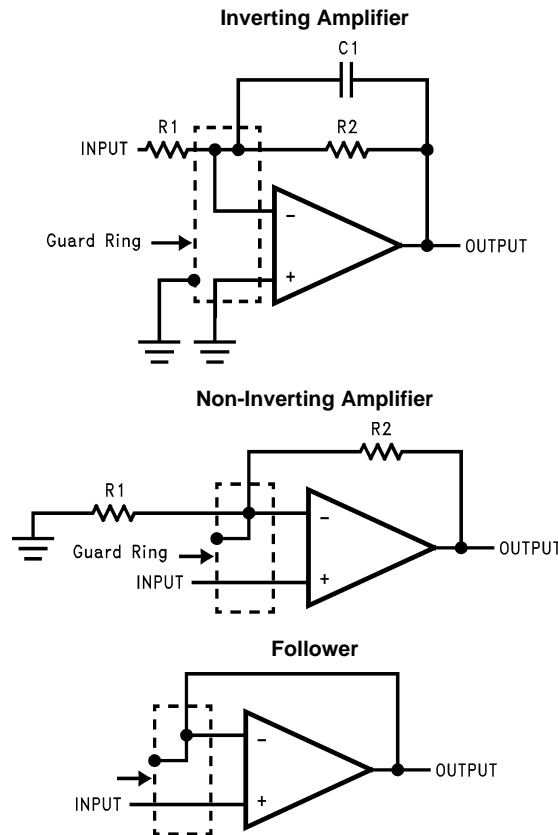
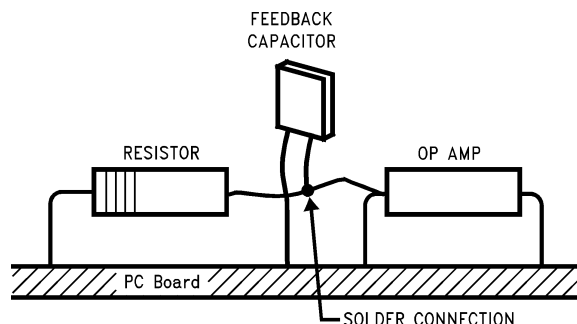


Figure 27. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See [Figure 28](#).

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6064 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

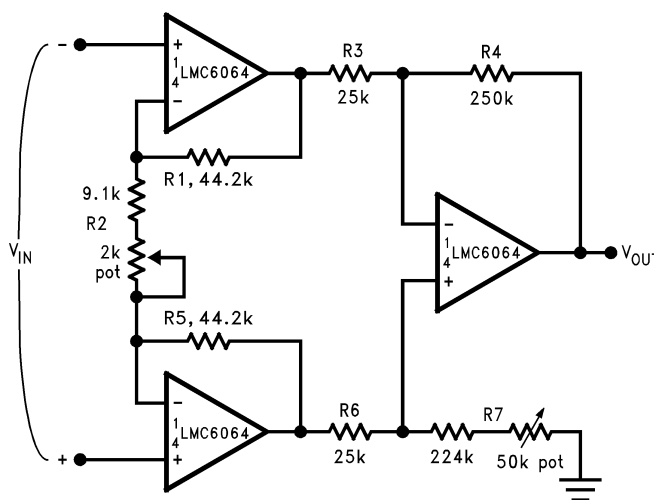
Figure 28. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6064 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 29 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 $\mu V/^\circ C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

∴ $A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

Figure 29. Instrumentation Amplifier

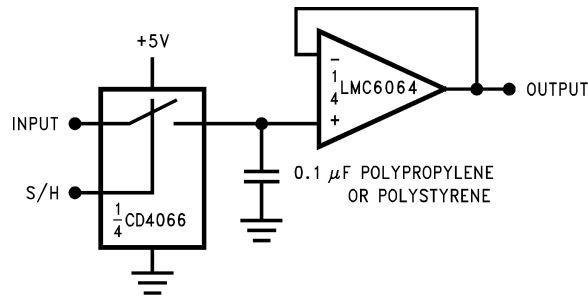


Figure 30. Low-Leakage Sample and Hold

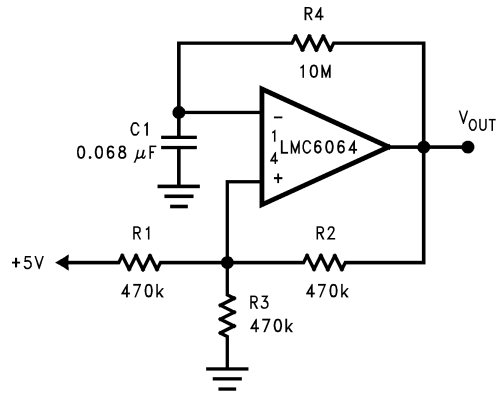


Figure 31. 1 Hz Square Wave Oscillator

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format <hr/>	<hr/> 14 <hr/>

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6064AIM	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LMC6064 AIM	
LMC6064AIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6064 AIM	Samples
LMC6064AIMX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LMC6064 AIM	
LMC6064AIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6064 AIM	Samples
LMC6064IM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6064IM	Samples
LMC6064IMX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LMC6064IM	
LMC6064IMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6064IM	Samples
LMC6064IN	NRND	PDIP	NFF	14	25	TBD	Call TI	Call TI	-40 to 85	LMC6064IN	
LMC6064IN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LMC6064IN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

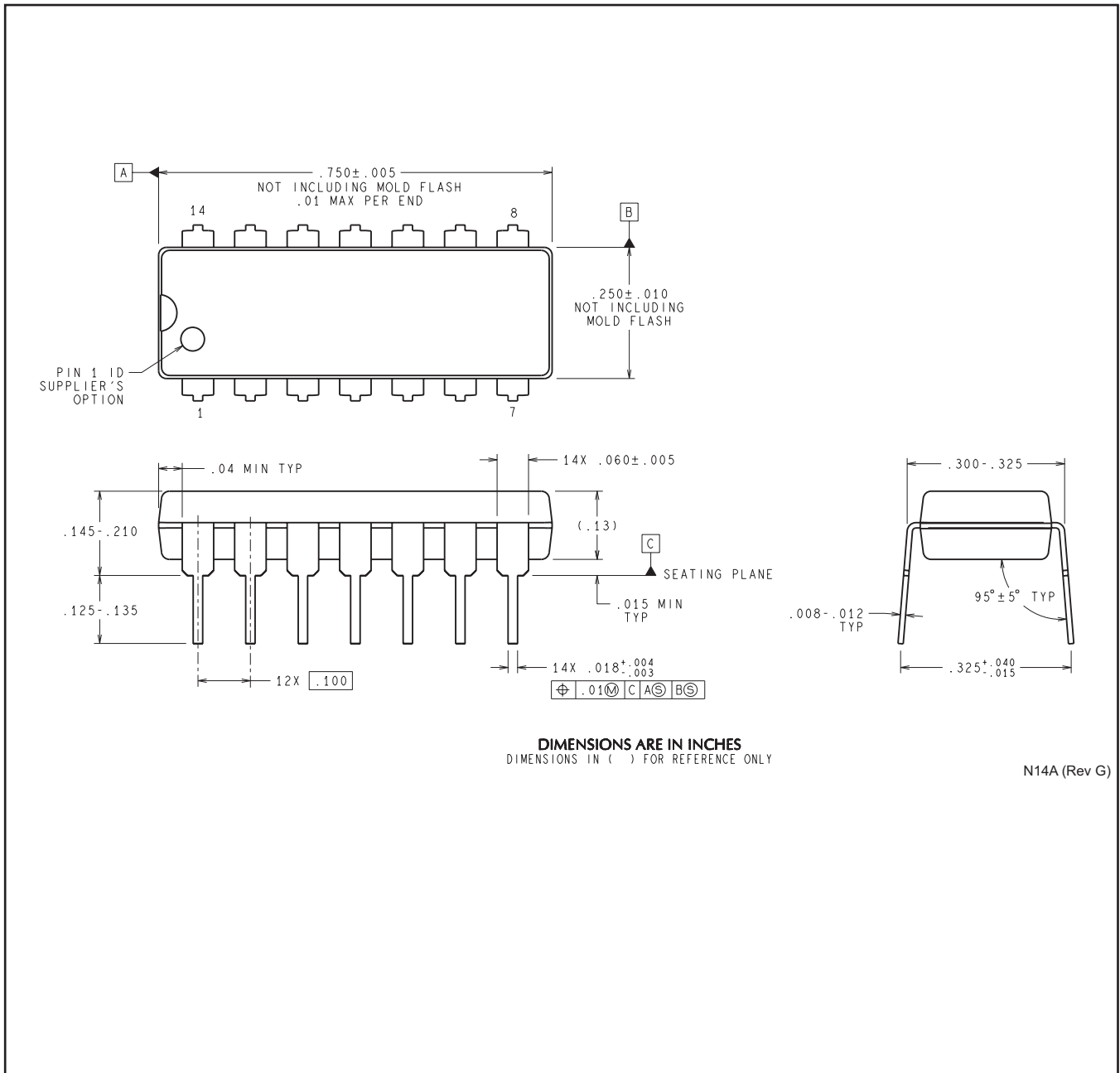
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6064AIMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6064AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6064IMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6064IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6064AIMX	SOIC	D	14	2500	367.0	367.0	35.0
LMC6064AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMC6064IMX	SOIC	D	14	2500	367.0	367.0	35.0
LMC6064IMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

NFF0014A

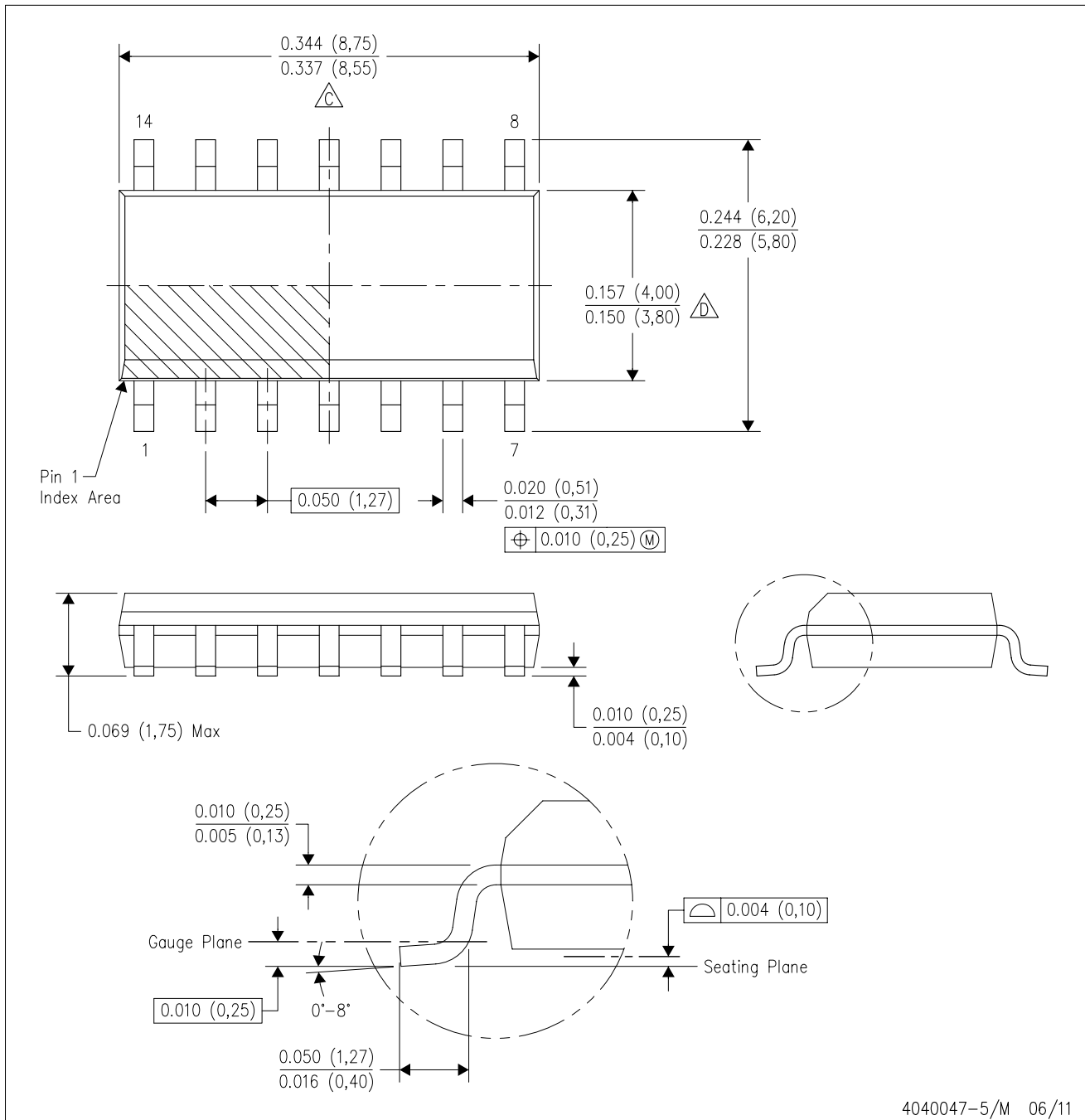


DIMENSIONS ARE IN INCHES
 DIMENSIONS IN () FOR REFERENCE ONLY

N14A (Rev G)

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com