Evaluation Board for the 1 MSPS 12-Bit Impedance Converter Network Analyzer

Preliminary Technical Data

EVAL-AD5933EB

FEATURES

Full-featured evaluation board for the AD5933
Graphic user interface software with frequency sweep capability for board control and data analysis
Various power supply linking options
Standalone capability with serial I²C loading from on-board microcontroller
Selectable system clock options, including internal RC oscillator or on-board 16 MHz crystal

APPLICATIONS

Electrochemical analysis
Impedance spectroscopy
Complex impedance measurement
Corrosion monitoring and protection equipment
Biomedical and automotive sensors
Proximity sensing

GENERAL DESCRIPTION

This document describes the evaluation board for the AD5933 and the application software developed to interface to the device.

The AD5933 is a high precision impedance converter system that combines an on-board frequency generator with a 12-bit, 1 MSPS ADC. The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC, and the DFT is processed by an on-board DSP engine at each excitation frequency. The AD5933 also contains an internal temperature sensor with 13-bit resolution and operates from a 2.7 V to 5.5 V supply.

Other on-board components include an ADR423 3.0 V reference that acts as a stable supply voltage for the separate analog and digital sections of the device and an ADP3303 ultrahigh precision regulator that acts as a supply to the on-board universal serial bus controller, which interfaces to the AD5933. The user can power the entire circuitry from the USB port of a computer. The evaluation board also has a high performance, trimmed, 16 MHz, surface-mount crystal that can act as a system clock for the AD5933, if required.

The various link options available on the evaluation board are explained in Table 2. Interfacing to the AD5933 is through a USB microcontroller, which generates the I²C signals necessary to communicate with the AD5933.The user interfaces to the USB microcontroller through a Visual Basic® graphic user interface located on and run from the user PC. More information on the AD5933 is available from Analog Devices, Inc., at www.analog.com and should be consulted when using the evaluation board.

FUNCTIONAL BLOCK DIAGRAM

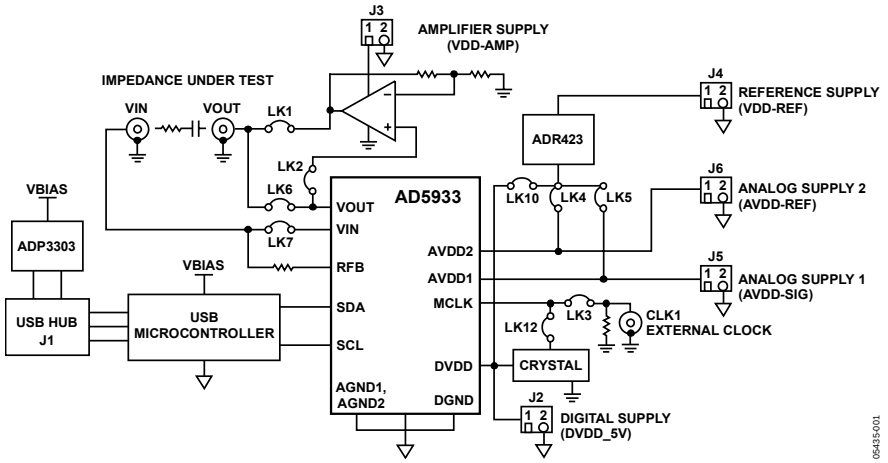

Figure 1. AD5933 Evaluation Board Block Diagram

Rev. PrC

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REVISION HISTORY

7/07—Revision PrC

EVALUATION BOARD HARDWARE

TERMINAL BLOCK FUNCTIONS

Table 1. Terminal Block Function Descriptions

Pin	Name	Description
J1	USB	USB Hub for the Evaluation Board.
J2-1	DVDD-5V	Digital Circuitry Supply Connection to Pin 9. This connector is decoupled to the digital ground plane via standard 0.1 µF and 10 µF suppression capacitors. This connector also supplies the high performance, 16 MHz, surface-mount crystal with the required operating supply voltage.
J2-2	DGND	Digital Ground Connection. This connector is decoupled to J2-1 using standard 0.1 µF and 10 µF suppression capacitors. The digital ground plane is connected to the analog ground plane at a single point underneath the board.
J3 -1	VDD-AMP	Single-Supply Amplifier Connection. There is a facility to place a single-supply operational amplifier (user supplied) on the output voltage pin (VOUT) of the AD5933. This terminal block is a connection to the single-supply positive rail of the operation amplifier.
J3-2	AGND	Analog Ground Connection. This connector is decoupled to J3-1 using standard 0.1 µF and 10 µF suppression capacitors. The analog ground plane is connected to the digital ground plane at a single point underneath the board.
J4-1	AVDD-REF	Analog Reference Input Supply to Pin 11. This connector is decoupled to J4-2 via standard 0.1 µF and 10 µF suppression capacitors.
J4-2	AGND	Analog Ground Connection. This connector is decoupled to J4-1 using standard 0.1 µF and 10 µF suppression capacitors. The analog ground plane is connected to the digital ground plane at a single point underneath the board.
J5-1	AVDD-SIG	Analog Circuit Input Supply to Pin 10. This connector is decoupled to J5-2 via standard 0.1 µF and 10 µF suppression capacitors.
J5-2	AGND	Analog Ground Connection. This connector is decoupled to J5-1 using standard 0.1 µF and 10 µF suppression capacitors. The analog ground plane is connected to the digital ground plane at a single point underneath the board.
J6-1	VDD-REF	Power Supply Connection for On-Board Reference. This provides a connection to the power supply pin of the on-board reference at U4 (ADR423).
J6-2	AGND	Analog Ground Connection. This connector is decoupled to J6-1 using standard 0.1 µF and 10 µF suppression capacitors. The analog ground plane is connected to the digital ground plane at a single point underneath the board.

LINK FUNCTIONS

Table 2. Link Function Descriptions

Link No.	Function
LK1	Link 1 is used to connect the output of the optional user-supplied external operational amplifier (U1) to the VOUT SMB connector (see Figure 1). This op amp can be used to amplify/buffer the output excitation voltage from the AD5933. Link 1 is used in conjunction with Link 6 and Link 2. When Link 1 and Link 2 are inserted, Link 6 should be removed and vice versa. The output of the AD5933 either can be connected to the external op amp by removing Link 6 (LK6) and inserting Link 1 and Link 2 (LK1 and LK2) and then routing to SMB VOUT or can be directly routed to SMB VOUT by removing Link 1 and Link 2 (LK1 and LK2) and inserting Link 6 (LK6). Therefore, the signal path is determined by suitably inserting/removing Link 1, Link 2, and Link 6. • When Link 1 is inserted, the output of the user-supplied amplifier (for example, AD820 or OP196) is applied to the SMB output, VOUT. When Link 1 and Link 2 are inserted, Link 6 should be removed to connect the noninverting op amp input in series with the AD5933 output pin. • When Link 1 is removed, the output of the user-supplied amplifier is no longer applied to the SMB output, VOUT. When Link 1 and Link 2 are removed, Link 6 should be inserted to connect the AD5933 output pin directly to the VOUT SMB connector.
LK2	This link option is used to connect the output excitation signal from Pin 6 (VOUT) of the AD5933 to the noninverting terminal of the user-supplied operational amplifier. This link is used in conjunction with Link 1 and Link 6. When Link 1 and Link 2 are inserted, Link 6 should be removed and vice versa. • When Link 2 (LK2) is inserted, the output of the AD5933 excitation voltage pin (Pin 6) is applied to the noninverting terminal (Pin 3 of U1) of the user-supplied operational amplifier. • When Link 2 is removed, the output of the AD5933 excitation voltage pin (Pin 6) is no longer applied to the noninverting terminal (Pin 3 of U1) of the user-supplied operational amplifier, but is routed directly to the SMB VOUT if Link 6 (LK6) is inserted.
LK3	The AD5933 can have an external clock signal applied to Pin 8 (MCLK) or can be clocked internally using the internal RC oscillator. A high performance, 16 MHz, surface-mount crystal is supplied with the evaluation board (Y2). However, the user can provide an alternative clock signal by applying a system clock signal through the CLK1 SMB connector. To do this, remove Link 12 (LK12) and insert Link 3 (LK3). As a result, the clock signal applied at CLK1 will be connected to the clock pin (MCLK).

Link No.	Function
LK4	The internal reference circuitry section of the AD5933 can be powered through Terminal Block J4-1 (AVDD-REF) or, alternatively, from the on-board reference (U4). The J4-1 terminal block can be connected to a user-supplied external voltage source or, alternatively, the on-board high performance voltage reference, ADR423 (U4), can act as the voltage supply to the AVDD2 pin of the AD5933. Ensure that Link 4 is removed if Terminal Block J4-1 is powered with an external power supply. • When Link 4 is inserted, the output of the ADR423 regulator (U4) is connected to the analog voltage supply pin of the AD5933 (Pin 11). • When Link 4 is removed, the output of the ADR423 regulator (U4) is disconnected from the analog voltage supply pin of the AD5933 (Pin 11). In this case, the AVDD-REF pin must have an external supply voltage applied to J4-1 to power the internal reference circuitry of the part. Therefore, the user can either derive the AD5933 AVDD2 supply from the on-board reference or supply an external voltage through Terminal Block J4-1 (AVDD-REF).
LK5	The analog circuitry section of the AD5933 can be powered through Terminal Block J5-1 (AVDD-SIG) or, alternatively, from the on-board reference (U4). The terminal block (J5-1) can be connected to a user-supplied external voltage source or, alternatively, the on-board high performance voltage reference, ADR423 (U4), can act as the voltage supply to the AVDD1 pin of the AD5933. Ensure that Link 5 is removed if the Terminal Block J5-1 is powered with an external power supply. • When Link 5 is inserted, the output of the ADR423 regulator (U4) is connected to the analog voltage supply pin of the AD5933 (Pin 10). • When Link 5 is removed, the output of the ADR423 regulator (U4) is disconnected from the analog voltage supply pin of the AD5933 (Pin 10). In this case, the VDD-SIG pin must have an external supply voltage applied to J5-1 to power the analog circuitry of the part. Therefore, the user can either derive the AD5933 AVDD1 supply from the on-board reference or supply an external voltage through Terminal Block J5-1 (AVDD-SIG).
LK6	This link is used in conjunction with Link 1 and Link 2. The output excitation voltage can be directly applied to the VOUT SMB connector by inserting Link 6 and removing both Link 1 and Link 2. The AD5933 output excitation voltage can be postamplified by routing the signal through a noninverting amplifier (user supplied), which is accomplished by removing Link 6 and inserting Link 1 and Link 2. • When link 6 is inserted, the output of AD5933 is connected directly to the VOUT SMB connector. When this link is inserted, Link 1 and Link 2 must be removed. • When Link 6 is removed, the output of the AD5933 is not connected directly to the VOUT SMB connector; therefore, Link 1 and Link 2 must be inserted to complete the signal path. This is assuming that the user has inserted an operational amplifier (user supplied).
LK7	This link is used to connect the VIN SMB connector to the inverting terminal of the transimpedance amplifier within the AD5933. This link is required to complete the signal path and should be inserted while running a sweep. • When Link 7 is inserted, the impedance being tested is connected to the inverting terminal of the transimpedance amplifier in the AD5933. Link 7 must be inserted for a successful sweep to complete the signal path. • When Link 7 is removed, the signal path is incomplete, preventing a successful sweep.
LK8	This link is an applications sweep test link and is used in conjunction with Link 9. • When this link is inserted, one end of a 15 pF capacitor is connected to the VIN pin of the AD5933. • This link should be removed when running a normal sweep with an impedance connected across the VOUT and VIN SMB connectors.
LK9	This link is an applications sweep test link and is used in conjunction with Link 8. • When this link is inserted, one end of a 15 pF capacitor is connected across the VOUT pin of the AD5933. • This link should be removed when running a normal sweep with an impedance connected across the VOUT and VIN SMB connectors.
LK10	The digital circuitry section of the AD5933 can be powered through Terminal Block J2-1 (DVDD-5V) or, alternatively, from the output of the on-board reference (ADR423, U4). The terminal block must be connected to a user-supplied external voltage source (and Link 10 must be removed) or, alternatively, the on-board high performance voltage reference, ADR423, can act as the voltage supply to the DVDD pin of the AD5933. • When Link 10 is inserted, the output of the ADR423 regulator (U4) is connected to the digital voltage supply pin of the AD5933 (Pin 9). • When Link 10 is removed, the output of the ADR423 regulator (U4) is disconnected from the analog voltage supply pin of the AD5933 (Pin 9). In this case, the DVDD-5V pin must have an external supply voltage applied to J2-1 to power the digital circuitry of the part. Therefore, the user can either derive the AD5933 digital supply from the on-board reference or supply an external voltage through Terminal Block J2-1 (DVDD-5V).

Link No.	Function
LK11	The on-board voltage reference ADR423 (U4) can be supplied with an external supply voltage at Terminal Block J6-1. Alternatively, the input voltage can be supplied to the reference by the 5 V available through the USB connector (J1). By inserting LK11, LK5, LK4, and LK10, the AD5933 is completely powered from the USB supply; however, it is recommended to power the three supply pins of the part from an external precision voltage source for best results.
LK12	This link is used to connect the high performance 16 MHz crystal oscillator (Y2) to Pin 8 (MCLK) of the AD5933. • When Link 12 (LK12) is inserted and Link 3 (LK3) is removed, the on-board crystal oscillator is connected to the MCLK pin. • When Link 12 (LK12) is removed, Link 3 (LK3) should be inserted and an external clock should be applied to the CLK1 SMB connector.

SMB JUMPER FUNCTIONS

Table 3. SMB Jumper Function Descriptions

SMB	Function
CLK 1	The user can apply an external clock signal to Pin 8 (MCLK) of the AD5933, use the supplied external 16 MHz crystal oscillator (Y2), or use the internal 16.776 MHz oscillator to clock the AD5933 system. When Link 3 is inserted and Link 12 is removed, the external clock signal applied at the CLK1 SMB connector is connected to Pin 8 (MCLK). Alternatively, if Link 3 is removed and Link 12 is inserted, the on-board high performance 16 MHz surface-mount crystal can be used to clock the system. If the internal 16.776 MHz oscillator is used, the clock signal applied at MCLK is isolated by an internal multiplexer.
CLK 2	This link is for test purposes only.
VOUT	The user connects one end of the impedance being analyzed ($Z_{UNKNOWN}$) to this connector and the other end across the VIN SMB connector. The signal present at this connector can either be the excitation voltage output from Pin 6 of the AD5933 or an amplified version, depending on the status of LK1, LK2, and LK6, assuming the presence of a user-supplied external op amp at U1 (see Figure 1).
VIN	This connector takes the response signal current from across the impedance being analyzed ($Z_{UNKNOWN}$), which is connected between the VIN and VOUT SMB connectors, and provides a path back to the input pin (VIN, Pin 5). Link 7 must be inserted for the path to be complete. The external feedback resistor (RFB) has one point connected to this signal path, as shown in the board schematic (see the Evaluation Board Schematic section) and Figure 2.

LINK SETUP CONDITIONS

Table 4. Default Link Positions (Refer to Figure 2)

Link	Position	Function
LK1, LK2	Removed	External Amplifier U1 (optional) connected to VOUT is disconnected. AD5933 VOUT is directly connected to the SMB connector VOUT.
LK3	Removed	Used in conjunction with Link 12 (LK12). Optional user-supplied clock signal at CLK1 is not connected to Pin 8 (MCLK).
LK4	Inserted	AVDD1 is supplied from the ADR423 reference output.
LK5	Inserted	AVDD2 is supplied from the ADR423 reference output.
LK6	Inserted	Connects the output pin of the AD5933, VOUT, to the VOUT SMB connector.
LK7	Inserted	Connects the input pin of the AD5933, VIN, to the VIN SMB connector.
LK8, LK9	Inserted	Connects a 15 pF capacitor across the input and output pins of the AD5933. These links are for board manufacturing test purposes only and should be removed when completing a sweep with impedance $Z_{UNKNOWN}$ connected between the SMB connectors, VOUT and VIN.
LK10	Inserted	DVDD is supplied from the ADR423 reference output.
LK11	Inserted	Connects the 5.0 V supplied from the USB hub of the user PC to the supply input (VDD, Pin 2 of U4) of the on-board ADR423 reference.
LK12	Inserted	Connects the output of the on-board 16 MHz oscillator to Pin 8 (MCLK) of the AD5933.

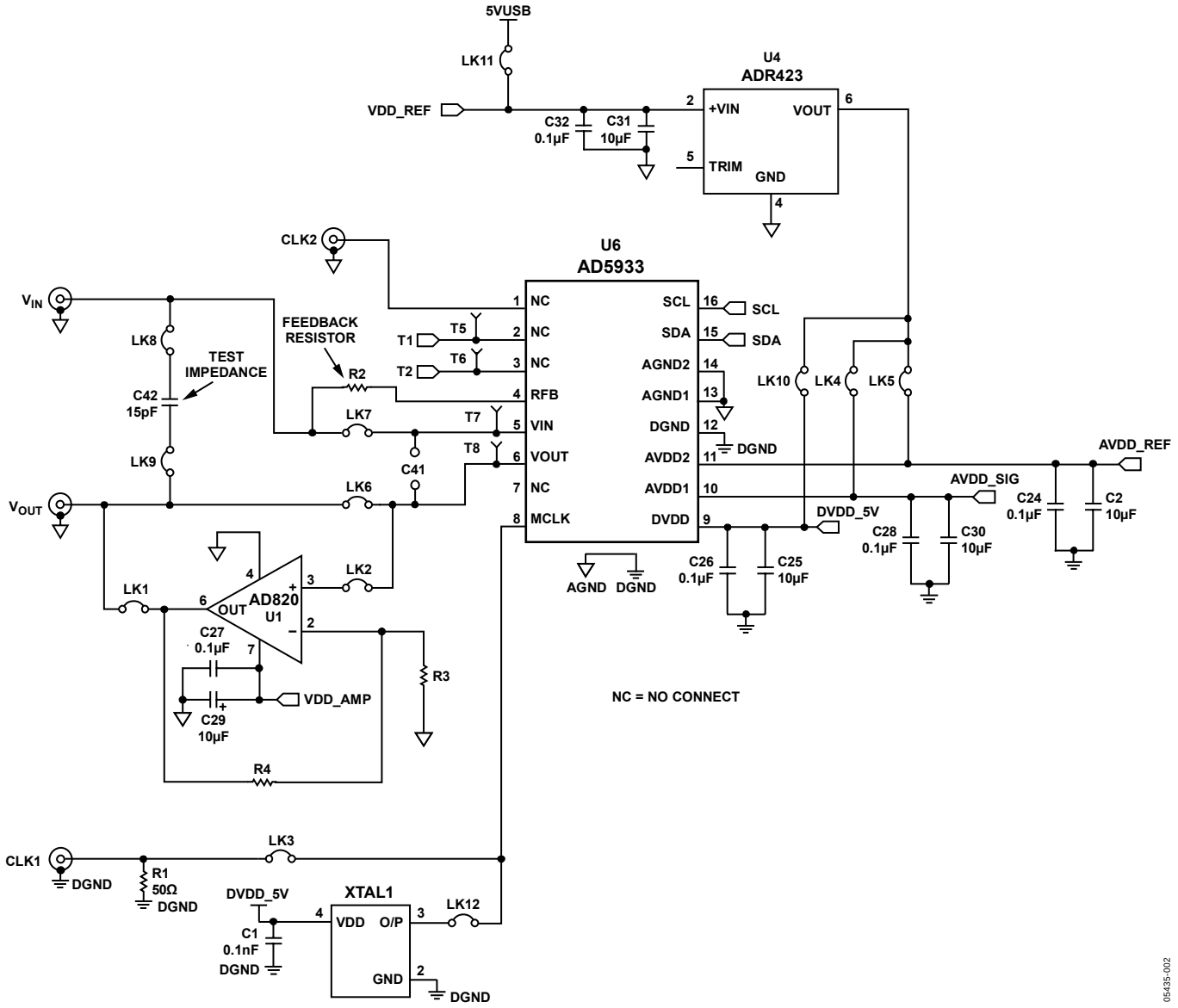


Figure 2. Setup Link Position Circuit (A 15 pF Capacitor Connected Between VIN and VOUT, with RFB = 200 kΩ and a Precision 16 MHz Connected to MCLK)

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

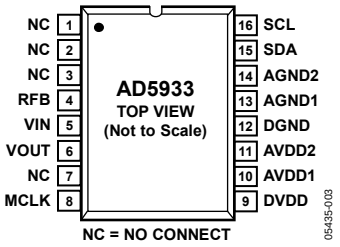


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions[1, 2]

Pin No.	Mnemonic	Description/Comment
1, 2, 3, 7	NC	No Connect.
4	RFB	External Feedback Resistor. Connected from Pin 4 to Pin 5 and used to set the gain of the current-to-voltage amplifier on the receive side.
5	VIN	Input to Receive Transimpedance Amplifier. Presents a virtual earth voltage of VDD/2.
6	VOUT	Excitation Voltage Signal Output.
8	MCLK	Master Clock for the System (User Supplied).
9	DVDD	Digital Supply Voltage.
10	AVDD1	Analog Supply Voltage 1.
11	AVDD2	Analog Supply Voltage 2.
12	DGND	Digital Ground.
13	AGND1	Analog Ground 1.
14	AGND2	Analog Ground 2.
15	SDA	I^2C Data Input. Open-drain pins requiring 10 kΩ pull-up resistors to VDD.
16	SCL	I^2C Clock Input. Open-drain pins requiring 10 kΩ pull-up resistors to VDD.

[1] It is recommended to tie all supply connections (Pin 9, Pin 10, and Pin 11) together and to run the device from a single supply between 2.7 V and 5.5 V.
[2] It is recommended to connect all ground signals (Pin 12, Pin 13, and Pin 14) together.

GETTING STARTED

SETUP SEQUENCE SUMMARY

This installation was carried out using the Windows® XP operating system with English (United States) settings. The regional and language settings of the computer can be changed in the **Regional and Language Options** directory within the control panel (**Start> Control Panel > Regional and Language Options**). The installation consists of the following steps, which are described in more detail in the sections that follow.

1. Install the AD5933 graphical user interface software on the compact disc (CD) that accompanies the evaluation board. Do not connect the USB cable from the AD5933 evaluation board to the computer USB hub until the evaluation software is properly installed. See the Step 1—Install the Software section.
2. Connect the computer USB port to the evaluation board using the USB cable provided in the evaluation kit, and run the USB hardware installation wizard after the evaluation software is installed correctly (the hardware installation may happen automatically, depending on the current operating system settings). See the Step 2—Connect the USB Cable section.
3. Ensure that the appropriate links are made throughout the evaluation board. Power up the evaluation board appropriately prior to opening and running the evaluation software program. See the Step 3—Verify the Links and Power Up section.
4. Configure the main dialog box of the evaluation board software to run the required sweep function. See the Step 4—Perform a Frequency Sweep section.

STEP 1—INSTALL THE SOFTWARE

Place the CD accompanying the evaluation board into the CD drive of your computer and click the **My Computer** icon on the desktop. Double-click the **compact disc drive** icon. Go to **AD5933 Installation** > **Setup.exe** (see Figure 4).

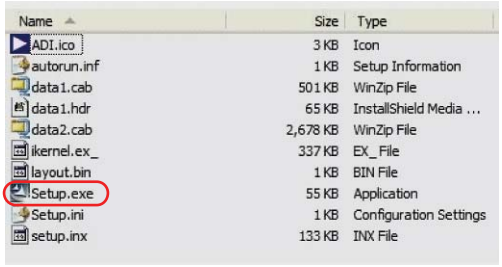


Figure 4. Evaluation Software CD Contents

Double-click **Setup.exe** and install the software onto the hard drive of your computer through the installation wizard (see Figure 5). It is recommended to install the software in the default destination folder path, **c\Program Files\Analog Devices\AD5933** (see Figure 6).

The CD software installation may happen automatically after the software CD is inserted into the disc drive, depending on the current operating system settings.

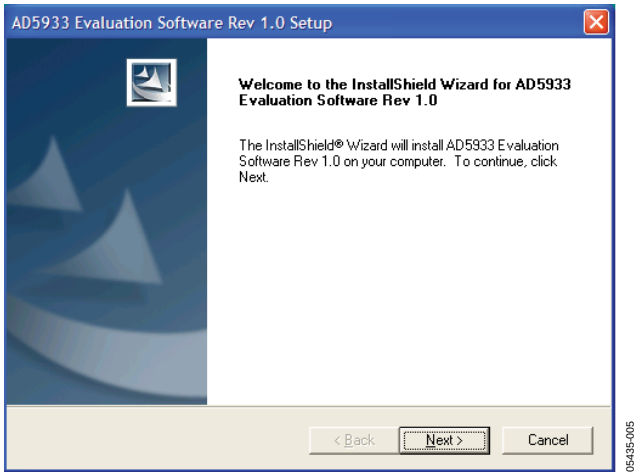


Figure 5. Installation Wizard

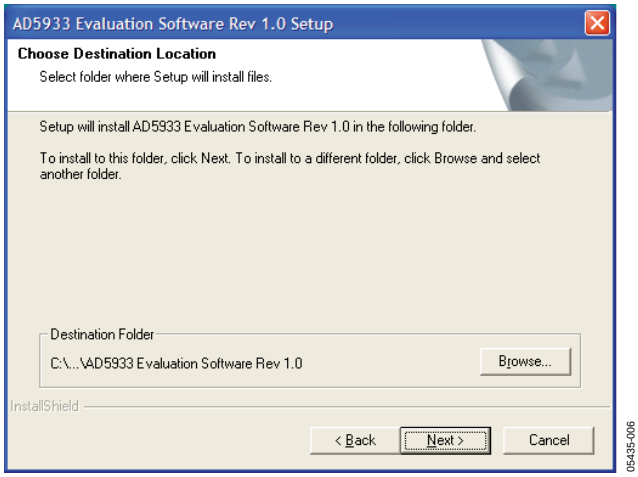


Figure 6. Recommended Path to Install the Setup.exe Software

Choose the **Analog Devices** directory (see Figure 7). If the Analog Devices folder does not exist yet, create a folder called Analog Devices and add the program icon to this new folder.

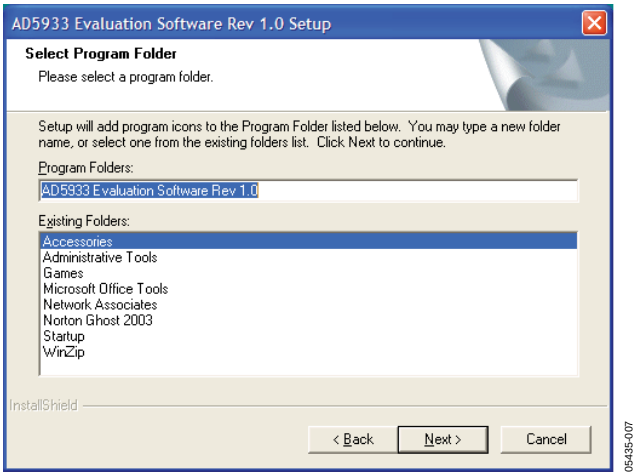


Figure 7. Evaluation Software Installation

After installing the software, remove the CD from the disc drive. You may be asked to reboot the computer.

Go to **Start** > **All Programs** > **Analog Devices** > **AD5933** > **AD5933** (see Figure 8).

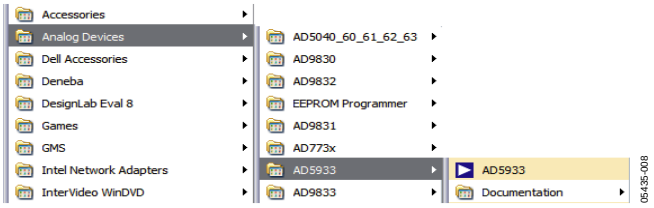


Figure 8. Opening the Evaluation Software

The message shown in Figure 9 will appear. This error message is to be expected because there is no USB connection between the computer and the AD5933 evaluation board at this stage. Therefore, the firmware code that the evaluation software operates from, and which needs to be downloaded to the evaluation board USB microcontroller memory each time the interface software program is opened, cannot be successfully downloaded to the evaluation board. Click **Cancel** and proceed to Step 2.

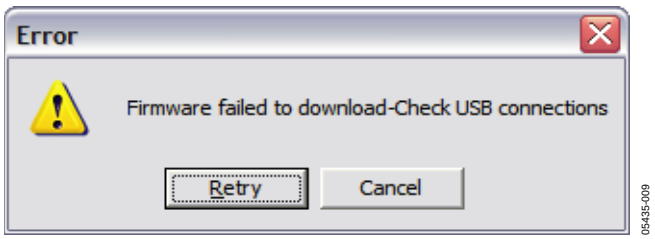


Figure 9. Expected Error Message

STEP 2—CONNECT THE USB CABLE

Plug one end of the USB cable into the computer USB hub and connect the other end to the AD5933 evaluation board USB socket (see J1 in Figure 37). A message may appear informing you that a USB device has been detected on the host computer and that new hardware has been found (see Figure 10).

Figure 10. USB Device Detected by Host Computer

The **Found New Hardware Wizard** dialog box appears (see Figure 11). This wizard locates and installs the appropriate driver files for the AD5933 evaluation kit in the operating system registry. Select the **Install the software automatically (Recommended)** option in the main dialog box of the software (see Figure 11). Click **Next** to continue.

Figure 11. Hardware Installation Wizard

A standard Windows operating system warning message appears, as shown in Figure 12. This indicates that the new hardware (the AD5933 evaluation kit) being installed on the Windows operating system has not passed the Windows logo testing to verify compatibility with Windows XP. This warning appears because the installation is an evaluation setup installation and is not intended to be used in a production environment. Click **Continue Anyway** and then click **Finish**.

Figure 12. Expected Warning Message

After the hardware has been successfully installed, the **Found New Hardware** message, stating that your new hardware is installed and ready to use, appears, as shown in Figure 13.

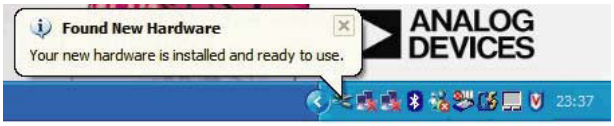


Figure 13. Successful Hardware Installation

STEP 3—VERIFY THE LINKS AND POWER UP THE EVALUATION BOARD

Ensure that the relevant links are in place on the evaluation board (see Table 2 and Table 4) and that the proper power connections and supply values are made to the terminal blocks before applying power to the evaluation board.

The power supply terminal blocks are outlined in Table 1. Note that the USB connector will supply power only to the Cypress USB controller chip that interfaces to the AD5933. It does not act as a supply source to the AD5933 if LK4, LK5, LK10, LK11, and LK12 are removed.

The user can provide a dedicated external voltage supply to each terminal block, if required. The user must ensure that all relevant power supply connections and links are made before running the evaluation software.

For optimum performance, it is recommended that the user supply the three supply signals (AVDD1, AVDD2, and DVDD) from a stable external reference supply via the power supply terminal blocks on the board as outlined in Table 1.

STEP 4—PERFORM A FREQUENCY SWEEP

The sequence for performing a linear frequency sweep across a 200 kΩ resistive impedance connected across the VOUT and VIN pins within the frequency range of 30 kHz to 30.2 kHz is outlined in this section. The default software settings for the evaluation board are shown in Figure 14 (note that a 200 kΩ resistor must be connected across the VIN and VOUT pins of the AD5933). The default link positions are outlined in Table 4 and should be reviewed before continuing with Step 4.

The sequence for opening the software is to go to **Start** > **Programs** > **Analog Devices** > **AD5933** and then click **AD5933 Evaluation Software**.

When the graphic user interface program is open and runs successfully, the dialog box shown in Figure 14 appears. The figure shows the interface panel along with a frequency sweep impedance profile for a 200 kΩ resistive impedance (note that RFB = 200 kΩ).

This section describes how to set up a typical sweep across a 200 kΩ impedance (when RFB = 200 kΩ) using the installed AD5933 software. The theory of operation and the internal system architecture of the AD5933 device are described in detail in the AD5933 data sheet. This is available at www.analog.com and should be consulted when using the evaluation board.

Set the start frequency to 30000 Hz in the **Start Frequency (Hz)** box (see Arrow 1A). The start frequency is 24-bit accurate.

Set the frequency sweep step size to 2 (Hz) in the **Delta Frequency** box (see Arrow 1A). The frequency step size is also 24-bit accurate.

To set the number of increments along the sweep to 200, type **200** into the **Number Increments (9 Bit)** box (see Arrow 1A). The maximum number of increments that the device can sweep across is 511. The value entered is stored in a register as a 9-bit value.

The delay between the time that a frequency increment takes place on the output of the internal DDS core and the time that the ADC samples the response signal at this new frequency is determined by the contents of the **Number of Settling Time Cycles** registers (0x8Ah and 0x8Bh). See the AD5933 data sheet for further details on the settling time cycle register.

For example, if the user programs a value of 15 into the **Number of Settling Time Cycles** box in the main dialog box and the next output frequency is 32 kHz, the delay between the time that the DDS core starts to output the 32 kHz signal and the time that the ADC samples the response signal is 15 × (1/32 kHz) ≈ 468.7 µs. The maximum **Number of Settling Time Cycles** that can be programmed to the board is 511 cycles. The value is stored in a register as a 9-bit value. This value can be further multiplied by a factor of 2 or 4.

Type **15** (cycles) into the **Number of Settling Time Cycles** box (see Arrow 1A). If you are sweeping across a high-Q structure, such as a resonant impedance, it is your responsibility to ensure that the contents of the settling time cycles register are sufficient for the impedance being tested to settle before incrementing between each successive frequency in the programmed sweep. This is achieved by increasing the value within the **Number of Settling Time Cycles** box.

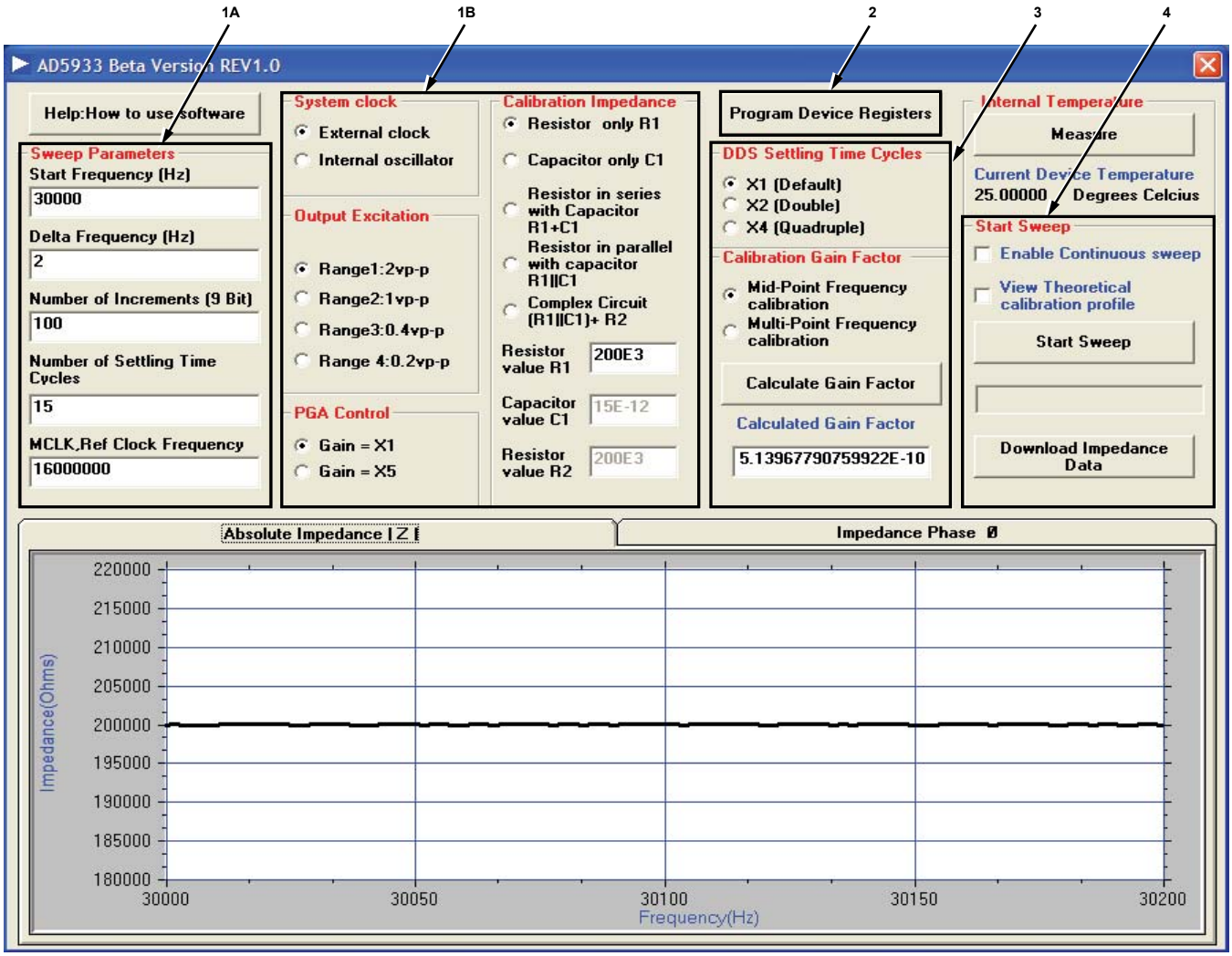


Figure 14. AD5933 Evaluation Software Main Dialog Box (The Impedance Profile of a 200 kΩ Resistor Is Displayed.)

Choose the external oscillator as the system clock. Select **External Clock** in the **System clock** section of the front panel (see Arrow 1B).

Set the output excitation voltage range of the AD5933 at Pin 6 (VOUT) to 2 V p-p (see Arrow 1B). The four possible output ranges available are 2 V p-p, 1 V p-p, 0.4 V p-p, and 0.2 V p-p typically.

In the **PGA Control** section, select the **Gain = ×1** option to set the gain on the receive stage (see Arrow 1B).

Refer to the **Calibration Impedance** box (see Arrow 1B). Prior to making any measurements, calibrate the AD5933 with a known (that is, accurately measured) calibration impedance connected between the VIN and VOUT pins of the AD5933. The choice of calibration impedance topology (for example, R1 in series with C1, R1 in parallel with C1, etc.) depends on the application in question. However, you must ensure that each component of the measured calibration impedance is entered correctly into each chosen topology component text box (see Arrow 1B). For example, in Figure 14 the **Resistor only R1** option is selected to measure the impedance of a 200 kΩ resistive impedance across frequency. For this example, type **200E3** (Ω) into the **Resistor Value R1** box.

To program the sweep parameters as chosen above into the appropriate on-board registers of the AD5933 through the I^2C interface, click **Program Device Registers** (see Arrow 2).

The value programmed into the **Number of Settling Time Cycles** box can be set so that the settling time is multiplied by a factor of 2 or 4 for a sweep (Arrow 3A). Select the **×1 (Default)** option.

Now that the frequency sweep parameters and gain settings are programmed, the next step is to calibrate the AD5933 system by calculating the gain factor.

The gain factor, which is calculated once at system calibration, must be calibrated correctly for a particular impedance range before any subsequent impedance measurement is valid (refer to the AD5933 data sheet for a more detailed explanation of gain factor).

The evaluation software can evaluate either a single midpoint frequency gain factor or multipoint frequency gain factors (that is, a gain factor for each point in the programmed sweep); see Arrow 3. The midpoint gain factor is determined at the midpoint of the programmed sweep; the multipoint gain factors are determined at each point in the programmed frequency sweep. After you click **Calculate Gain Factor**, the software automatically calculates the gain factor(s) for the subsequent sweep.

Once the midpoint gain factor or the multipoint gain factors have been calculated, a message is returned to the main dialog box of the evaluation software (see Figure 15). The gain factor(s) returned to the evaluation software are subsequently used for the sweep across the impedance being tested.

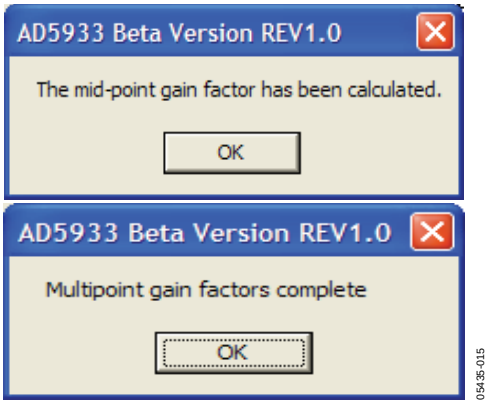


Figure 15. Confirmation of a Midpoint Gain Factor Calculation or a Multipoint Gain Factors Calculation

After the system interface software calculates the gain factor(s) for the programmed sweep parameters, this value appears in the **Calculated Gain Factor** section in the main dialog box of the evaluation software.

However, it is important to note that if you change any of the system gain settings (for example, if you change the output excitation range, PGA gain, etc.) after the system has been calibrated (that is, after the gain factor(s) have been calculated), it is necessary to recalculate the gain factor(s) in order to subsequently obtain accurate impedance measurement results. The gain factor(s) calculated in software are not programmed into the AD5933 RAM and are only valid when the evaluation software program is open and running. The gain factor(s) are not retained in the evaluation software after the software program is closed.

To begin the sweep, click **Start Sweep** (see Arrow 4). Once the evaluation software completes the sweep, it automatically returns both a plot of impedance vs. frequency and a plot of phase vs. frequency for the impedance being tested (see Figure 14). The progress of the sweep is outlined with a progress bar, as shown in Figure 16.

Figure 16. Sweep Progress Bar (Blue)

To take a reading from the on-board temperature sensor, click **Measure** in the **Internal Temperature** box of the main dialog box. This returns the 13-bit temperature of the device. See the AD5933 data sheet for more information on the temperature sensor.

To download the frequency sweep data (that is, frequency, impedance, phase, real, imaginary, and magnitude data) from the DFT of the sweep, click **Download Impedance Data**. The common dialog box shown in Figure 17 now appears. Choose a file name in the directory of choice and click **Save** (see Figure 17). Note that the default is to save the file in a .csv format.

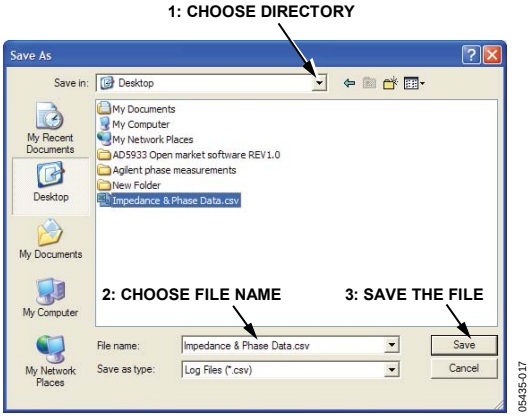
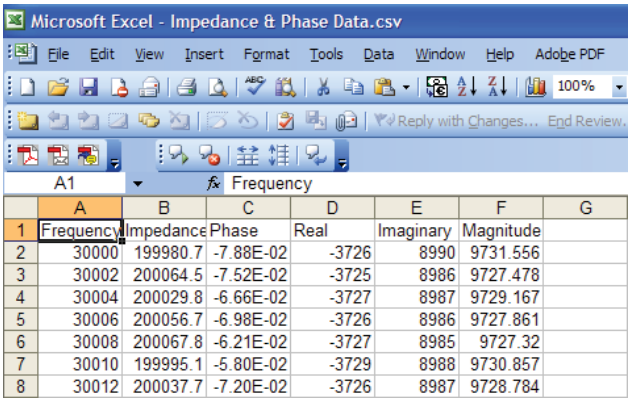


Figure 17. Saving the Sweep Data

This saves the sweep data as a comma separated variable file (.csv) located in the directory of your choice.

You can access this file content by using Notepad or Excel to plot the data. Each file contains a single column of data. The format of the downloaded data is shown in Figure 18



	A	B	C	D	E	F	G
1	Frequency	Impedance	Phase	Real	Imaginary	Magnitude	
2	30000	199980.7	-7.88E-02	-3726	8990	9731.556	
3	30002	200064.5	-7.52E-02	-3725	8986	9727.478	
4	30004	200029.8	-6.66E-02	-3727	8987	9729.167	
5	30006	200056.7	-6.98E-02	-3726	8986	9727.861	
6	30008	200067.8	-6.21E-02	-3727	8985	9727.32	
7	30010	199995.1	-5.80E-02	-3729	8988	9730.857	
8	30012	200037.7	-7.20E-02	-3726	8987	9728.784	

Figure 18. Opening the Sweep Data in Excel

Each data entry corresponds to a single measurement (frequency) point. Therefore, if you program 511 points as the value for the number of increments, the array contains a single column of data with 512 data points, starting at the start frequency value and ending at the stop frequency value. The stop frequency value is determined by

Start Frequency + (*Number of Increments* × *Delta Frequency*)

Graphs of the impedance profile vs. frequency and the phase profile vs. frequency appear in the main dialog box of the evaluation software after the sweep has completed. The user can switch between the impedance (|Z|) profile and phase (Ø) profile by clicking the corresponding tabs. The **Absolute Impedance |Z|** tab shows how the impedance being analyzed ($Z_{UNKNOWN}$) varies across the programmed frequency range. To view how the phase varies across the network being analyzed, click the **Impedance Phase Ø** tab (see Figure 19).

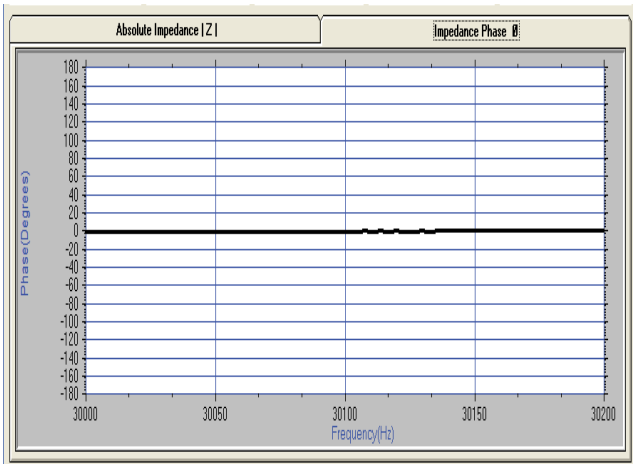


*Figure 19. The **Impedance Phase Ø** Tab on the Main Dialog Box (the Phase of a 200 kΩ Resistor (0°) Is Displayed)*

Note that the phase measured by the AD5933 takes into account the phase introduced through the *entire* signal path, that is, the phase introduced through the output amplifiers, the receive I-V amplifier, the low-pass filter, etc., along with the phase through the impedance (ZØ) being analyzed, which is connected between VOUT and VIN (Pin 6 and Pin 5 of the AD5933). The phase of the system must be calibrated using a resistor before any subsequent impedance phase (ZØ) measurement can be calculated. You need to perform the calibration with a resistor in the evaluation software in order to calibrate the system phase correctly. Refer to the Impedance Measurement Tips section for more details.

FREQUENTLY ASKED QUESTIONS ABOUT INSTALLATION

Q: How can I confirm that the hardware has been installed correctly in my computer?

A: Right-click **My Computer** and then left-click **Properties**. On the **Hardware** tab, click **Device Manager**.

Figure 20. System Properties

Scroll to **Universal Serial Bus controllers** and expand the directory root (see Figure 21). Figure 21 indicates what to expect when the AD5933 evaluation board is installed correctly and the evaluation board and USB cable are connected correctly to the computer. The root directory is refreshed after the USB cable is unplugged from the evaluation board, and then the AD5933 evaluation kit icon is removed from the main root.

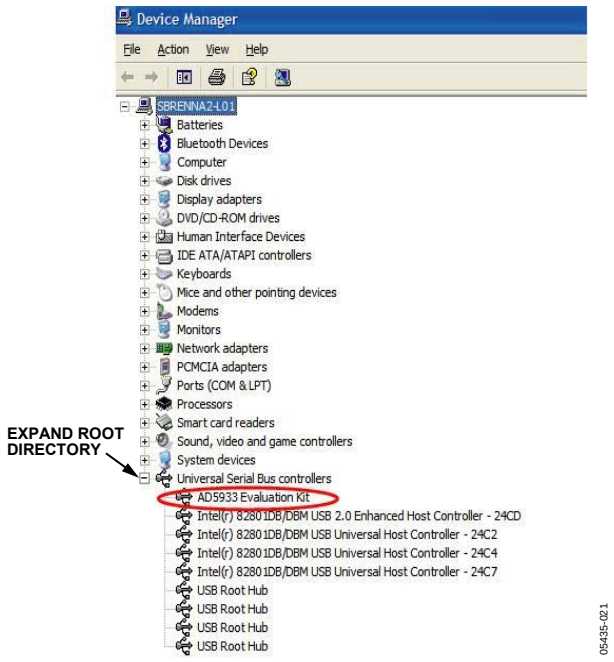


Figure 21. Correctly Installed Hardware

Q: When I plug in my board for the first time during the installation process, the message shown in Figure 22 appears. Then, when I click **Finish**, the message shown in Figure 23 appears. What should I do next?

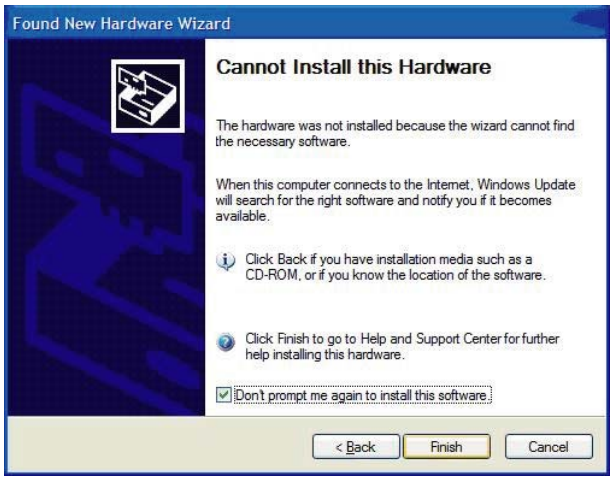


Figure 22. Error During the Hardware Installation

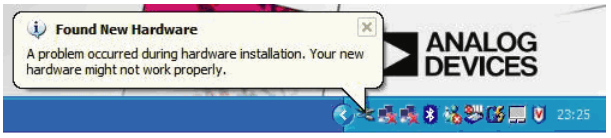


Figure 23. Error During the Hardware Installation

A: The computer has not recognized the USB device, that is, the AD5933 evaluation board that is plugged in. Assuming that the evaluation software is installed correctly (you should have installed the software correctly prior to plugging in the board for the first time), this message simply indicates that the AD5933 device drivers have not been installed to the correct registry and therefore cannot be correctly located by the install wizard.

To reinstall the device drivers, right-click **My Computer** and then left-click **Properties**. On the **Hardware** tab, choose **Device Manager**. Expand **Other devices** (see Figure 24). Right-click **USB Device** and then left-click **Uninstall Driver**. Unplug the evaluation board and wait approximately 30 seconds before plugging it in again. Proceed through the installation wizard a second time. A correct installation should be indicated by the expanded root directory in Figure 25.

If you encounter the same error message, uninstall both the device driver and the software and Contact the Analog Devices Technical Support Center for further instructions regarding valid driver files.

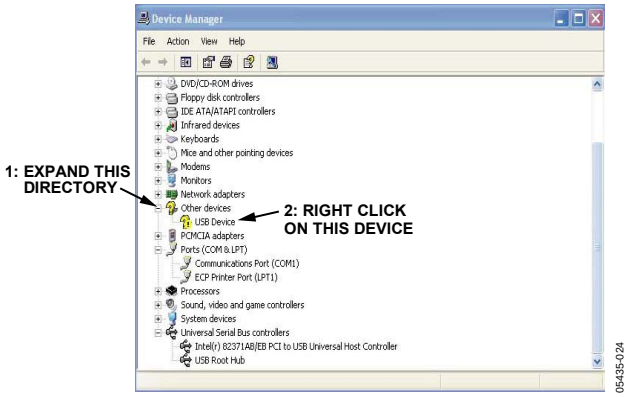


Figure 24. Device Manager

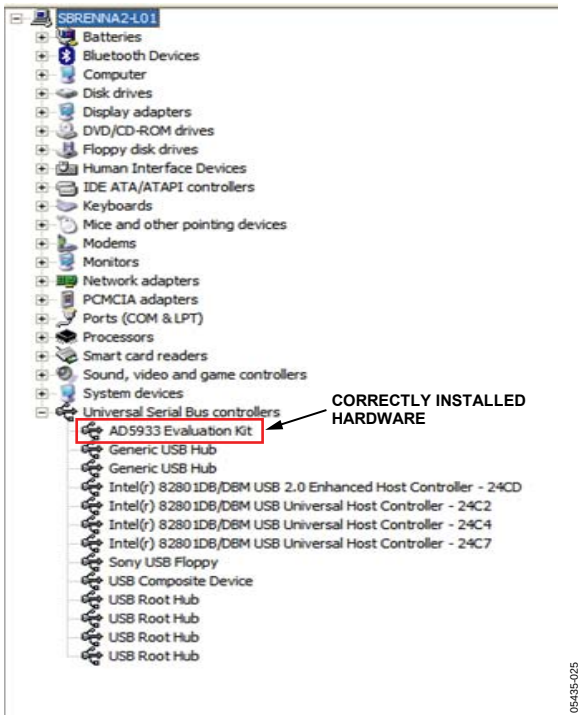


Figure 25. Correctly Installed Hardware

SOURCE CODE FOR IMPEDANCE SWEEPS

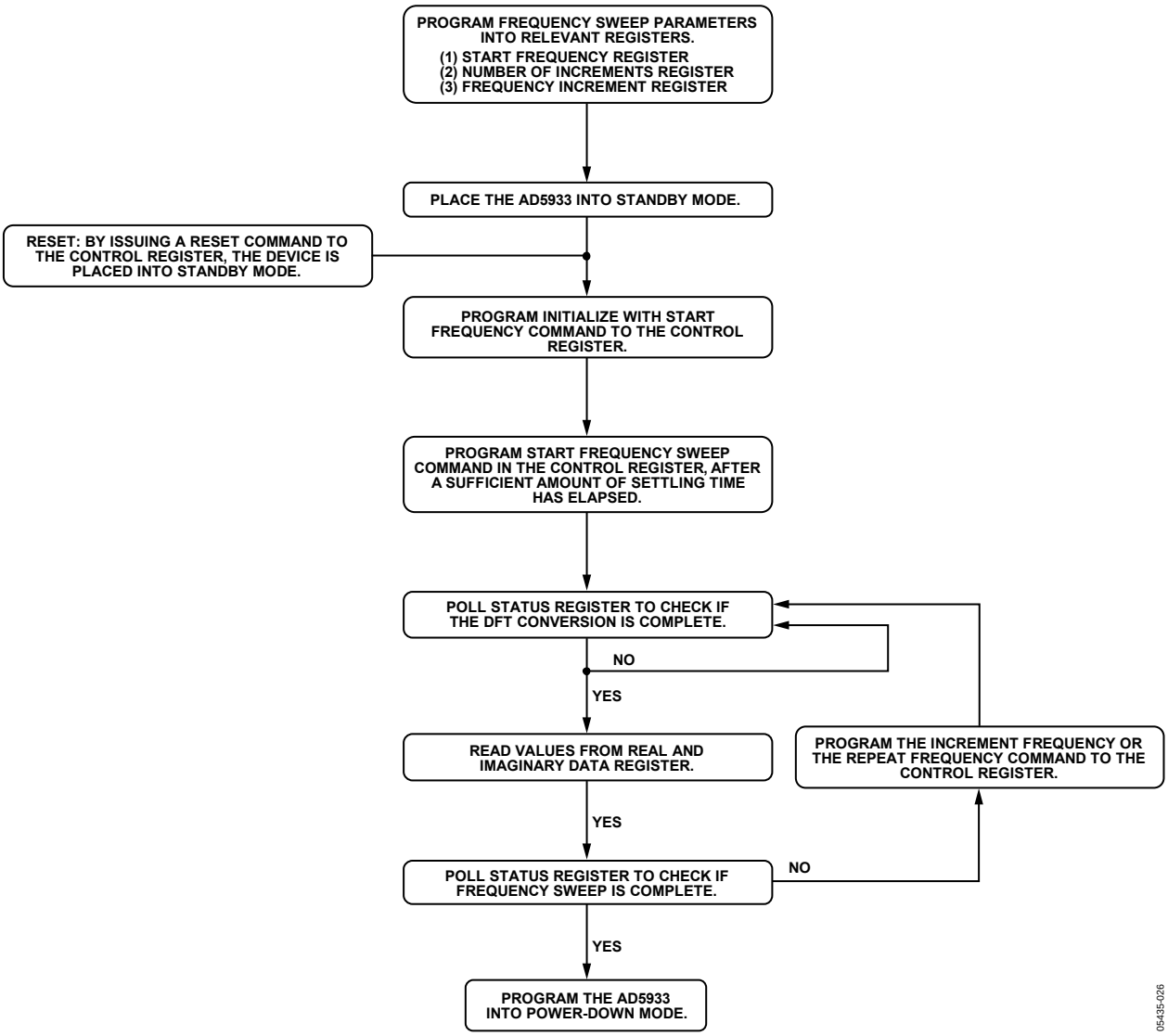


Figure 26. Sweep Flowchart

This section outlines the evaluation board code structure required to set up the AD5933 frequency sweep. The sweep flow outline is shown in Figure 26. Each section of the flowchart will be explained with the help of Visual Basic code extracts. The evaluation board source code (Visual Basic) is available upon request from the Analog Devices Technical Support Center. The firmware code (C code), which is downloaded to the USB microcontroller connected to the AD5933, implements the low level I^2C signal control (that is, read and write vendor requests).

The Evaluation Board Source Code Extract section provides an example of how to program a single frequency sweep, starting at 30 KHz, with a frequency step of 10 Hz and 150 points in the sweep. The code assumes that a 16 MHz clock signal is connected to Pin 8 (the MCLK pin) of the AD5933. The impedance range being tested is from 90 kΩ to 110 kΩ. The gain factor is calculated at the midpoint of the frequency sweep, that is, 30.750 kHz. The calibration is carried out with a 100 kΩ resistor connected between VOUT and VIN. The feedback resistor is 100 kΩ.

The first step in Figure 26 is to program the three sweep parameters that are necessary to define the frequency sweep (that is, the start frequency, the frequency increment, and the number of frequency increments in the sweep). Refer to the AD5933 data sheet for more details.

EVALUATION BOARD SOURCE CODE EXTRACT

```
‘-------------------------------------------------------------------------------------------------------
‘Code developed using visual basic® 6.
‘Datatype   range
‘Byte       0-255
‘Double     -1.797e308 to – 4.94e-324 and 4.94e-324 to 1.7976e308
‘Integer    -32,768 to 32767
‘Long       -2,147,483,648 to 2,147,483,647
‘Variant‘...when storing numbers same range as double. When storing strings same range as string.
‘------------------------------------ Variable Declarations -----------------------------------------
Dim ReadbackStatusRegister As Long   'stores the contents of the status register.
Dim RealData As Double               'used to store the 16 bit 2s complement real data.
Dim RealDataUpper As Long            'used to store the upper byte of the real data.
Dim RealDataLower As Long            'used to store the lower byte of the real data.
Dim ImagineryData As Double          'used to store the 16 bit 2s complement real data.
Dim ImagineryDataLower As Long       'used to store the upper byte of the imaginary data.
Dim ImagineryDataUpper As Long       'used to store the lower byte of the imaginary data.
Dim Magnitude As Double              'used to store the sqrt (real^2+imaginary^2).
Dim Impedance As Double              'used to store the calculated impedance.
Dim MaxMagnitude As Double           'used to store the max impedance for the y axis plot.
Dim MinMagnitude As Double           'used to store the min impedance for the y axis plot.
Dim sweep_phase As Double            'used to temporarily store the phase of each sweep point.
Dim Frequency As Double              'used to temporarily store the current sweep frequency.
Dim Increment As Long                'used as a temporary counter
Dim i As Integer                     'used as a temporary counter in (max/min) mag,phase loop
Dim xy As Variant                    'used in the stripx profile
Dim varray As Variant
Dim Gainfactor as double            ‘either a single mid point calibration or an array of calibration points
Dim TempStartFrequency     As Double
Dim StartFrequencybyte0    As Long
Dim StartFrequencybyte2    As Long
Dim StartFrequencybyte1A   As Long
Dim StartFrequencybyte1B   As Long
Dim DDSRefClockFrequency   As Double
Dim NumberIncrementsbyte0  As Long
Dim NumberIncrementsbyte1  As Long
Dim FrequencyIncrementbyt0 As Long
Dim FrequencyIncrementbyt1 As Long
Dim FrequencyIncrementbyt2 As Long
Dim SettlingTimebyte0      As Long
Dim SettlingTimebyte1      As Long
‘------------------------------------ I^2C read/write definitions-----------------------------------------
‘used in the main sweep routine to read and write to AD5933.This is the vendor request routines in the
firmware

Private Sub WritetToPart(RegisterAddress As Long, RegisterData As Long)
PortWrite &HD, RegisterAddress, RegisterData
‘parameters = device address register address register data
End Sub

Public Function PortWrite(DeviceAddress As Long, AddrPtr As Long, DataOut As Long) As Integer
PortWrite = VendorRequest(VRSMBus, DeviceAddress, CLng(256 * DataOut + AddrPtr), VRWRITE, 0, 0)
End Function

Public Function PortRead(DeviceAddress As Long, AddrPtr As Long) As Integer
PortRead = VendorRequest(VRSMBus, DeviceAddress, AddrPtr, VRREAD, 1, DataBuffer(0))
PortRead = DataBuffer(0)
End Function

‘------------------------------------ PHASE CONVERSION FUNCTION DEFINITION -------------------------------
‘This function accepts the real and imaginary data(R, I) at each measurement sweep point and converts it to
a degree
‘-------------------------------------------------------------------------------------------------------
Public Function phase_sweep (ByVal img As Double, ByVal real As Double) As Double

Dim theta As Double
  Dim pi As Double
  pi = 3.141592654

  If ((real > 0) And (img > 0)) Then
     theta = Atn(img / real)             ' theta = arctan (imaginary part/real part)
```

```
     phase2 = (theta * 180) / pi               'convert from radians to degrees

ElseIf ((real > 0) And (img < 0)) Then
      theta = Atn(img / real)                  '4th quadrant theta = minus angle
      phase2 = ((theta * 180) / pi ) +360

ElseIf ((real < 0) And (img < 0)) Then
      theta = -pi + Atn(img / real)            '3rd quadrant theta img/real is positive
      phase2 = (theta * 180) / pi

ElseIf ((real < 0) And (img > 0)) Then
      theta = pi + Atn(img / real)             '2nd quadrant img/real is neg
      phase2 = (theta * 180) / pi

End If

End Function
‘-------------------------------------------------------------------------------------------------------

Private Sub Sweep ()
’ the main sweep routine

‘This routine coordinates a frequency sweep using a mid point gain factor (see datasheet).
'The gain factor at the mid-point is determined from the real and imaginary contents returned at this mid
‘point frequency and the calibration impedance.
'The bits of the status register are polled to determine when valid data is available and when the sweep is
‘complete.
'-------------------------------------------------------------------------------------------------------
IndexArray = 0                   'initialize counter variable.
Increment = NumberIncrements + 1 'number of increments in the sweep.
Frequency = StartFrequency       'the sweep starts from here.

‘------------------------ PROGRAM 30K Hz to the START FREQUENCY register --------------------------------

DDSRefClockFrequency = 16E6               ‘Assuming a 16M Hz clock connected to MCLK
StartFrequency = 30E3                     ‘frequency sweep starts at 30K Hz

TempStartFrequency = (StartFrequency / (DDSRefClockFrequency / 4)) * 2^27 ‘dial up code for the DDS
TempStartFrequency = Int(TempStartFrequency)  ‘30K Hz = 0F5C28 hex

StartFrequencybyte0 = 40     ‘40 DECIMAL = 28 HEX
StartFrequencybyte1 = 92     ‘92 DECIMAL = 5C HEX
StartFrequencybyte2 = 15     ’15 DECIMAL = 0F HEX

'Write in data to Start frequency register
WritetToPart &H84, StartFrequencybyte0   '84 hex lsb
WritetToPart &H83, StartFrequencybyte1   '83 hex
WritetToPart &H82, StartFrequencybyte2   '82 hex
‘--------------------------------- PROGRAM the NUMBER OF INCREMENTS register -----------------------------
‘The sweep is going to have 150 points 150 DECIMAL = 96 hex
'Write in data to Number Increments register
WritetToPart &H89, 96     ‘lsb
WritetToPart &H88, 00     ‘msb
 ‘--------------------------------- PROGRAM the FREQUENCY INCREMENT register -----------------------------
‘The sweep is going to have a frequency increment of 10Hz between successive points in the sweep

DDSRefClockFrequency = 16E6               ‘Assuming a 16M Hz clock connected to MCLK
FrequencyIncrements = 10                 ‘frequency increment of 10Hz

TempStartFrequency = (FrequencyIncrements / (DDSRefClockFrequency / 4)) * 2^27 ‘dial up code for the DDS
TempStartFrequency = Int(TempStartFrequency)  ’10 Hz =  335 decimal = 00014F hex

FrequencyIncrementbyt0 = 4F     ‘335 decimal = 14f hex
FrequencyIncrementbyt1 = 01
FrequencyIncrementbyt2 = 00

'Write in data to frequency increment register
WritetToPart &H87, FrequencyIncrementbyt0   '87 hex lsb
WritetToPart &H86, FrequencyIncrementbyt1   '86 hex
WritetToPart &H85, FrequencyIncrementbyt2   '85 hex msb

 ‘--------------------------------- PROGRAM the SETTLING TIME CYCLES register -----------------------------
```

```
‘The DDS is going to output 15 cycles of the output excitation voltage before the ADC will start sampling
‘the response signal. The settling time cycle multiplier is set to x1

SettlingTimebyte0 = 0F ‘15 cycles (decimal) = 0F hex
SettlingTimebyte1 = 00 ’00 = X1

WritetToPart &H8B, SettlingTimebyte0
WritetToPart &H8A, SettlingTimebyte1


‘------------------------------------ PLACE AD5933 IN STANDBYMODE ---------------------------------------

‘Standby mode command = B0 hex
 WritetToPart &H80, &HB0

'------------------------ Program the system clock and output excitation range and PGA setting-----------
‘Enable external Oscillator
WritetToControlRegister2 &H81, &H8
‘Set the output excitation range to be 2vp-p and the PGA setting to = x1
WritetToControlRegister2 &H80, &H1

‘-----------------------------------------------------------------------------------------------------------
‘------------- ------------ Initialize impedance under test with start frequency --------------------------
'Initialize Sensor with Start Frequency
 WritetToControlRegister &H80, &H10

msDelay 2  'this is a user determined delay dependant upon the network under analysis (2ms delay)

‘------------------------------------ Start the frequency sweep ----------------------------------------
'Start Frequency Sweep
WritetToControlRegister &H80, &H20

'Enter Frequency Sweep Loop

ReadbackStatusRegister = PortRead(&HD, &H8F)
ReadbackStatusRegister = ReadbackStatusRegister And &H4 ' mask off bit D2 (i.e. is the sweep complete)

Do While ((ReadbackStatusRegister <> 4) And (Increment <> 0))
'check to see if current sweep point complete

ReadbackStatusRegister = PortRead(&HD, &H8F)
ReadbackStatusRegister = ReadbackStatusRegister And &H2
'mask off bit D1 (valid real and imaginary data available)
                ‘-------------------------------------------------------------------------
                If (ReadbackStatusRegister = 2) Then
                ' this sweep point has returned valid data so we can proceed with sweep
                Else
                Do
          ‘if valid data has not been returned then we need to pole stat reg until such time as valid data
          'has been returned
         ‘i.e. if point is not complete then Repeat sweep point and pole staus reg until valid data returned
                WritetToControlRegister &H80, &H40 'repeat sweep point
                       Do
                ReadbackStatusRegister = PortRead(&HD, &H8F)
                ReadbackStatusRegister = ReadbackStatusRegister And &H2
                ' mask off bit D1- Wait until dft complete
                       Loop While (ReadbackStatusRegister <> 2)

                Loop Until (ReadbackStatusRegister = 2)
                End If
                '-------------------------------------------------------------------------

                RealDataUpper = PortRead(&HD, &H94)
                RealDataLower = PortRead(&HD, &H95)
                RealData = RealDataLower + (RealDataUpper * 256)
                'The Real data is stored in a 16 bit 2's complement format.
                'In order to use this data it must be converted from 2's complement to decimal format
                If RealData <= &H7FFF Then  ' h7fff 32767
                ' Positive
                Else
                ' Negative
'                RealData = RealData And &H7FFF
```

```
                RealData = RealData - 65536
                End If
                ImagineryDataUpper = PortRead(&HD, &H96)
                ImagineryDataLower = PortRead(&HD, &H97)
                ImagineryData = ImagineryDataLower + (ImagineryDataUpper * 256)
                'The imaginary data is stored in a 16 bit 2's complement format.
                'In order to use this data it must be converted from 2's complement to decimal format
                If ImagineryData <= &H7FFF Then
                ' Positive Data.
                Else
                ' Negative
'                ImagineryData = ImagineryData And &H7FFF
                ImagineryData = ImagineryData - 65536
                End If

‘-----------------Calculate the Impedance and Phase of the data at this frequency sweep point -----------
                Magnitude = ((RealData ^ 2) + (ImagineryData ^ 2)) ^ 0.5
                'the next section calculates the phase of the dft real and imaginary components
                ‘phase_sweep calculates the phase of the sweep data.
                 sweep_phase = (phase_sweep(ImagineryData, RealData) - calibration_phase_mid_point)
                 GainFactor = xx ‘this is determined at calibration.see gain factor section and Datasheet.
                 Impedance = 1 / (Magnitude * GainFactor)

                ' Write Data to each global array.
                MagnitudeArray(IndexArray) = Impedance
                PhaseArray(IndexArray) = sweep_phase
                ImagineryDataArray(IndexArray) = ImagineryData
                code(IndexArray) = Magnitude
                RealDataArray(IndexArray) = RealData
                Increment = Increment - 1 ' increment was set to number of increments of sweep at the start
                FrequencyPoints(IndexArray) = Frequency
                Frequency = Frequency + FrequencyIncrements ' holds the current value of the sweep freq
                IndexArray = IndexArray + 1

              ------------- Check to see if sweep complete ----------------------
ReadbackStatusRegister = PortRead (&HD, &H8F)
ReadbackStatusRegister = ReadbackStatusRegister And &H4 ' mask off bit D2

'Increment to next frequency point Frequency
WritetToControlRegister &H80, &H30
Loop

‘--------------------- END OF SWEEP: Place device into POWERDOWN mode-----------------------------------
'Enter Powerdown Mode,Set Bits D15,D13 in Control Register.
WritetToPart &H80, &HA0

END SUB
‘-------------------------------------------------------------------------------------------------------


‘The programmed sweep is now complete and the impedance and phase data is available to read in the two
‘arrays MagnitudeArray() = Impedance and PhaseArray() = phase.


sweepErrorMsg:
                    MsgBox "Error completing sweep check values"
End Sub


‘The programmed sweep is now complete and the impedance and phase data is available to read in the two
‘arrays MagnitudeArray() = Impedance and PhaseArray() = phase.
```

GAIN FACTOR CALCULATION

The code in the Evaluation Board Source Code Extract section for the impedance sweep is based on a single-point gain factor calculation, which is determined at the midpoint sweep frequency with a known impedance connected between VOUT and VIN. The gain factor for this example is calculated by exciting the calibration impedance using a 2 V p-p sinusoid with a frequency of 30.750 kHz, a PGA setting of ×1, a 100 kΩ resistor connected between VOUT and VIN, and a feedback resistor of 100 kΩ. The magnitude of the real and imaginary components at the calibration frequency is given by the formula:

$$Magnitude = \sqrt{R^2 + I^2}$$

where R is the real component, and I is the imaginary component of the calibration code.

The gain factor is then given by

$$Gain\ Factor = \left(\frac{Admittance}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude} = \frac{\left(\frac{1}{100\ k\Omega}\right)}{Magnitude}$$

Refer to the AD5933 data sheet for more details.

TEMPERATURE MEASUREMENT

The temperature sensor data is stored in a 14-bit, twos complement format. For the conversion formula and more details on the temperature sensor, see the AD5933 data sheet.

```
Private Sub MeasureTemperature()
' The Digital temperature Result is stored over two registers as a 14 bit twos complement number.
' 92H <D15-D8> and 93H<D7 to D0>.
Dim TemperatureUpper As Long.
Dim TemperatureLower As Long
'Write xH90  to the control register to take temperature reading.
WritetToPart &H80, &H90
msDelay 5 'nominal delay
ReadbackStatusRegister = PortRead(&HD, &H8F)
ReadbackStatusRegister = ReadbackStatusRegister And &H1
'if a valid temperature conversion is complete, ignore this.
If ReadbackStatusRegister <> 1 Then
        'loop to wait for temperature measurement to complete.
         Do
   ReadbackStatusRegister = PortRead(&HD, &H8F)
   ReadbackStatusRegister = ReadbackStatusRegister And &H1
    Loop Until (ReadbackStatusRegister = 1)
        Form1.Label10.Caption = "Current Device Temperature"
        MsgBox "Device Temperature Measurement Complete"
End If

' The Digital temperature Result is stored over two registers as a 14 bit twos complement number.
' 92H <D15-D8> and 93H<D7 to D0>.
TemperatureUpper = PortRead(&HD, &H92)
TemperatureLower = PortRead(&HD, &H93)
Temperature = TemperatureLower + (TemperatureUpper * 256)
```

```
If Temperature <= &H1FFF Then ' msb =0.
' Positive Temperature.
Label8.Caption = (Temperature / 32#)
Else
' Negative Temperature.
Label8.Caption = (Temperature - 16384) / 32#
End If
're-assign variables used.
TemperatureUpper = 0
TemperatureLower = 0
Temperature = 0
End Sub
```

IMPEDANCE MEASUREMENT TIPS

This section outlines some of the workarounds for using the AD5933 to measure impedance profiles under certain conditions.

Calibrating the AD5933

When calculating the calibration term (that is, the gain factor; see the AD5933 data sheet for further details), it is important that the receive stage is operating in its linear region. This requires careful selection of the system gain settings. The system gain settings are

- Output excitation voltage range
- Current-to-voltage gain setting resistor
- PGA gain

The gain through the system shown in Figure 27 is given by

$$OutputExcitationVoltageRange \times \frac{GainSettingResistor}{Z_{UNKNOWN}} \times PGAGain$$

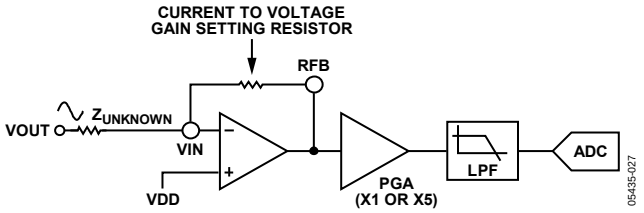


Figure 27. AD5933 System Voltage Gain

For example, assume the following system calibration settings:

VDD = 3.3 V
Gain setting resistor = 200 kΩ
$Z_{UNKNOWN}$ = 200 kΩ
PGA setting = ×1
Range 1 = 2 V p-p

The peak-to-peak voltage presented to the ADC input is 2 V p-p. However, if a programmable gain amplifier setting gain of ×5 is chosen, the voltage saturates the ADC, and, as a result, the calculated calibration term (that is, the gain factor) is inaccurate.

The gain factor should be calculated when the largest response signal is presented to the ADC while ensuring that the signal is maintained within the linear range of the ADC over the impedance range of interest. (The reference range of the ADC is the supply AVDD.)

Therefore, based on your knowledge of the unknown impedance span over the frequency range of interest, correctly configure the system gain settings (see Figure 27). These settings include the output excitation voltage range (Range 1, Range 2, Range 3, or Range 4), the current-to-voltage amplifier gain setting resistor, and the programmable gain amplifier setting (either ×1 or ×5) that precedes the ADC.

Select a calibration impedance value that is approximately halfway between the limits of the unknown impedance (therefore, the impedance limits must be known to correctly calibrate the system). Then, choose a value for the I-V gain setting resistor that is equal to the calibration impedance. This results in a unity gain condition on the receive side of the current-to-voltage amplifier.

For example, assume the following:

- The unknown test impedance limits are defined by

  $$180\ k\Omega \leq Z_{UNKNOWN} \leq 220\ k\Omega$$

- The frequency range of interest is 30 kHz and 32 kHz
- The following are the system calibration gain settings:
  VDD = 3.3 V
  Gain setting resistor (RFB) = 200 kΩ
  $Z_{CALIBRATION}$ = 200 kΩ
  PGA setting = ×1
  Calibration frequency = 31 kHz (midpoint frequency)

The gain factor calculated at the midpoint frequency of 31 kHz can be used to calculate any impedance in the 180 kΩ to 220 Ω range. If the unknown impedance span or the frequency sweep is too large, the accuracy of the calculated impedance measurement degrades. In addition, if any of the calibration system gain settings change, you must recalibrate the AD5933 and recalculate the gain factor (see the AD5933 data sheet for further details).

Measuring Small Impedances

The AD5933 is capable of measuring impedance values of up to 10 MΩ if the system gain settings are chosen correctly for the impedance subrange of interest. However, there are two points to understand when measuring small impedances with the AD5933.

First, if the user places a small impedance value (< ≈ 500 Ω over the sweep frequency of interest) between the VOUT and VIN pins, the signal current flowing through the impedance for a fixed excitation voltage increases in accordance with Ohm's law. The output stage of the transmit side amplifier that is available at the VOUT pin may not be able to provide the required increase in current through the impedance. In addition, to ensure a unity gain condition on the receive side I-V amplifier, there must be a similar small value of feedback resistance for system calibration, as outlined in the Calibrating the AD5933 section. The voltage presented at the VIN pin is hard biased at VDD/2 due to the virtual earth on the receive side I-V amplifier (see the AD5933 data sheet for further details). The increased current's sink/source requirement on the output of the receive side I-V amplifier may also cause the amplifier to operate outside of the linear region, resulting in significant errors in subsequent impedance measurements.

Second, the value of the output series resistance (R_{OUT} see Figure 28) at the VOUT pin of the AD5933 must be taken into account when measuring small impedances ($Z_{UNKNOWN}$), specifically when the value of the output series resistance is comparable to the value of the impedance being tested ($Z_{UNKNOWN}$). If the R_{OUT} value is unaccounted for in the system calibration (that is, the gain factor calculation) when measuring small impedances, an error will be introduced in subsequent impedance measurements. (The error introduced depends on the relative magnitude of the impedance being tested compared with the value of the output series resistance.)

The value of the output series resistance depends on the selected output excitation range at VOUT, and, like with all discrete resistors manufactured in a silicon fabrication process, the tolerance varies from device to device. Typical values of the output series resistance are listed in Table 6.

Table 6. Output Series Resistance (R_{OUT}) vs. Excitation Range

Parameter	Value (Typ)	Output Series Resistance Value (Typ)
Range 1	2 V p-p	200 Ω
Range 2	1 V p-p	2.4 kΩ
Range 3	0.4 V p-p	1.0 kΩ
Range 4	0.2 V p-p	600 Ω

Therefore, to accurately calibrate the AD5933 to measure small impedances, it is necessary to reduce the signal current by sufficiently attenuating the excitation voltage and to account for the output series resistance value (R_{OUT}) by factoring it into the gain factor calculation (see the AD5933 data sheet for further details).

During device characterization, measuring the output series resistance value (R_{OUT}) was achieved by selecting the appropriate output excitation range at VOUT and then sinking and sourcing a known current (for example, ±2 mA) at the pin and measuring the change in dc voltage. The output series resistance was calculated by measuring the inverse of the slope (that is, 1/slope) of the resultant I-V plot.

A circuit that helps to minimize the effects of the two previously described issues is shown in Figure 28. The aim of this circuit is to place the AD5933 system gain within its linear range when measuring small impedances by using an additional external amplifier circuit along the signal path. The external amplifier attenuates the peak-to-peak excitation voltage at VOUT if the user chooses suitable values for Resistors R1 and R2. This reduces the signal current flowing through the impedance and minimizing the effect of the output series resistance in the impedance calculations.

In the circuit shown in Figure 28, the impedance being tested ($Z_{UNKNOWN}$) sees the output series resistance of the external amplifier. This value is typically much less than 1 Ω with feedback applied, depending on the op amp device (for example, AD820, AD8641, or AD8531), the load current, the bandwidth, and the gain.

The key point is that the output impedance of the external amplifier in Figure 28, which is also in series with the impedance being tested ($Z_{UNKNOWN}$), has a far less significant

effect on the AD5933 calibration (that is, the gain factor calculation) and subsequent impedance readings in comparison with those obtained by connecting the small impedance directly to the VOUT pin (and directly in series with R_{OUT}). The external amplifier buffers the unknown impedance from the effects of the output series resistance of the AD5933 (R_{OUT}) and introduces a smaller output impedance in series with the impedance being tested ($Z_{UNKNOWN}$).

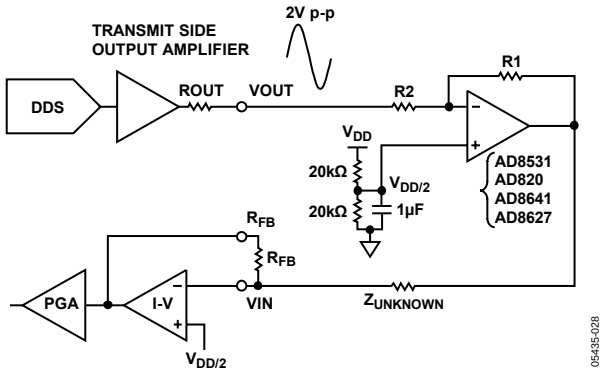


Figure 28. Additional External Amplifier Circuit for Measuring Small Impedances

For example, a user might want to measure an impedance, $Z_{UNKNOWN}$, that is known to have a value within the range of 90 Ω to 110 Ω (that is, a small impedance) over the frequency range of 30 kHz to 32 kHz. In this case, the user may not be able to characterize the output series resistance (R_{OUT}) directly in the factory/lab. Therefore, the user may choose to add an extra amplifier circuit as shown in Figure 28 to the signal path of the AD5933. The user must ensure that the chosen external amplifier has a sufficiently low output series resistance over the bandwidth of interest in comparison with the impedance range being tested (visit www.analog.com/opamps for an op amp selection guide). The data sheets of most Analog Devices amplifiers show the closed loop output impedance vs. frequency at different amplifier gains to provide an idea of the effect on output series impedance.

The system settings are as follows:

VDD = 3.3 V
VOUT = 2 V p-p
R2 = 20 kΩ
R1 = 4 kΩ
Gain setting resistor = 500 Ω
$Z_{UNKNOWN}$ = 100 Ω
PGA setting = ×1

Choose a ratio of R1/R2 to attenuate the excitation voltage at VOUT. With the values of R1 = 4 kΩ and R2 = 20 kΩ, the signal is attenuated by 1⁄5 (1/5 of 2 V p-p = 400 mV). The maximum current flowing through the impedance will be 400 mV/90 Ω = 4.4 mA.

The system is subsequently calibrated at a midpoint frequency in the sweep using the usual method with a midpoint impedance value of 100 Ω for the calibration resistor and feedback resistor. Increasing the value of the I-V gain resistor at the RFB pin improves the dynamic range of the input signal to the receive side of the AD5933. For example, by increasing the I-V gain setting resistor at the RFB pin, the peak-to-peak signal presented to the ADC input increases from 400 mV (Rfb = 100 Ω) to 2 V p-p (Rfb = 500 Ω).

The gain factor calculated is for a 100 Ω resistor connected between VOUT and VIN, assuming the output series resistance of the external amplifier is small enough to be ignored.

One final important point to note about the biasing of the circuit shown in Figure 28 is that the receive side of the AD5933 is hard biased about VDD/2 by design. Therefore, to prevent the output of the external amplifier (attenuated AD5933 range 1 excitation signal) from saturating the receive side amplifiers of the AD5933, a voltage equal to VDD/2 must be applied to the noninverting terminal of the external amplifier.

Measuring Lower Excitation Frequencies

The AD5933 has a flexible internal direct digital synthesizer (DDS) core and DAC, which together generate the excitation signal used to measure the impedance ($Z_{UNKNOWN}$). The DDS core has a 27-bit phase accumulator, allowing subhertz (<0.1 Hz) frequency resolution. The output of the phase accumulator is connected to the input of a read only memory (ROM). The digital output of the phase accumulator is used to address individual memory locations in the ROM. The digital contents of the ROM represent amplitude samples of a single cycle of a sinusoidal excitation waveform. The content of each address within the ROM look-up table are in turn passed to the input of a digital-to-analog converter (DAC) that produces the analog excitation waveform made available at the VOUT pin. The DDS core (that is, the phase accumulator and the ROM look-up table) and the DAC are referenced from a single system clock. The function of the phase accumulator is to act as a system clock divider.

The system clock for the AD5933 DDS engine can be provided in one of two ways.

- Use a highly accurate and stable clock (crystal oscillator) at the external clock pin (MCLK, Pin 8).
- Use the AD5933 internal clock oscillator with a typical frequency of 16.776 MHz. (The internal oscillator is not available in the AD5934; therefore, the user must apply a clock to the external clock pin (MCLK).)

Select the preferred system clock by programming Bit D3 in the CONTROL register (Address 81 hex; see AD5933 data sheet).

The system clock is also used by the internal ADC to digitize the response signal. The ADC requires 16 clock periods to perform a single conversion. Therefore, with a maximum

system clock frequency of 16.776 MHz, the ADC can sample the response signal with a frequency of 1.0485 MHz, that is, a throughput rate of ≈1.04 MSPS. The ADC converts 1024 samples and passes the digital results to the multiply accumulate (MAC) core for processing. The AD5933 MAC core performs a 1024-point DFT to determine the peak of the response signal at the ADC input. The DFT offers many advantages over conventional peak detection mechanisms, including excellent dc rejection as well as an averaging of errors and phase information.

The throughput rate of the AD5933 ADC scales with the system clock. Therefore, lower ADC throughput rates, and hence sampling frequencies, can be achieved by lowering the system clock.

The conventional DFT assumes a sequence of periodic input data samples in order to determine the spectral content of the original continuous signal. In the AD5933, these samples come from the 12-bit ADC for a user-defined range of signal frequencies. The conventional DFT correlates the input signal with a series of test phasor frequencies in order to determine the fundamental signal frequency and its harmonics. The frequency of the test phasor is at integer multiples of a fundamental frequency given by the following formula:

$$Test\ Phasor\ Frequency = \frac{f_S}{N}$$

where f_S is the sampling frequency of ADC, and N is the number of samples taken (1024).

The correlation is performed for each integer frequency. If the resulting correlation of the test phasor with the input sample set is nonzero, there is signal energy at this frequency. If no energy is found in a bin, there is no energy at that test frequency.

The DFT implemented by the AD5933 is called a single-point DFT, meaning that the analysis or correlation frequency in the MAC core is always at the same frequency as the current output excitation frequency. Therefore, when the system clock for the AD5933 is 16.776 MHz, the sample rate of the ADC is 1.04 MHz. The DSP core requires 1024 samples to perform the single-point DFT. Therefore, the resolution of the DFT is 1.04 MHz/1024 points ≈ 1 kHz. This calculation is based on a system clock frequency of 16 MHz applied at MCLK. If the AD5933 tries to examine excitation frequencies below ≈1 kHz, the errors introduced by spectral leakage become very significant and result in erroneous impedance readings.

If the input signal over the 1024-point sample interval is an integer, there will be a smooth transition from the end of one period to the beginning of the next point, as shown in Figure 29. If this number is not an integer, there will not be a smooth transition from the end of one period to the beginning of the next point, as shown in Figure 30. The leakage is a result of the discontinuities introduced by the DFT, assuming a periodic input signal like that shown in Figure 30.

In order for the AD5933 to analyze the impedance ($Z_{UNKNOWN}$) at frequencies lower than ≈1 kHz, it is necessary to scale the system clock so that the sample rate of the ADC is lower and causes the 1024 samples required for the single-point DFT to cover an integer number of periods of the current excitation frequency.

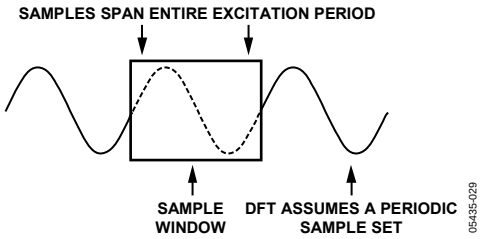


Figure 29. Sample Set Spanning the Entire Excitation Period

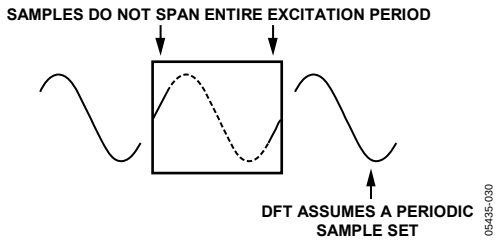


Figure 30. Sample Set not Spanning the Entire Excitation Period

Frequently Asked Questions About Measuring Lower Excitation Frequencies

Q: I want to analyze frequencies in the range between 1 kHz and 10 kHz using the AD5933 with a 16 MHz crystal. Will this work?

A: This is possible, but you will need to scale the system clock by using an external clock divider. This reduces the sampling frequency of the ADC to a value less than 1 MHz ($f_{SAMPLING}$ = MCLK/16); however, the 1024 sample set will now span the response signal being analyzed. Note that by scaling the system clock, you reduce the maximum bandwidth of the sweep.

You can use an additional low power DDS part, such as the AD9834 (see Figure 31), or an integer N divider, such as the ADF4001 (see Figure 32), to divide down a system clock signal before applying it to the external clock pin (MCLK) of the AD5933.

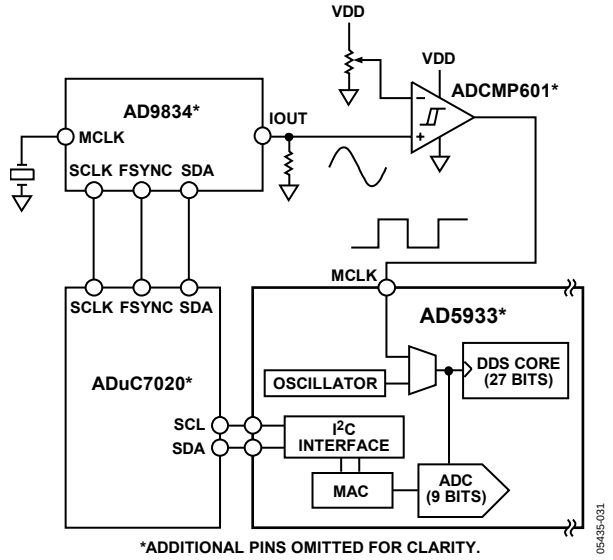


Figure 31. Using an External AD9834 to Scale the System Clock

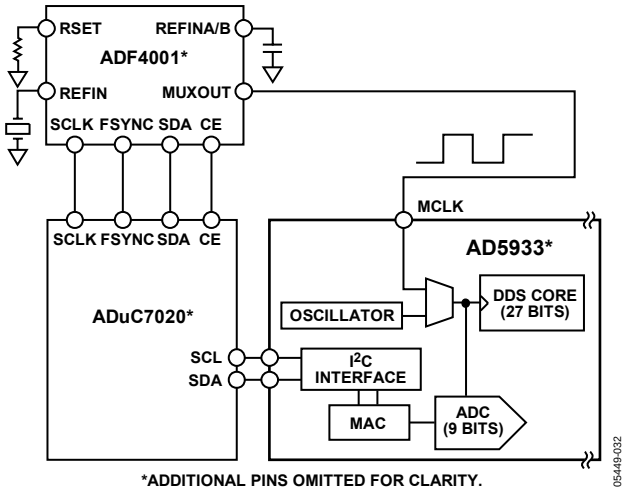


Figure 32. Using an External Integer Divider to Scale the System Clock

Q: I have scaled the system clock connected to the AD5933 to allow an analysis of lower clock frequencies. Although I established the lower frequency limit (see Table 7), my upper excitation frequency is now limited. What is the reason for this limitation?

Table 7. Experimental Lower Frequency Limits vs. MCLK

Frequency Interval	AD5933 Lower Frequency[1]	Clock Frequency Applied to MCLK Pin[2]
1	100 kHz to 5 kHz	16 MHz
2	5 kHz to 1 kHz	4 MHz
3	5 kHz to 300 Hz	2 MHz
4	300 Hz to 200 Hz	1 MHz
5	200 Hz to 100 Hz	250 kHz
6	100 Hz to 30 Hz	100 kHz
7	30 Hz to 20 Hz	50 kHz
8	20 Hz to 10 Hz	25 kHz

[1] The lower frequency sweep limit is established by applying the divided clock signal to the MCLK pin of the AD5933, and then calibrating and remeasuring a nominal impedance, $Z_{CALIBRATION}$, for example, a 200 kΩ resistor over a 500 Hz linear sweep from the programmed start frequency (I-V gain resistor setting = $Z_{CALIBRATION}$, for example, 200 kΩ, PGA = ×1, Δ frequency = 5 Hz, number of points = 100). The lower frequency limit is established as the frequency at which the DFT, and hence the impedance vs. frequency results, begins to degrade and deviate from the expected value of the measured impedance, $Z_{CALIBRATION}$, for example, 200 kΩ.

[2] TTL clock levels applied to the MCLK pin, with V_{IH} = 2 V and V_{IL} = 0.8 V.

A: In measuring lower clock frequencies, the two main tradeoffs are that the AD5933 takes longer to return the impedance results due to the slower ADC conversion clock speed and that the upper excitation limit is restricted.

For example, if the user has established that a scaled clock frequency of 4 MHz must be applied to the external clock pin of the AD5933 to correctly analyze a 3 kHz signal, the applied system clock (external or internal oscillator) is divided by a factor of 4 before being routed as the reference clock to the DDS. The system clock is directly connected to the ADC without further division so that the ADC sampling clock is running at four times the speed of the DDS core. Therefore, with a system clock of 4 MHz, the DDS reference clock is 1/4 × 4 MHz = 1 MHz, and the ADC clock is 4 MHz. The AD5933 DDS has a 27-bit phase accumulator; however, the top three most significant bits (MSBs) are internally connected to Logic 0. Therefore, with the top three MSBs set to 0, the maximum DDS output frequency is further reduced by a factor of 1/8, and the maximum output frequency is 1/32 × 1 MHz = 31.25 kHz.

Therefore, it is possible to accurately measure the 3 kHz signal using a lower system clock of 4 MHz; however, the AD5933 takes longer to return the impedance results due to the slower ADC conversion clock speed and the upper excitation limit is now restricted to 31.25 KHz.

Measuring Higher Excitation Frequencies

The AD5933 is specified to a typical system accuracy of 0.5% within the frequency range of 1 kHz up to 100 kHz (assuming the AD5933 system is calibrated correctly for the impedance range being tested).

The lower frequency limit is determined by the value of the system clock frequency connected to the external clock pin (MCLK) of the AD5933. The lower limit can be reduced by scaling the system clock (see Measuring Lower Excitation Frequencies).

The upper frequency limit of the system is due to the finite bandwidth of the internal amplifiers coupled with the effects of the low-pass filter pole locations (for example, 200 kHz and 300 kHz), which are used to roll off any noise signals from corrupting the DFT output on the receive side of the AD5933. Therefore, the AD5933 has a finite frequency response similar to that shown in Figure 33.

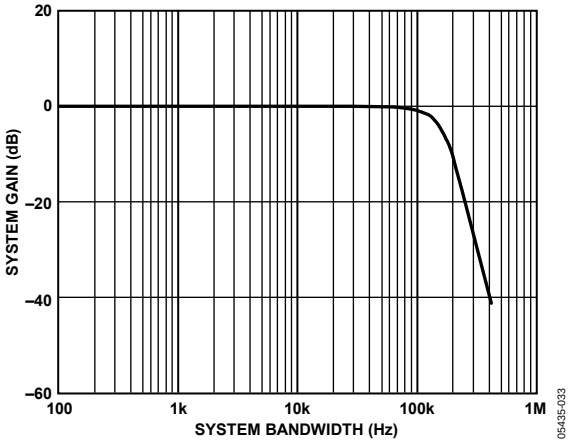


Figure 33. Typical AD5933 System Bandwidth

Using the AD5933 to analyze frequencies above 100 kHz introduces errors in the impedance profile if the sweep span is too large. This is due to the effect of the increased roll-off in the finite frequency response of the system for frequencies above 100 kHz. However, if the user is performing a sweep with a frequency above 100 kHz, it is important to ensure that the sweep range is as small as possible, for example, 120 kHz to 122 kHz. The impedance error from the calibration frequency is approximately linear over a small frequency range. The user can remove any linear errors introduced by performing an end-point or multipoint calibration (see the AD5933 data sheet for further details on end-point calibration).

Measuring the Phase Across an Impedance

The AD5933 returns a complex output code composed of separate real and imaginary components. The real component is stored at Register Addresses 94h and 95h, and the imaginary component is stored at Register Addresses 96h and 97h after each sweep measurement. These correspond to the real and imaginary components of the DFT, not to the resistive and reactive components of the impedance being tested.

For example, it is a common misconception to assume that if a customer is analyzing a series RC circuit, the real value stored in 94h and 95h and the imaginary value stored at 96h and 97h correspond to the resistance and capacitive reactance, respectfully. This is incorrect. However, the magnitude of the impedance (|Z|) can be determined by first calculating the magnitude of the real and imaginary components of the DFT by using the following formula:

$$Magnitude = \sqrt{R^2 + I^2}$$

Next multiply by the calibration term (see the Gain Factor Calculation section in the AD5933 data sheet) and invert the product gives the impedance. Therefore, the magnitude of the impedance is given by the following formula:

$$Impedance \ \ (|Z|) = \frac{1}{Gain \ \ Factor \ \times Magnitude}$$

The gain factor is given by the following formula:

$$Gain\ Factor = \left(\frac{Admittance}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude}$$

Before a valid measurement can occur, the user must calibrate the AD5933 system for a known impedance range to determine the gain factor. Therefore, the user of the AD5933 must know the impedance limits of the complex impedance ($Z_{UNKNOWN}$) for the sweep frequency range of interest. The gain factor is determined by placing a known impedance between the input and output of the AD5933, and then measuring the resulting magnitude of the code. The AD5933 system gain settings need to be chosen so that the excitation signal is in the linear region of the on-board ADC. (Refer to the data sheet for further details.)

Because the AD5933 returns a complex output code composed of real and imaginary components, the user can calculate the phase of the response signal through the AD5933 signal path. The phase is given by the following formula.

$$Phase\ (\text{rads}) = \tan^{-1}(I / R)$$

This equation accounts for the phase shift introduced in the DDS output signal as it passes through the internal amplifiers on the transmit and receive sides of the AD5933, the low-pass filter, and the impedance connected between the VOUT and VIN pins of the AD5933.

The parameters of interest for many users of the AD5933 are the magnitude of the impedance ($|Z_{UNKNOWN}|$) and the impedance phase (ZØ). The measurement of the impedance phase (ZØ) is a two-step process.

The first step involves calculating the AD5933 system phase. The AD5933 system phase can be calculated by placing a resistor across the VOUT and VIN pins of the AD5933, and then calculating the phase (using the formula above) after each measurement point in the sweep. By placing a resistor across the VOUT and VIN pins, there is no additional phase lead or lag introduced in the AD5933 signal path. Therefore, the resulting phase, that is, the system phase, is due entirely to the internal poles of the AD5933.

After the system phase is calibrated using a resistor, the phase of any unknown impedance can be calculated by inserting it between the VIN and VOUT terminals of the AD5933, and then recalculating the new phase (including the phase due to the impedance) by using the same formula. The phase of the unknown impedance (ZØ) is given by the following formula.

$$ZØ = (\Phi Unknown - \nabla System)$$

where:
∇ *System* is the phase of the system with a calibration resistor connected between VIN and VOUT.
Φ*Unknown* is the phase of the system with the unknown impedance connected between VIN and VOUT.
ZØ is the phase due to the impedance (impedance phase).

Note that it is possible to both calculate the gain factor and calibrate the system phase using the same real and imaginary component values when a resistor is connected between the VOUT and VIN pins of the AD5933.

Example of Measuring the Impedance Phase (ZØ) of a Capacitor

The excitation signal current leads the excitation signal voltage across a capacitor by −90°. Therefore, before any measurement is performed, one would intuitively expect to see approximately a −90° phase difference between the system phase response measured with a resistor and the system phase response measured with a capacitive impedance.

As outlined in the Measuring the Phase Across an Impedance section, if the user would like to determine the phase angle of a capacitive impedance (ZØ), the user must first determine the system phase response (∇ System), and then subtract this from the phase calculated with the capacitor connected between VOUT and VIN (ΦUnknown).

A plot showing the AD5933 system phase response calculated using a 220 kΩ calibration resistor (Rfb = 220 kΩ, PGA = ×1) and the repeated phase measurement with a 10 pF capacitive impedance is shown in Figure 34.

The phase difference (that is, ZØ) between the phase response of a capacitor and the system phase response using a resistor is the impedance phase (ZØ) of the capacitor and is shown in Figure 35.

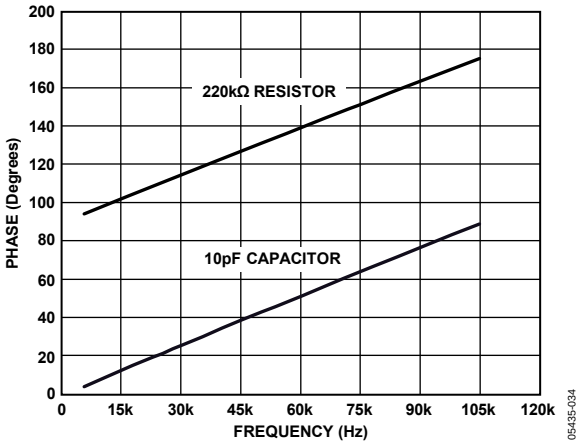


Figure 34. System Phase Response vs. Capacitive Phase

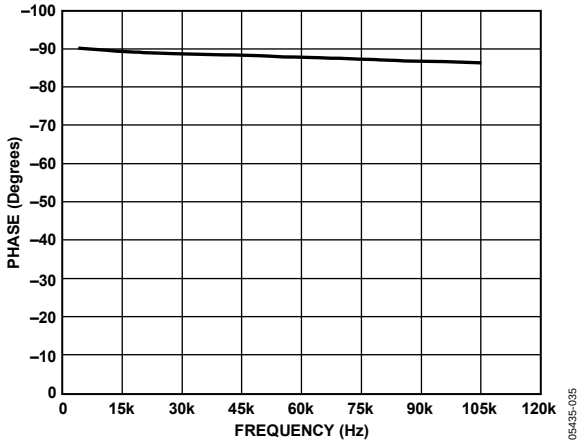


Figure 35. Phase Response of a Capacitor

It is important to note that the formula used to calculate the phase and to plot Figure 34 is based on the arctangent function, which returns a phase angle in radians. Therefore, it is necessary to convert the calculated phase angle from radians to degrees.

In addition, care must be taken with the arctangent formula when using the real and imaginary values to interpret the phase at each measurement point. The arctangent function returns the correct standard phase angle only if the sign of the real and imaginary values are positive, that is, if the coordinates lie in the first quadrant.

The standard angle is the angle taken counterclockwise from the positive real x-axis. If the sign of the real component is positive and the sign of the imaginary component is negative, that is, the data lies in the second quadrant, then the arctangent formula returns a negative angle, and it is necessary to add 180° to calculate the correct standard angle.

Likewise, when the real and imaginary components are both negative, that is, when the coordinates lie in the third quadrant, the arctangent formula returns a positive angle, and it is necessary to add 180° to the angle in order to determine the correct standard phase.

Finally, when the real component is positive and the imaginary component is negative, that is, the data lies in the fourth quadrant, then the arctangent formula returns a negative angle, and it is necessary to add 360° to the angle in order to calculate the correct phase angle.

Therefore, the correct standard phase angle is dependant on the sign of the real and imaginary components (see Table 8 for a summary).

Table 8. Phase Angle

Real	Imaginary	Quadrant	Phase Angle (Degrees)
Positive	Positive	First	$\tan^{-1}(I/R)\times\frac{180}{\pi}$
Positive	Negative	Second	$180+\left(\tan^{-1}(I/R)\times\frac{180}{\pi}\right)$
Negative	Negative	Third	$180+\left(\tan^{-1}(I/R)\times\frac{180}{\pi}\right)$
Positive	Negative	Fourth	$360+\left(\tan^{-1}(I/R)\times\frac{180}{\pi}\right)$

After the magnitude of the impedance (|Z|) and the impedance phase angle (ZØ, in radians) are correctly calculated, it is possible to determine the magnitude of the real (resistive) and imaginary (reactive) components of the impedance ($Z_{UNKNOWN}$). This is accomplished by the vector projection of the impedance magnitude onto the real and imaginary impedance axes using the following formulas:

$$|Z_{REAL}| = |Z| \times \cos(Z\text{Ø})$$

$$|Z_{IMAG}| = |Z| \times \sin(Z\text{Ø})$$

where Z_{REAL} is the real component, and Z_{IMAG} is the imaginary component.

EVALUATION BOARD SCHEMATIC

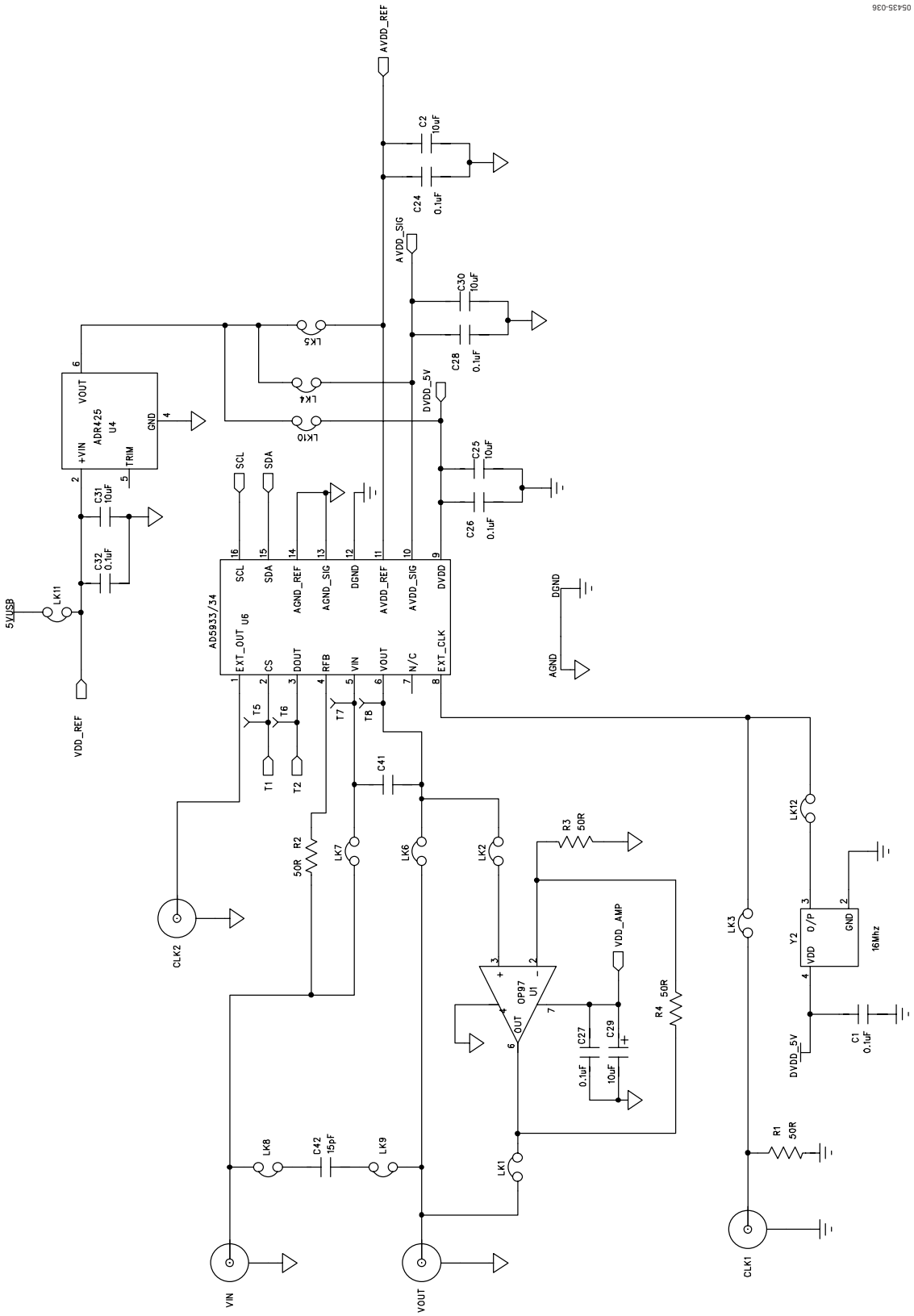


Figure 36. Schematic

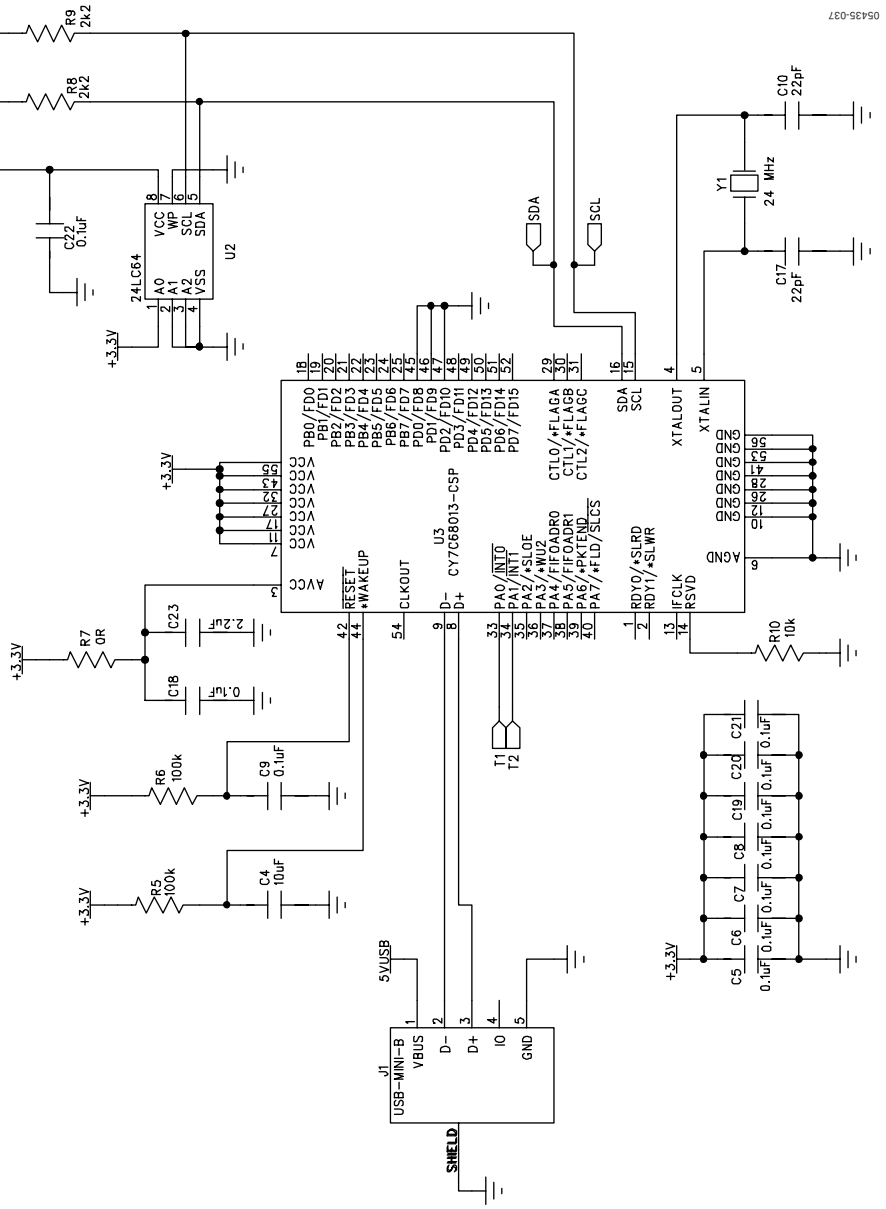


Figure 37. Schematic

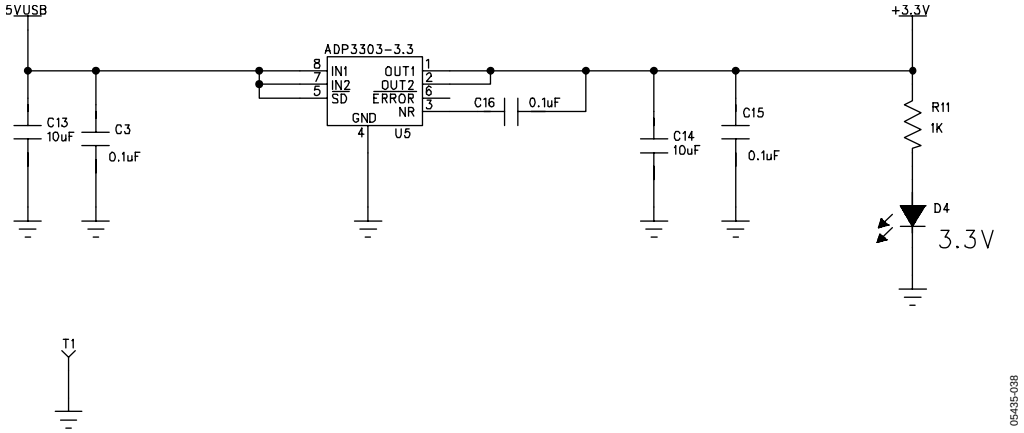


Figure 38.

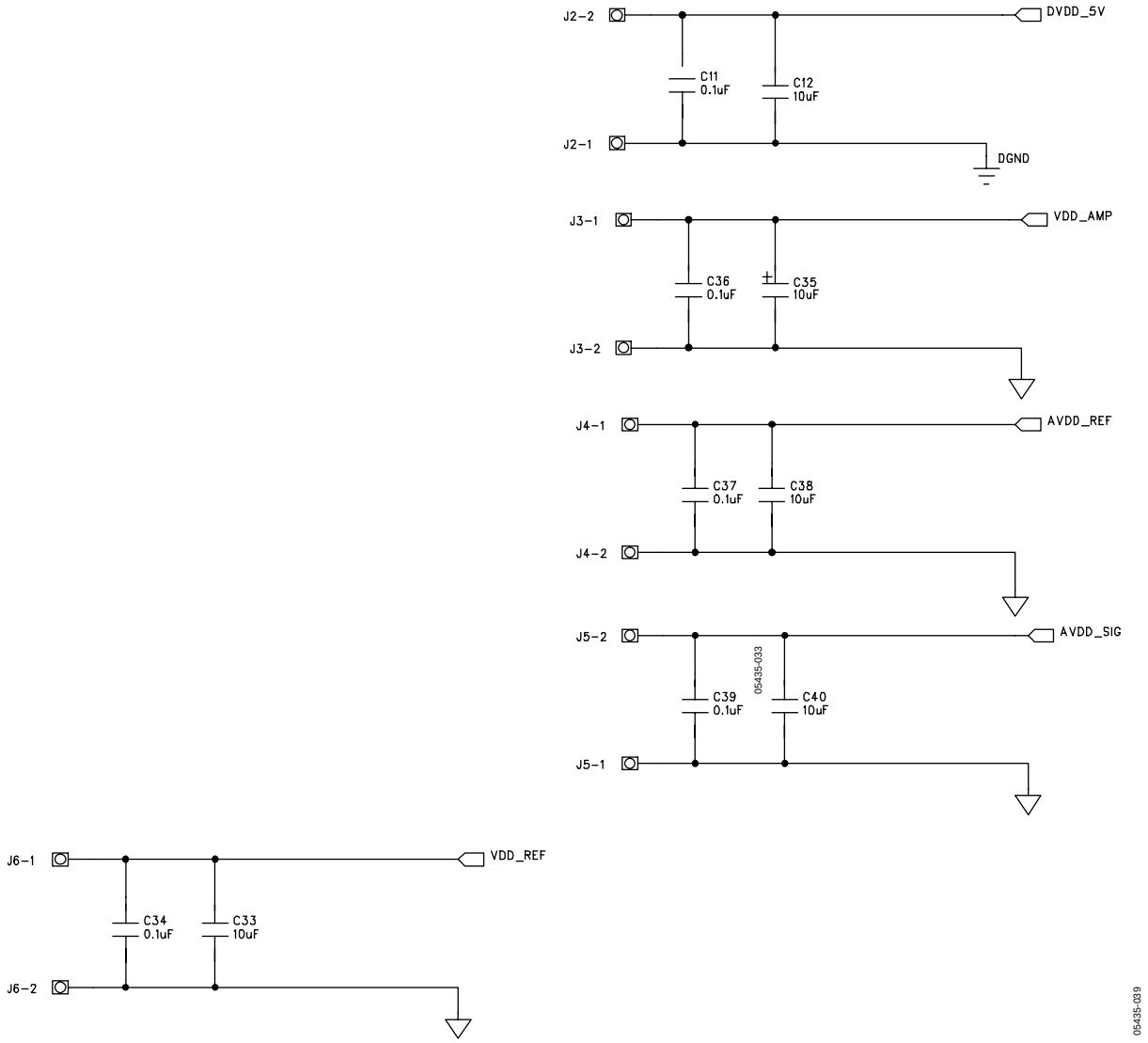


Figure 39. Schematic

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
EVAL AD5933EB	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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