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# SIMPLE WIDE FREQUENCY RANGE IMPEDANCE METER BASED ON AD5933 INTEGRATED CIRCUIT

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**Abstract**

As it contains elements of complete digital impedance meter, the AD5933 integrated circuit is an interesting solution for impedance measurements. However, its use for measurements in a wide range of impedances and frequencies requires an additional digital and analogue circuitry. This paper presents the design and performance of a simple impedance meter based on the AD5933 IC. Apart from the AD5933 IC it consists of a clock generator with a programmable prescaler, a novel DC offset canceller for the excitation signal based on peak detectors and a current to voltage converter with switchable conversion ratios. The authors proposed a simple method for choosing the measurement frequency to minimalize errors resulting from the spectral leakage and distortion caused by a lack of an anti-aliasing filter in the DDS generator. Additionally, a novel method for the AD5933 IC calibration was proposed. It consists in a mathematical compensation of the systematic error occurring in the argument of the value returned from the AD5933 IC as a result. The performance of the whole system is demonstrated in an exemplary measurement.

Keywords: impedance, converter, AD5933, SoC, system on a chip, measurement.



## 1. Introduction

As per the AD5933 integrated circuit (IC) datasheet, "The AD5933 is a high precision impedance converter system solution that combines an on-board frequency generator with a 12-bit, 1 MSPS, analogue-to-digital converter (ADC). (…) The response signal from the impedance is sampled by the on-board ADC and a discrete Fourier transform (DFT)" [1]. The AD5933 output voltage and measurement frequency are fully programmable and the communication is provided by an $I^2C$ interface.

An application of the AD5933 IC in biological diagnostics research has been reported by other authors. The AD5933 IC was used in the cell culture growth monitoring [2, 3], single cell measurement [4], blood coagulation detection [5], biosensor applications [6], general bio-impedance measurements [7–11], and was also used in technical object monitoring [12, 13]. It should be noted however, that in order to obtain the complete information about electrical properties of a measured object and to use a convenient method of the impedance spectra analysis (equivalent circuit modelling) the impedance has to be measured in a wide range of frequencies [14].

The technical data of exemplary impedance meters based on the AD5933 IC are listed in Table 1. Only three of the described devices allow to measure the impedance at more than three orders of magnitude of frequencies. The range of measured impedance is typically from 10 Ω to over 1 MΩ. However, in many cases the exact range is not given. Most of the mentioned impedance meters require additional analogue front-end circuits to provide a proper interface between the AD5933 IC and a measured sample.

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The motivation of the work was to construct a simple impedance meter based on the AD5933 IC for measuring impedance sensors used in microbiology. The designed, fabricated and tested device enables measurements in the frequency range from 1 Hz to 100 kHz and in the range of impedance from 10 Ω to 1 MΩ. It should be noted that in contrast to the design proposed by Hoja and Lentka [12, 13], the designed system is based on a single AD5933 IC which simplifies the measurement system architecture and enables its further miniaturisation.

Table 1. The list of impedance meters based on the AD5933.

| Author | Purpose | Frequency range | Impedance range | Maximum error |
|---|---|---|---|---|
| C. J. Chen et al. [2] | Cell culture minitoring | Fixed 10 Hz | No data | No data |
| T. Schwarzenberger et al. [3] | Cell culture minitoring | 100 Hz – 100 kHz | No data | 2 % - modulus, 2 % - argument |
| M. H. Wang et al. [4] (AD5934 used) | Single cell measurement | 0.1 Hz – 100 kHz | 100 Ω – 10 MΩ | Over 10 % for cell measurmeent |
| J. Broeders et al. [6] | Biosensor applications | 10 Hz – 100 kHz | 10 Ω – 5 MΩ | No data |
| P. Bogónez-Franco et al. [8] | Bioimpedance monitor | 100 Hz – 200 kHz | 10 Ω – 1 kΩ | 2.5 % - modulus, 4.5 % - argument |
| J. Ferreira et al. [9] | Bioimpedance with textile electrodes | 5 kHz – 450 kHz | No data | 0.7 % - resistance, 17 % - reactance |
| C. Margo et al. [10] | Bioimpedance embedded applications | 1 kHz – 100 kHz | No data | 2.5 % - modulus, 1.3 % - argument |
| A. Melwin and K. Rajasekaran [11] | Body composition measurement | Fixed 50 kHz | No data | 2 % (not specified) |
| J. Hoja and G. Lentka [12, 13] | Technical objects monitoring | 0.01 Hz – 100 kHz | 10 Ω – 10 GΩ | 1.6 % - modulus, 0.6 % - argument |

A number of difficulties were encountered during the construction of a simple impedance meter with a wide frequency range. Most of the cited papers focus on the experimental aspect of the work and do not mention the details of the impedance meter construction. Even the datasheets and application notes provided for the AD5933 IC by its manufacturer (Analog Devices) do not include some of the important information. This paper presents a detailed description of the design that will be useful to anyone building an impedance analyser based on the AD5933 IC.

Designers of impedance meters dedicated for biological objects should not forget about the requirements that have to be met. Besides, a measurement system should offer a wide frequency range, high degree of integration, portability and accuracy.

## 2. A simple impedance meter with a wide frequency range based on the AD5933 IC

### *2.1. The AD5933 IC*

The AD5933 IC is designed as a complete system for the impedance measurement (Fig. 1). It consists of a 27-bit direct digital synthesis (DDS) sine excitation voltage ($V_{out}$) generator, a digital-to-analogue converter (DAC) and a programmable gain amplifier ($PGA_1$) which determines the $V_{out}$ amplitude. The receive stage consists of a current-to-voltage converter (CVC), a programmable gain amplifier ($PGA_2$) and a low pass filter. The data processing block consists of a 12-bit analogue-to-digital converter (ADC) and a 1024 point discrete Fourier transform (DFT) engine with a sample windowing unit and a multiply-accumulate unit (MAC). As the result of DFT, the AD5933 gives a complex number; its modulus and argument should be proportional to the magnitude and phase of the measured current through an unknown impedance $Z_x$ which - for a constant amplitude of the voltage excitation - will also be proportional to the admittance of $Z_x$. An $I^2C$ interface provides communication with a microcontroller.

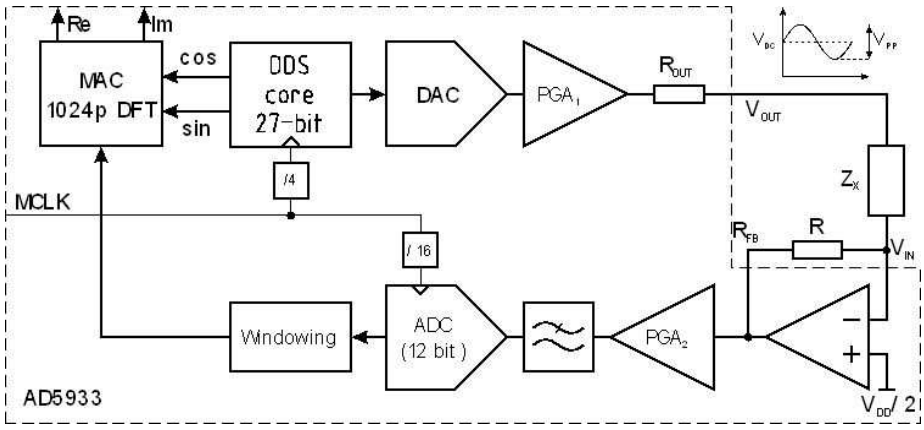



Fig. 1. A simplified block diagram of the AD5933 [1].

### *2.2. Hardware*

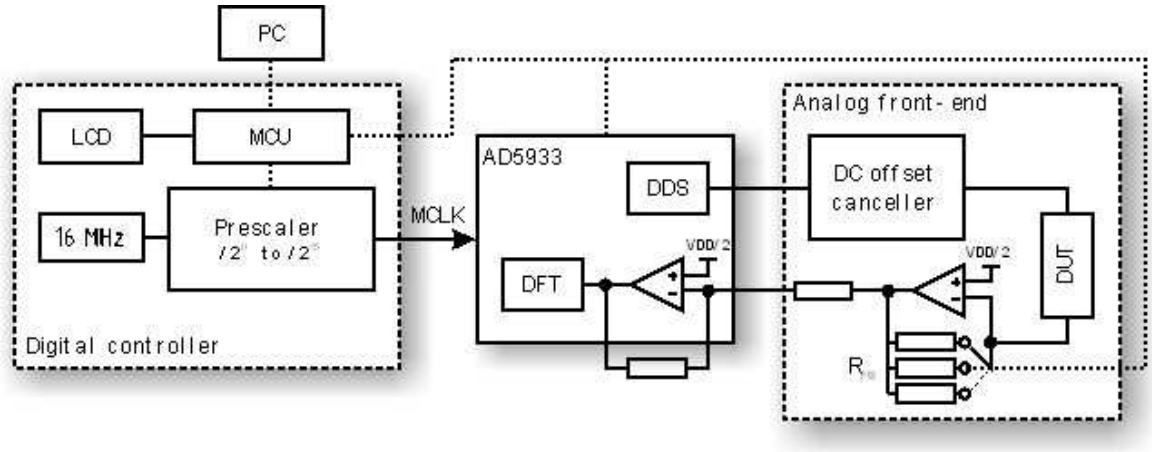
A dedicated measurement system was designed, fabricated and tested (Fig. 2). It consists of a digital controller, an AD5933 IC and an analogue front-end circuit. The digital controller is based on the Atmel ATmega32 microcontroller (MCU). It also consists of an external 16 MHz clock source for the AD5933 IC, a selectable clock prescaler ($/2^0 \div /2^{15}$), an LCD display and a USART to USB converter. The measurement system is equipped with a female goldpin socket for connecting measured objects directly or for an additional analogue front-end board (Fig. 2c) which contains a DC offset canceller (described in section 2.3.), an additional socket for the measured device under test (DUT) and an external CVC with selectable feedback resistors $R_{FB}$. Separate 5 V voltage supplies for digital (VCC) and analogue (AVCC) circuits are provided.

### *2.3. Sample excitation*

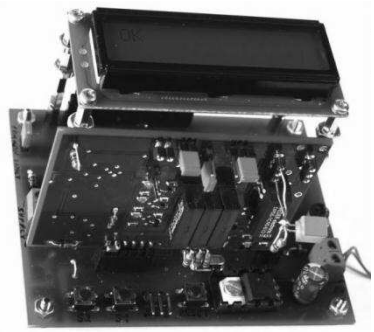
The AD5933 IC provides four selectable output voltage levels each with a different DC bias (Table 2). At the same time the voltage at the input of CVC is constant and for 3.3 V supply equals to 1.65 V. This would cause the DC polarization at the measured impedance. This type of excitation is not suitable for biological object measurements because of their ionic conductivity [14]. The excitation voltage should be free of a DC bias and its amplitude

should be low enough, to not cause an electrolysis in the measured object. The magnitude of the electric field should not exceed 1 $V \cdot cm^{-1}$ [15].

a)




b)



c)

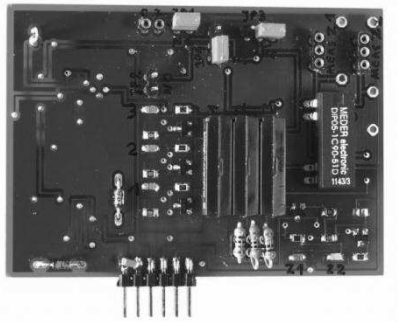


Fig. 2. A simple impedance meter with a wide frequency range based on the AD5933 IC: a block diagram a), a general view b) and the analogue front-end board c).

Table 2. AD5933 Output voltage ranges for 3.3 V voltage supply [1].

| Range | Output voltage level | DC bias | Typical output serial resistance |
|---|---|---|---|
| 1 | 1.98 $V_{pp}$ | 1.48 V | 200 Ω |
| 2 | 0.97 $V_{pp}$ | 0.76 V | 2.4 kΩ |
| 3 | 383 $mV_{pp}$ | 0.31 V | 1 kΩ |
| 4 | 198 $mV_{pp}$ | 0.173V | 600 Ω |

The presence of an output serial resistance (Table 2) limits the lower boundary of the measured impedance range.

The solution to the problems described above requires an additional analogue front-end circuitry. Its purpose would be the DC offset removal without limiting a frequency range, an attenuation of the excitation voltage and minimizing the output resistance. A diagram of the analogue front-end circuit is presented in Fig. 3.

The DC canceller based on a simple RC high-pass filter which is proposed by Analog Devices and is used in some of exemplary AD5933 IC impedance meters [6, 10], is not suitable for operating in a wide range of frequencies. The time constant of the RC filter has to be significantly longer than the longest period of the excitation voltage. Therefore, it would require a long settling time before the measurement.

The authors present another approach to a DC bias canceller (Fig. 3). It consists of positive (IC1A, IC2A) and negative (IC1B, IC2B) peak detectors following the upper and lower envelope of the excitation voltage which can be reset if necessary by Q1 and Q2 transistors.

The voltage from the detectors is averaged on R8 and R9 resistors and it corresponds to the DC bias voltage. The performance of the DC bias detector circuit is presented in Fig. 4. For low frequencies the exact value of the DC bias is detected after one excitation period.

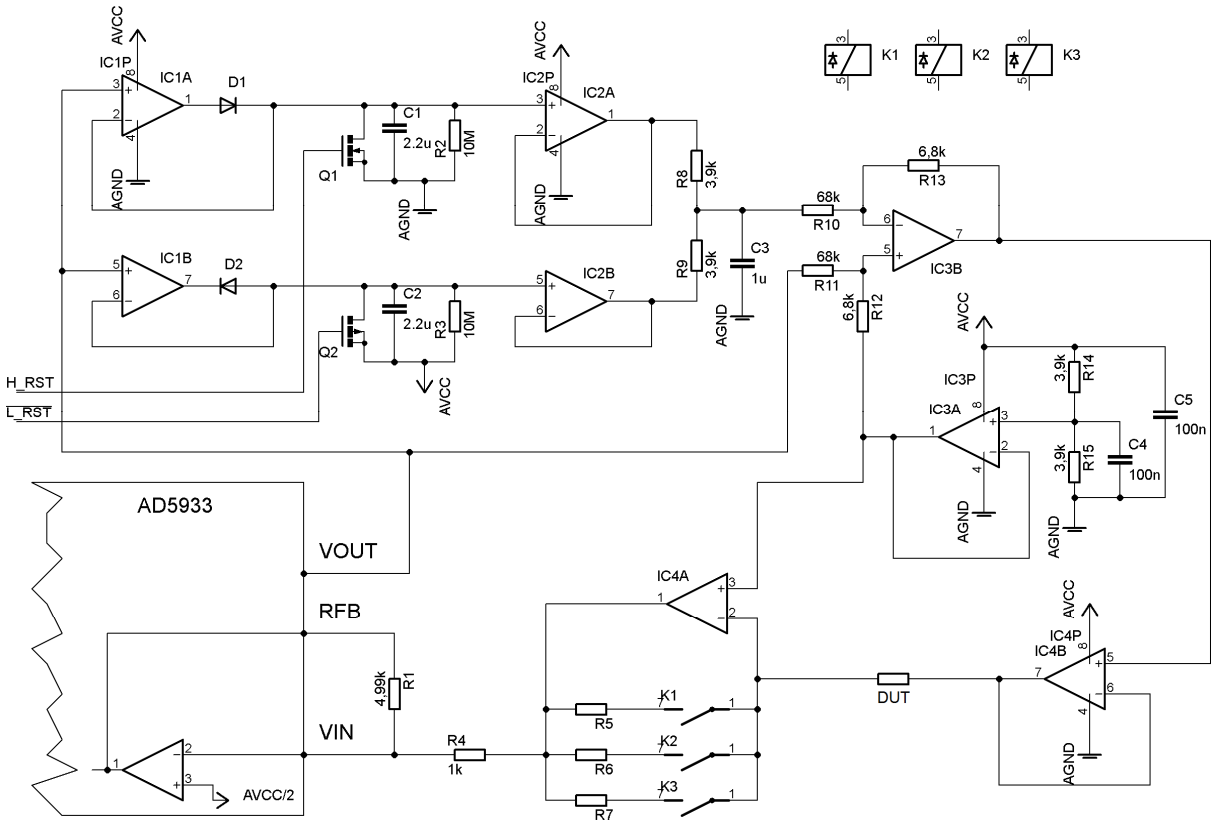



Fig. 3. A diagram of the analogue front-end board for a simple impedance meter with a wide frequency range based on the AD5933 IC.

$V_{out}$ of the AD5933 IC is attenuated 10 times and its DC bias level is shifted to AVCC/2 in IC3B (Fig. 3). As a result, the output voltage of IC3B has the same DC bias as CVC and its amplitude is low enough to be suitable for biological objects. To provide a low output impedance the IC4B buffer is used.

The IC4A amplifier is an external CVC with known parameters, able to measure impedances down to 10 Ω. An internal AD5933 IC CVC is not used; its gain is fixed at 5. Note that adding the second CVC causes the phase inversion of the measured signal.

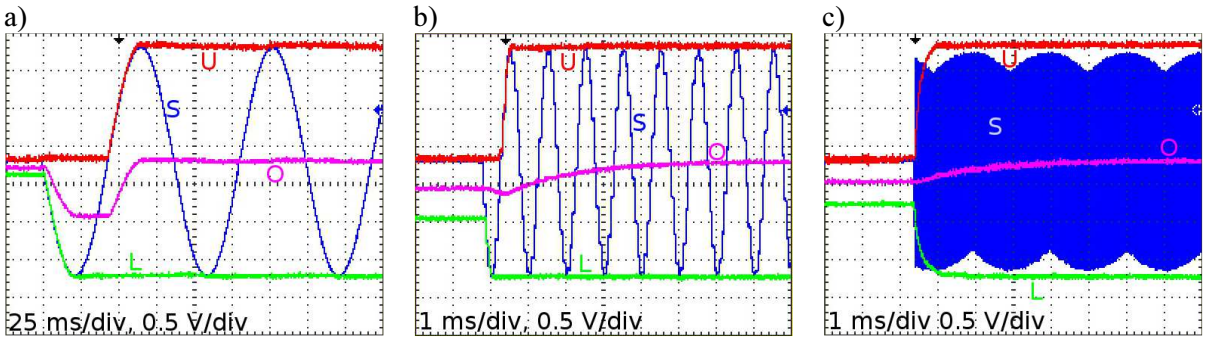



Fig. 4. Oscillograms illustrating the operation of a DC bias detector for 10 Hz a), 1 kHz b) and 100 kHz signal c). Positive and negative peak detectors track the upper (U) and lower (L) envelope of the signal (S) evaluating the average of the signal at the bias canceller output (O) in a wide range of freqencies.

### *2.4. Measured impedance range*

The CVC in the receive stage can work properly only with a given range of the impedance modulus of the measured object, depending on the resistor value in its negative feedback loop.

Due to a limited dynamics of the 12-bit ADC in the AD5933 IC the voltage amplitude at its input should be greater than 15 mV (verified experimentally). As a consequence, the voltage from the external CVC in our circuit (Fig. 3) should be greater than 0.6 mV because of the 25 times amplification.

The maximum output voltage of the external CVC is determined by its conversion ratio and should not be greater than $V_{OUT}$ which is applied on the DUT. When the CVC is built on an operational amplifier maintaining an amplification ratio below unity it ensures the bandwidth independency of the measured impedance. For a proper operation, the $R_{fb}$ resistor value in the CVC feedback loop must be smaller than the impedance modulus of the DUT. Also, the voltage amplitude applied on the ADC in the AD5933 IC cannot exceed a half of the supply voltage.

The minimum and maximum values of the impedance modulus are given in (1) and (2), respectively:

$$|Z|_{x\_\min} = \frac{V_{OUT} \cdot R_{fb}}{V_{CVC\_\max}}, \tag{1}$$

$$|Z|_{x\_\max} = \frac{V_{OUT} \cdot R_{fb}}{V_{CVC\_\min}}, \tag{2}$$

where $V_{OUT}$ is the amplitude of the voltage applied on the DUT, $R_{fb}$ is the resistor value in the CVC feedback loop, $V_{CVC\_min}$ is the minimum output voltage amplitude from the CVC (0.6 mV) and $V_{CVC\_max}$ is the maximum output voltage amplitude from the CVC (equal to $V_{OUT}$, in our case - 30 mV). To widen the measured impedance range, $R_{fb}$ can be switched by simple relays as shown in Fig. 3 (parts R5, R6, R7 and K1, K2, K3). The number of the relays may be increased to widen the measured impedance range.

## 3. An analysis of the impedance measurement by the AD5933

### *3.1. DFT accuracy*

The DFT implemented in the AD5933 IC is called a single-point DFT, meaning that the analysis or correlation frequency in the MAC core is always at the same frequency as the current output excitation frequency. If the input signal period over the 1024-point sample interval is an integer, there will be a smooth transition from the end of one period to the beginning of the next one. If this number is not an integer, there will not be a smooth transition from the end of one period to the beginning of the next one. The leakage is a result of the discontinuities introduced by the DFT [16].

To achieve accurate results using the DFT and to avoid the leakage it is necessary that the sampling time $T_s$ given by:

$$T_S = \frac{1024}{\frac{MCLK}{16}}, \tag{3}$$

is the integer multiplication of the DDS generator period $T_S$:

$$T_S = k \cdot T_{DDS} = k \frac{2^{27}}{DDS \cdot \frac{MCLK}{4}}, \tag{4}$$

where $k$ is the number of DDS generator periods per the sampling time ($T_{DDS}$), $MCLK$ is the master clock frequency and $DDS$ is the DDS tuning word. The equation (4) yields:

$$k = \frac{DDS}{2^{15}}. \tag{5}$$

The effect of the leakage is reduced by the signal windowing. The results of setting the DDS frequency without concerning this effect are shown in Fig. 5.

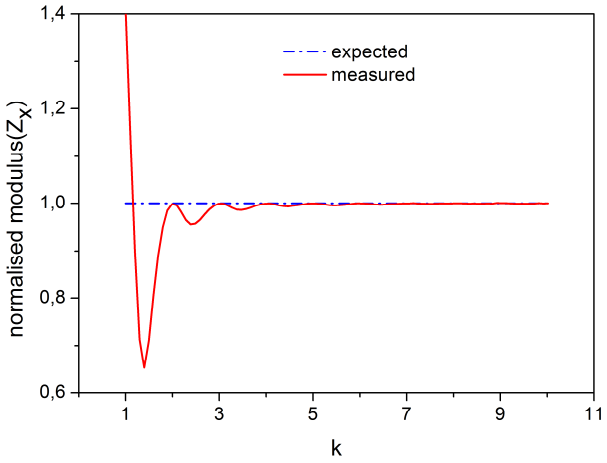



Fig. 5. The results of the aliasing in the DFT implemented in the AD5933 for a given number of periods of the DDS signal (k) per the sampling time.

For high values of $k$ (therefore large values of the DDS tuning word) another issue appears. Large values of DDS tuning words cause that the DDS output changes significantly at each clock cycle resulting in a stair-shaped excitation signal (Fig. 6). If e.g. the DUT equivalent circuit contains serial R-C branches having time constants similar to the period of consecutive steps in the excitation signal, then spikes at the CVC output appear. This distortion is caused by the charging current of the R-C branches of the equivalent circuit.

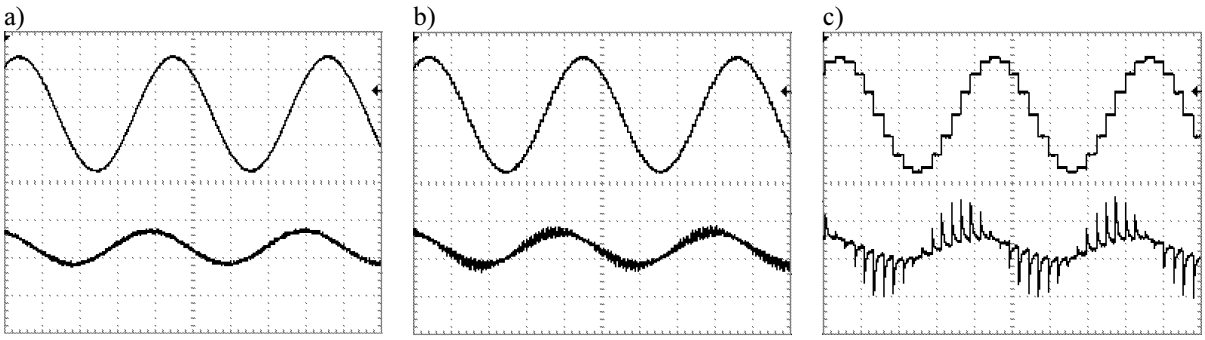



Fig. 6. Oscillograms of the AD5933 output signal (the upper waveform) and the CVC output signal (the lower waveform) while measuring a serial R-C network at 976 Hz for k=16 MCLK=1 MHz a), k=64 MCLK=250 kHz b) and k=256 MCLK = 62.5 kHz c). Horizontal scale: 250µs/div.

### *3.2. Systematic admittance argument error*

The results from the AD5933 IC have a systematic, frequency dependent error in the admittance argument which the user has to compensate. The dependence of the argument on the values generated by the AD5933 measuring the 10 kΩ resistor with 10 kΩ $R_{FB}$ on the DDS tuning word is presented in Fig. 7a. The measurement was performed without external analog circuits from Fig. 3.

For the resistor, the argument of the result should be frequency independent and equal to 0 but the AD5933 IC returns the values which depend linearly on the DDS tuning word and in addition are offset by 90°. Analog Devices propose to eliminate this error by the calibration [1, 16]. Another proposal of how to deal with this problem is presented in a measurement circuit developed by Hoja and Lentka who used two AD5933 ICs in a new configuration different from the one recommended in the manufacturer's application note [12, 13], where a simultaneous measurement of the voltage and current eliminates a need of the calibration cycle and removes the systematic error. We tried to analyze the factors on which this error depends and to compensate it mathematically.

The 90° argument offset must be a result of using the DFT for analysing a sinusoidal signal. If the DDS produces a cosinusoidal excitation the issue does not appear. The frequency-dependence of the systematic argument error must be the result of a delay between the sampling of the voltage at the input of the internal ADC and feeding the conversion result to the DDS. At each cycle the DDS multiplies the current value generated by the DFT with the ADC result shifted several clock cycles (Fig. 4b). Such a delay may be caused e.g. by a time required for the ADC conversion and windowing.

The DDS frequency is given by [1]:

$$f = \frac{DDS \cdot MCLK}{2^{29}}, \tag{6}$$

where *DDS* is the 24-bit tuning word, *f* is the output frequency of the generator and *MCLK* is the clock signal applied to AD5933. The time delay described above causing the apparent argument shift $\Delta\varphi$ depends on the period of the signal:

$$\frac{\Delta\varphi}{360°} \cdot \frac{1}{f} = \Delta t = n \cdot \frac{1}{MCLK}, \tag{7}$$

where $\Delta t$ is the time delay. On the other hand, it should be possible to express the delay with an integer number of MCLK clock signal cycles; in the above equation that number is *n*. Combining (6) and (7) we obtain:

$$\frac{\Delta\varphi}{360^\circ} = n \cdot \frac{DDS}{2^{29}}. \tag{8}$$

Therefore, plotting the argument $\Delta\varphi/360°$ vs. $DDS/2^{29}$ we obtain the delay in MCLK cycles as a slope of the linear fit which would allow to calculate the necessary value for correcting the argument of the value returned by the AD5933 IC. The results of fitting are shown in Fig. 7a.

The delay discussed above appears to be dependent on the MCLK frequency. The delays were 29 cycles for 16 MHz, 24 cycles for 8 MHz, 21 cycles for 4 MHz and 20 cycles for 2 MHz and lower clock frequencies.

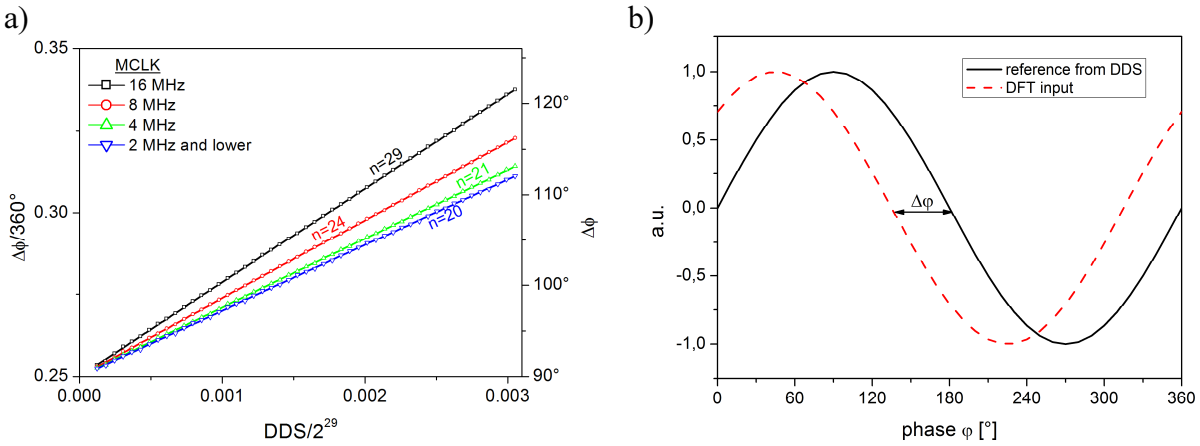



Fig. 7. The systematic error in the argument measurement of Δφ dependence on the AD5933 DDS tuning word a) and the illustration of the time offset between the excitation and the sine value for a DFT transform b).

## 4. Exemplary measurements

A measurement of a simple RLC network was conducted to test the measurement system performance and the correctness of the AD5933 result processing proposed in section 3. The external analogue front-end circuit was used. First, the one – point calibration has to be done but only for scaling the CVC, as the argument measurement systematic error is already known.

For a given excitation level and $PGA_2$ state, the magnitude $M$ of the complex number read from the AD5933 after the measurement is proportional to the magnitude of the admittance $|Y|$ of the measured object.

$$M = C \cdot R_{fb} \cdot |Y| . \tag{9}$$

The calibration was done at the 1 kHz excitation using a 10 kΩ resistor as the reference, with a 3.3 kΩ resistor as $R_{fb}$ for 2 $V_{pp}$ DAC amplitude and 5x $PGA_2$ turned on. The scaling factor $C$ was calculated as 1119. The equation (9) may be rearranged to give the value of the magnitude of the admittance or impedance based on the measured $M$ and a known scaling factor:

$$|Z| = \frac{1}{|Y|} = \frac{C \cdot R_{fb}}{M} . \tag{10}$$

To demonstrate the performance of the system, an expemplary measurement of a model RLC network (Fig. 8) was performed. The parameters of its components were determined basing on the impedance spectra measurement with a precise Agilent 4249A analyzer and equivalent circuit modelling using a ZView (Scribner Assoc., 2010) software. Next, the impedance spectrum of the RLC network was simulated and assumed as the reference value.

The impedance spectrum of the same model was then measured with an AD5933-based impedance analyzer using the magnitude calibration methods and the systematic argument error correction (described in section 3.2). The results are presented in Fig. 9.

The comparison between the measurement and the reference shows a good agreement at wide ranges of frequencies and impedances The standard uncertainty of the measurement was determined, and its value is 3.5 % for the impedance modulus and 2.8 degrees for the impedance argument.

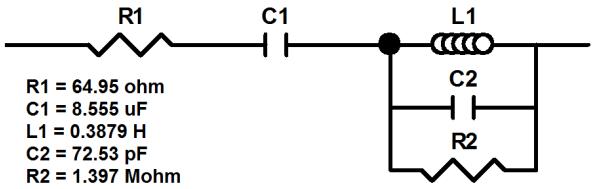



Fig. 8. The RLC network used to test the measurement system.

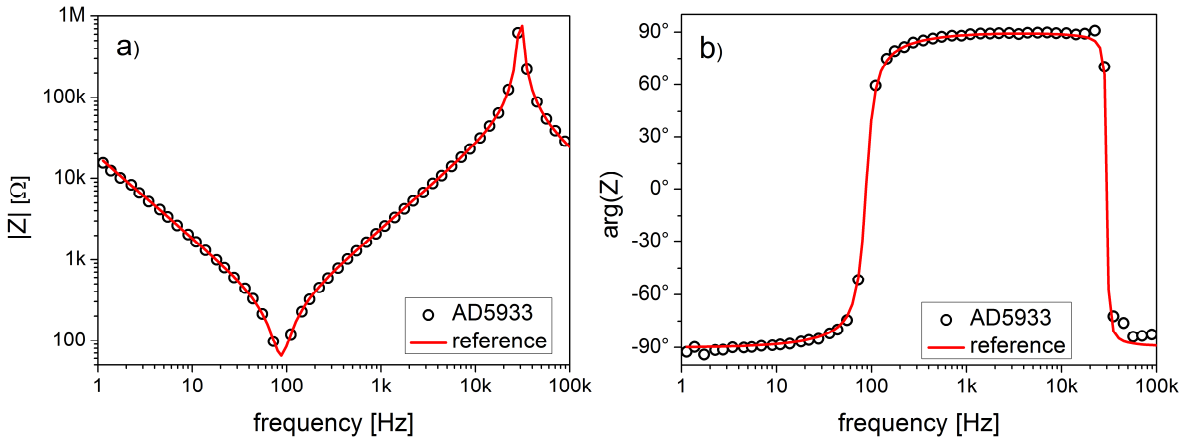



Fig. 9. The Bode plot of the impedance magnitude a) and argument b) of the RLC network in a wide range of frequencies and impedances measured with our system (dots) and in the ideal case (lines).

## 5. Conclusions

An operating example of the AD5933-based simple impedance analyser is presented. It allows to measure impedances from 10 Ω to 1 MΩ at frequencies from 1 Hz to 100 kHz, which covers the range needed for biological applications.

To achieve the goal, an algorithm for selecting DDS tuning words and MCLK clocks was implemented. It allows to avoid two issues: spikes at the CVC output and a DFT spectrum leakage. Most of the wide frequency range measurements are done with the frequency changing logarithmically. Such logarithmic sweeps are not supported automatically by the AD5933. Therefore, in our system they are controlled by an MCU. Independently of the type of the sweep (linear or logarithmic), the measurement procedure at each point of the sweep consists of the following steps:

a) Determining the wanted frequency $f_w$.
b) Selecting an appropriate prescaler ratio for MCLK to limit the $k$ (described in section 3.1) in the range from 16 to 32 (if possible) to avoid spikes in the CVC. Using the equation (11).

$$k = \frac{f_w \cdot 1024}{\frac{MCLK}{16}}. \tag{11}$$

c) For a given prescaler, selecting the nearest frequency which may be measured without a spectrum leakage; in other words – the frequency for which $k$ is an integer.
d) Setting the DDS tuning word with the value calculated from (4) – keeping $k$ as an integer and starting the measurement.

The AD5933 IC offers almost a complete system for measuring the electrical impedance. Unfortunately, it is not free from flaws that need to be corrected. For biological objects measurements it is necessary to reduce the amplitude of the output excitation voltage $V_{out}$ and to remove the DC offset using additional analog circuits. To improve the measurement accuracy it is necessary to reduce the output impedance of the AD5933 IC by adding a voltage follower, or - even better - using two AD5933 ICs - one for measuring the current and second for monitoring the voltage on the measured object. An extension of the measured impedance modulus range can be obtained by switching resistors $R_{fb}$ in the feedback loop of the current-to-voltage converter. Unfortunately, it also requires an additional analog part which increases the complexity of the complete device. The system also requires separating analogue and digital power supplies due to the voltage noise. The software controlling the AD5933 must have calibration data implemented not only for the measured impedance modulus but also for the impedance argument which is dependent on the signal frequency. The impedance argument is not constant due to the delay in the input tract of the DFT block. To maintain a good measurement accuracy it is necessary to ensure that the number of signal periods processed in the DFT is either an integer or is large enough to minimise a spectrum leakage.

## Acknowledgements

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