SBOS391–DECEMBER 2007

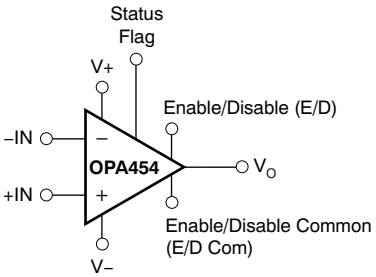
# High-Voltage (100V), High-Current (50mA) OPERATIONAL AMPLIFIERS, G = 1 Stable

## FEATURES

- **WIDE POWER-SUPPLY RANGE: ±5V (10V) to ±50V (100V)**
- **HIGH OUTPUT LOAD DRIVE: $I_O$ > ±50mA**
- **WIDE OUTPUT VOLTAGE SWING: 1V to Rails**
- **INDEPENDENT OUTPUT DISABLE OR SHUTDOWN**
- **WIDE TEMPERATURE RANGE: –40°C to +85°C**
- **PACKAGES: SO and HSOP PowerPAD™**

## APPLICATIONS

- **TEST EQUIPMENT**
- **AVALANCHE PHOTODIODE: High-V Current Sense**
- **PIEZOELECTRIC CELLS**
- **TRANSDUCER DRIVERS**
- **SERVO DRIVERS**
- **AUDIO AMPLIFIERS**
- **HIGH-VOLTAGE COMPLIANCE CURRENT SOURCES**
- **GENERAL HIGH-VOLTAGE REGULATORS/POWER**




## DESCRIPTION

The OPA454 is a low-cost operational amplifier with high voltage (100V) and relatively high current drive (25mA). It is unity-gain stable and has a gain-bandwidth product of 2.5MHz.

The OPA454 is internally protected against over-temperature conditions and current overloads. It is fully specified to perform over a wide power-supply range of ±5V to ±50V or on a single supply of 10V to 100V. The status flag is an open-drain output that allows it to be easily referenced to standard low-voltage logic circuitry. This high-voltage op amp provides excellent accuracy, wide output swing, and is free from phase inversion problems that are often found in similar amplifiers.

The output can be independently disabled using the Enable/Disable Pin that has its own common return pin to allow easy interface to low-voltage logic circuitry. This disable is accomplished without disturbing the input signal path, not only saving power but also protecting the load.

Featured in a small exposed metal pad package, the OPA454 is easy to heatsink over the extended industrial temperature range, –40°C to +85°C.

**Table 1. OPA454 RELATED PRODUCTS**

| PRODUCT | DESCRIPTION |
|---|---|
| OPA445 (1) | 80V, 15mA |
| OPA452 | 80V, 50mA |
| OPA547 | 60V, 750mA |
| OPA548 | 60V, 3A |
| OPA549 | 60V, 9A |
| OPA551 | 60V, 200mA |
| OPA567 | 5V, 2A |
| OPA569 | 5V, 2.4A |

(1) The OPA445 is pin-compatible with the OPA445, except in applications using the offset trim, and NC pins other than open.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING |
|---|---|---|---|
| OPA454 | SO-8 | DDA | OPA454 |
| OPA454 | HSOP-20(2) | DWD | OPA454 |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Available Q2, 2008.

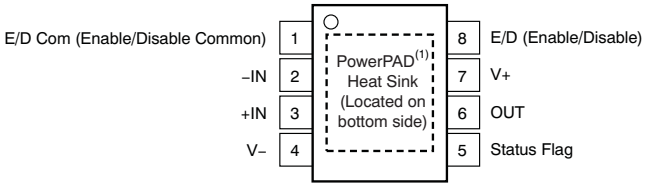
## ABSOLUTE MAXIMUM RATINGS(1)

| | | | OPA454 | UNIT |
|---|---|---|---|---|
| Supply Voltage | | $V_S$ = (V+) – (V–) | 120 | V |
| Signal Input Terminals, Voltage(2) | | | (V–) – 0.3 to (V+) + 0.3 | V |
| Signal Input Terminals, Current(2) | | | ±10 | mA |
| E/D to E/D Com Voltage | | | +5.5 | V |
| Output Short-Circuit(3) | | $I_{SC}$ | Continuous | |
| Operating Temperature | | $T_J$ | –55 to +125 | °C |
| Storage Temperature | | | –55 to +125 | °C |
| Junction Temperature | | $T_J$ | +150 | °C |
| ESD Rating: | Human Body Model (HBM) | | 4000 | V |
| | Charged Device Model (CDM) | | 500 | V |
| | Machine Model (MM) | | 150 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground.

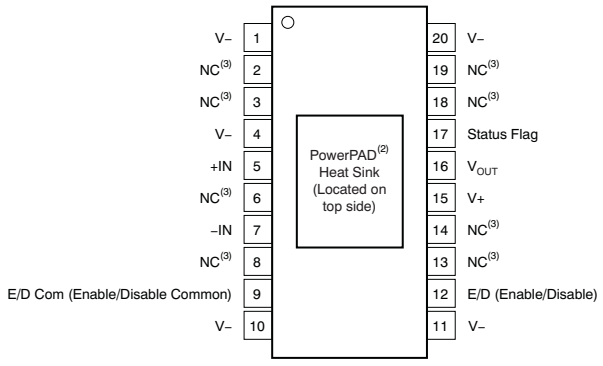
## PIN ASSIGNMENTS

**DDA PACKAGE**
**SO-8 PowerPAD**
**(TOP VIEW)**




(1) PowerPAD is internally connected to V–. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation.

**DWD PACKAGE(1)**
**HSOP-20 PowerPAD**
**(TOP VIEW)**




(1) Available Q2, 2008.
(2) PowerPAD is internally connected to V–.
(3) NC = No internal connection

## ELECTRICAL CHARACTERISTICS: $V_S$ = ±50V

**Boldface** limits apply over the specified temperature range, **$T_A$ = –40°C to +85°C.**
At $T_P$ (1) = +25°C, $R_L$ = 4.8kΩ to mid-supply, $V_{CM}$ = $V_{OUT}$ = mid-supply, unless otherwise noted.

| PARAMETER | | CONDITIONS | OPA454 MIN | OPA454 TYP | OPA454 MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $I_O$ = 0 | | ±0.2 | ±4 | mV |
| **vs Temperature (2)** | **$dV_{OS}/dT$** | | | **±1.6** | **±10** | **µV/°C** |
| vs Power Supply | PSRR | $V_S$ = ±4V to ±60V, $V_{CM}$ = 0V | | 25 | 100 | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| Input Bias Current | $I_B$ | | | ±1.4 | ±100 | pA |
| **vs Temperature** | | | **See Typical Characteristics** | | | |
| Input Offset Current | $I_{OS}$ | | | ±0.2 | ±100 | pA |
| **NOISE** | | | | | | |
| Input Voltage Noise Density, f = 10Hz | $e_n$ | | | 300 | | nV/√Hz |
| Input Voltage Noise Density, f = 10kHz | | | | 35 | | nV/√Hz |
| f = 0.01Hz to 10Hz | | | | 15 | | $\mu V_{PP}$ |
| Current Noise Density, f = 1kHz | $i_n$ | | | 40 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | Linear Operation | (V–) + 2.5 | See Note (3) | (V+) – 2.5 | V |
| Common-Mode Rejection | CMRR | $V_S$ = ±50V, –25V ≤ $V_{CM}$ ≤ +25V | 100 | 146 | | dB |
| | | $V_S$ = ±50V, –45V ≤ $V_{CM}$ ≤ +45V | 100 | 147 | | dB |
| **Over Temperature** | | **$V_S$ = ±50V, –25V ≤ $V_{CM}$ ≤ +25V** | **80** | **88** | | **dB** |
| **Over Temperature** | | **$V_S$ = ±50V, –45V ≤ $V_{CM}$ ≤ +45V** | **72** | **82** | | **dB** |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | $10^{13}$ \|\| 10 | | Ω \|\| pF |
| Common-Mode | | | | $10^{13}$ \|\| 9 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-Loop Voltage Gain (4) | $A_{OL}$ | | | | | |
| | | (V–) + 1V < $V_O$ < (V+) – 1V, $R_L$ = 49kΩ, $I_O$ = ±1mA | 100 | 130 | | dB |
| | | **(V–) + 1V < $V_O$ < (V+) – 1V, $R_L$ = 49kΩ, $I_O$ = ±1mA** | | **112** | | **dB** |
| | | (V–) + 1V < $V_O$ < (V+) – 2V, $R_L$ = 4.8kΩ, $I_O$ = ±10mA | 100 | 115 | | dB |
| | | **(V–) + 1V < $V_O$ < (V+) – 2V, $R_L$ = 4.8kΩ, $I_O$ = ±10mA** | | **106** | | **dB** |
| | | (V–) + 2V < $V_O$ < (V+) – 3V, $R_L$ = 1880Ω, $I_O$ = ±25mA | 80 | 102 | | dB |
| | | **(V–) + 2V < $V_O$ < (V+) – 3V, $R_L$ = 1880Ω, $I_O$ = ±25mA** | | **84** | | **dB** |

(1) $T_P$ is the temperature of the leadframe die pad (exposed thermal pad) of the PowerPAD package.
(2) See typical characteristic curve, *Offset Voltage Drift Production Distribution* (Figure 14).
(3) Typical range is (V–) + 1.5V to (V+) – 1.5V.
(4) Measured using low-frequency (<10Hz) ±49V square wave. See typical characteristic curve, *Current Limit vs Temperature* (Figure 24).

## ELECTRICAL CHARACTERISTICS: $V_S$ = ±50V (continued)

**Boldface** limits apply over the specified temperature range, **$T_A$ = –40°C to +85°C.**
At $T_P$ = +25°C, $R_L$ = 4.8kΩ to mid-supply, $V_{CM}$ = $V_{OUT}$ = mid-supply, unless otherwise noted.

| PARAMETER | | CONDITIONS | OPA454 MIN | OPA454 TYP | OPA454 MAX | UNIT |
|---|---|---|---|---|---|---|
| **FREQUENCY RESPONSE**(5) | | | | | | |
| Gain-Bandwidth Product | GBW | Small-Signal | | 2.5 | | MHz |
| Slew Rate | SR | G = ±1, $V_O$ = 80V Step, $R_L$ = 3.27kΩ | | 13 | | V/µs |
| Full-Power Bandwidth(6) | | | | 35 | | kHz |
| Settling Time: ±0.1%(7) | | G = ±1, $V_O$ = 20V Step | | 3 | | µs |
| Settling Time: ±0.01%(7) | | G = ±5 or ±10, $V_O$ = 80V Step | | 10 | | µs |
| Total Harmonic Distortion + Noise(8) | THD+N | $V_S$ = +40.6V/–39.6V, G = ±1, f = 1kHz, $V_O$ = 77.2$V_{PP}$ | | 0.0008 | | % |
| **OUTPUT** | | | | | | |
| Voltage Output Swing From Rail(9) | $V_O$ | $R_L$ = 49kΩ, $A_{OL}$ ≥ 100dB, $I_O$ = 1mA | (V–) + 1 | | (V+) – 1 | V |
| | | $R_L$ = 4.8kΩ, $A_{OL}$ ≥ 100dB, $I_O$ = 10mA | (V–) + 1 | | (V+) – 2 | V |
| | | $R_L$ = 1880Ω, $A_{OL}$ ≥ 80dB, $I_O$ = 26mA | (V–) + 2 | | (V+) – 3 | V |
| Continuous Current Output, dc | | Depends on Circuit Conditions | | See Figure 6 | | |
| Maximum Peak Current Output, Current Limit(10) | $I_O$ | | | +120/–150 | | mA |
| **Over Temperature** | | | | **+140/–170** | | **mA** |
| Capacitive Load Drive(5) | $C_{LOAD}$ | | | 200 | | pF |
| Open-Loop Output Impedance | $R_O$ | | | See Figure 5 | | Ω |
| Output Disabled | | | | | | |
| Output Capacitance | | | | 18 | | pF |
| Feedthrough Capacitance(11) | | | | 150 | | fF |
| **STATUS FLAG PIN (Referenced to E/D Com)**(12) | | | | | | |
| Status Flag Delay | | Enable → Disable | | 6 | | µs |
| | | Disable → Enable | | 4 | | µs |
| | | Over-Current Delay(13) | | 15 | | µs |
| | | Over-Current Recovery Delay(13) | | 10 | | µs |
| Junction Temperature | $T_J$ | | | | | |
| Alarm (status flag high) | | | | +150 | | °C |
| Return to Normal Operation (status flag low) | | | | +130 | | °C |
| Output Voltage(5) | | Normal Operation | | | E/D Com + 2 | V |
| | | $R_L$ = 100Ω During Thermal Overdrive, Alarm | (V+) – 2.5 | | | V |

(5) See Typical Characteristic curves.
(6) See typical characteristic curve, *Maximum Output Voltage vs Frequency (Figure 12)*.
(7) See the Applications Information section, *Settling Time*.
(8) Supplies reduced to allow closer swing to rails due to test equipment limitations. See typical characteristic curve *Total Harmonic Distortion + Noise vs Temperature* (Figure 30 and Figure 31) for additional power levels.
(9) See typical characteristic curve, *Output Voltage Swing vs Output Current* (Figure 11).
(10) Measured using low-frequency (<10Hz) ±49V square wave. See typical characteristic curve, *Current Limit vs Temperature* (Figure 24).
(11) Measured using Figure 1.
(12) 100kΩ pull-up resistor to (V+). E/D common to (V–). Status flag indicates an over temperature or over-current condition.
(13) See Typical Characteristic curves for current limit behavior.

## ELECTRICAL CHARACTERISTICS: $V_S$ = ±50V (continued)

**Boldface** limits apply over the specified temperature range, **$T_A$ = –40°C to +85°C.**
At $T_P$ = +25°C, $R_L$ = 4.8kΩ to mid-supply, $V_{CM}$ = $V_{OUT}$ = mid-supply, unless otherwise noted.

| PARAMETER | | CONDITIONS | OPA454 MIN | OPA454 TYP | OPA454 MAX | UNIT |
|---|---|---|---|---|---|---|
| **E/D (ENABLE/DISABLE) PIN** | | | | | | |
| E/D Pin, Referenced to E/D Com Pin(14)(15) | | | | | | |
| High (output enabled) | $V_{SD}$ | Pin Open or Forced High | E/D Com + 2.5 | | E/D Com + 5 | V |
| Low (output disabled) | $V_{SD}$ | Pin Forced Low | E/D Com | | E/D Com + 0.65 | V |
| Output Disable Time | | | | 4 | | µs |
| Output Enable Time | | | | 3 | | µs |
| **E/D COM PIN** | | | | | | |
| Voltage Range | | | (V–) | | (V+) – 5 | V |
| **POWER SUPPLY** | | | | | | |
| Specified Range | $V_S$ | | | ±50 | | V |
| Operating Voltage Range | | | ±5 | | ±50 | V |
| Quiescent Current | $I_Q$ | $I_O$ = 0 | | 3.2 | 4 | mA |
| Quiescent Current in Shutdown Mode | | $I_O$ = 0, $V_{E/D}$ = 0.65V | | 150 | 210 | µA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | $T_A$ | | –40 | | +85 | °C |
| Operating Range | $T_A$ | | –55 | | +125 | °C |
| Thermal Resistance, Junction-to-Case(16) | | | | | | |
| SO-8 PowerPAD(17) | $\theta_{JC}$ | | | 10 | | °C/W |
| HSOP-20 | | | | 10 | | °C/W |
| Thermal Resistance, Junction-to-Ambient | $\theta_{JA}$ | | | | | |
| SO-8 PowerPAD(17) | | | | 24/52 | | °C/W |
| HSOP-20(18) | | | | 65 | | °C/W |

(14) See typical characteristic curve, *$I_{ENABLE}$ vs $V_{ENABLE}$* (Figure 46).
(15) High enables the outputs.
(16) $T_P$ is the temperature of the leadframe die pad (exposed thermal pad) of the PowerPAD package.
(17) Lower value is for land area of 1-inch × 1-inch, 2-oz copper. Upper value is for exposed-pad sized area of 1-oz copper.
(18) Value given is for DW-20 package, similar to the DWD package, but without an exposed pad. Actual $\theta_{JA}$ may approach $\theta_{JC}$ by selection of external heatsink and airflow.

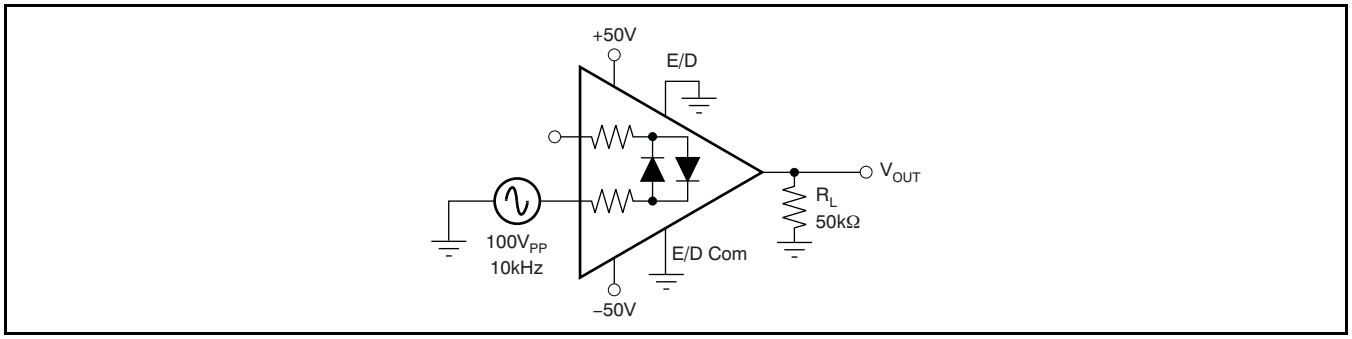



**Figure 1. Feedthrough Capacitance Circuit**

## TYPICAL CHARACTERISTICS

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

**OPEN-LOOP GAIN AND PHASE vs FREQUENCY**

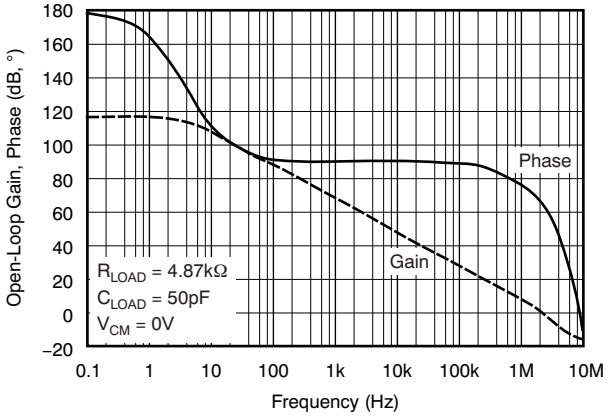



**Figure 2.**

**PHASE MARGIN vs TEMPERATURE**

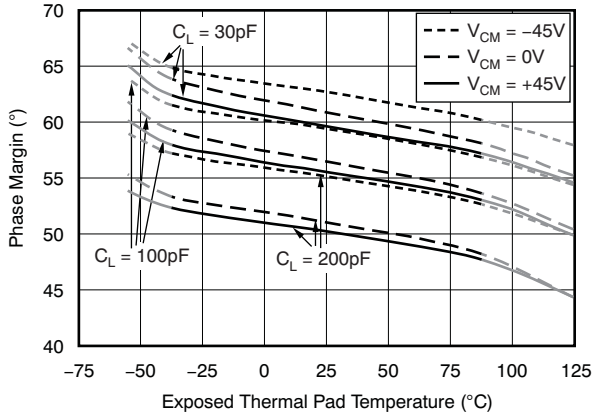



**Figure 3.**

**UNITY-GAIN BANDWIDTH vs TEMPERATURE**

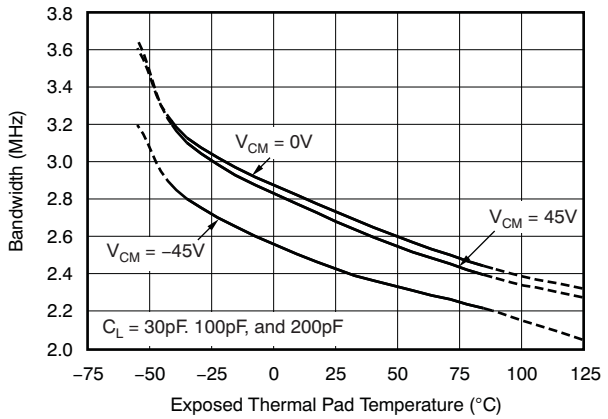



**Figure 4.**

**OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY**

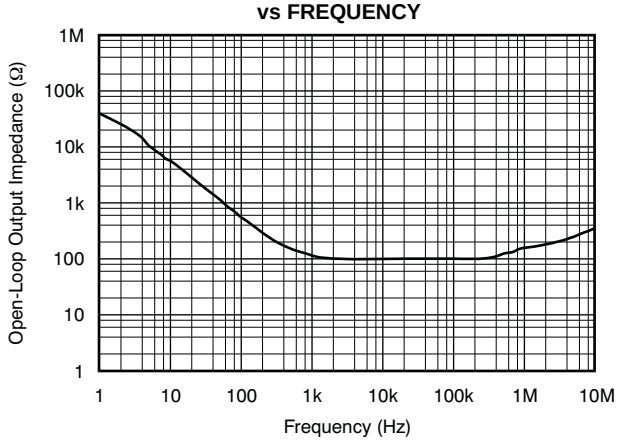



**Figure 5.**

**OPEN-LOOP GAIN vs PEAK-LOAD CURRENT**

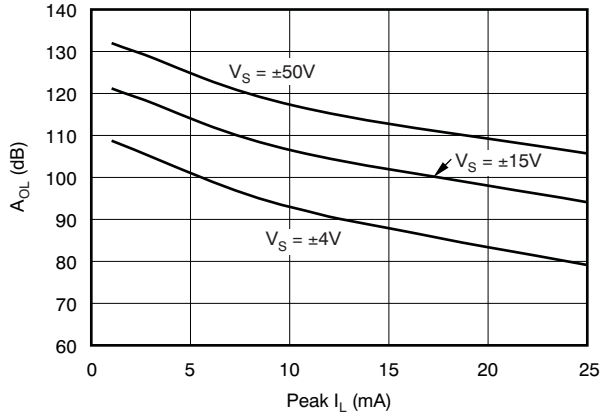



**Figure 6.**

**OPEN-LOOP GAIN vs TEMPERATURE**

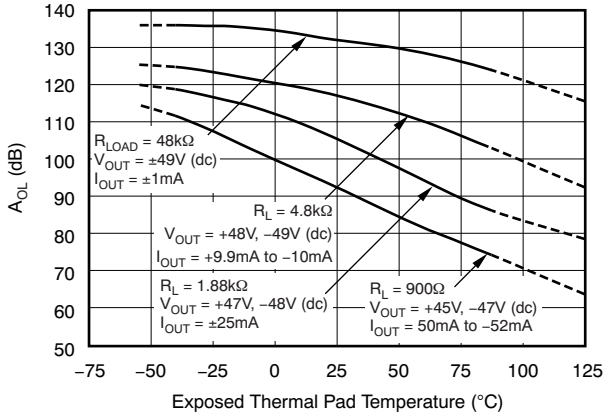



**Figure 7.**

## TYPICAL CHARACTERISTICS (continued)

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

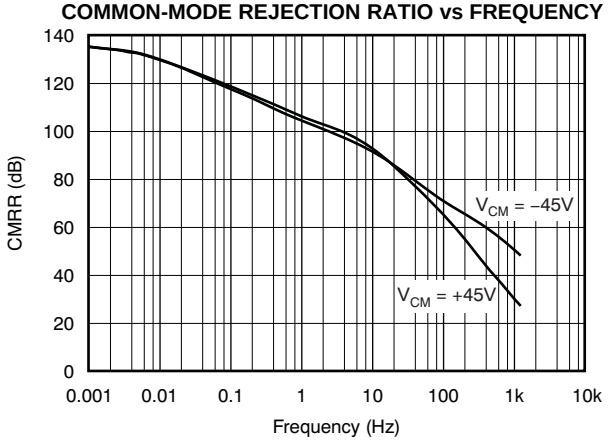



**Figure 8.**

**POWER-SUPPLY AND COMMON-MODE REJECTION RATIO vs TEMPERATURE**

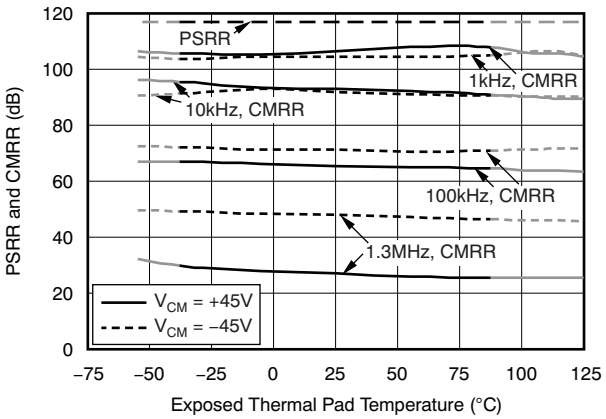



**Figure 9.**

**POWER-SUPPLY REJECTION RATIO vs FREQUENCY**

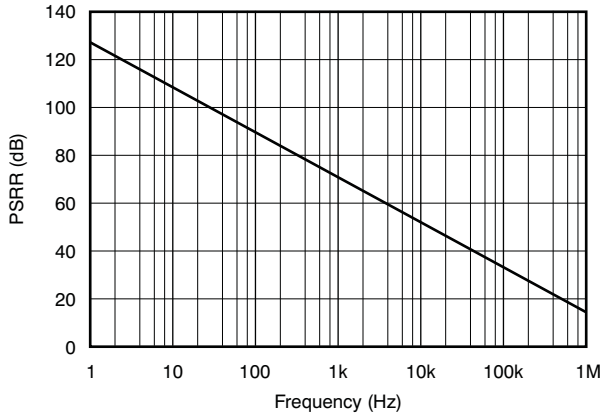



**Figure 10.**

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (Measured When Status Flag Transitions From Low to High)**

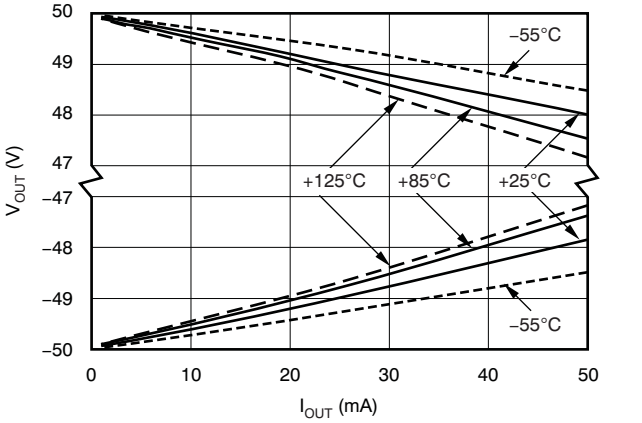



**Figure 11.**

**MAXIMUM OUTPUT VOLTAGE vs FREQUENCY**

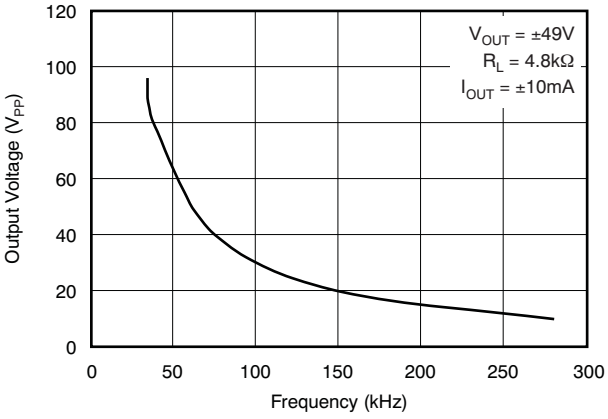



**Figure 12.**

**DDA PACKAGE OFFSET VOLTAGE PRODUCTION DISTRIBUTION**

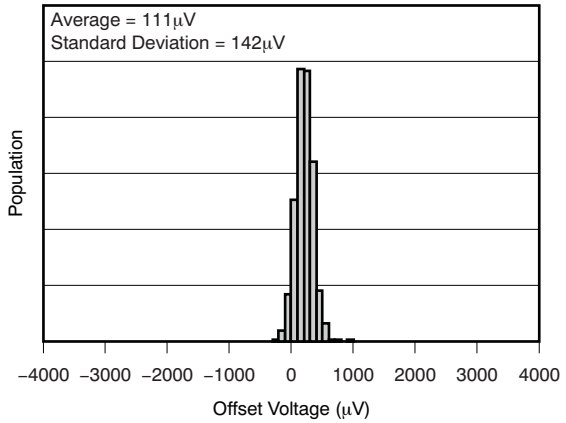



**Figure 13.**

## TYPICAL CHARACTERISTICS (continued)

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

**DDA PACKAGE OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION**

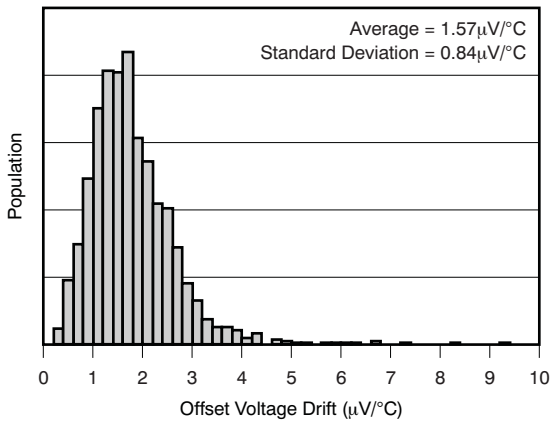



**Figure 14.**

**DDA PACKAGE, SOLDER-ATTACHED, $V_{OS}$ TC SHIFT**

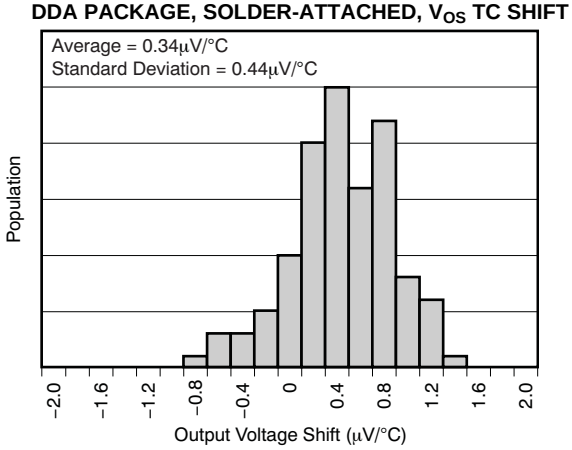



**Figure 15.**

**DDA PACKAGE, SOLDER-ATTACHED, $V_{OS}$ SHIFT**

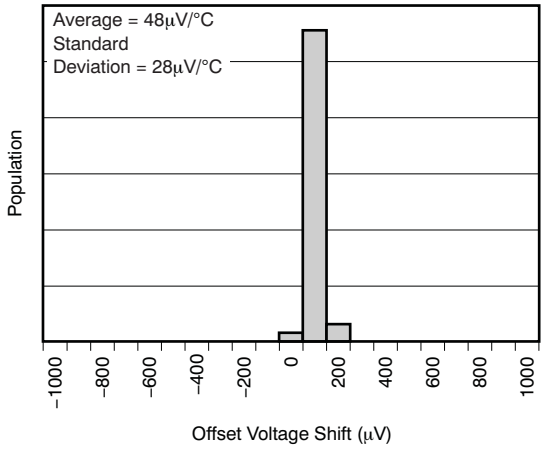



**Figure 16.**

**OFFSET VOLTAGE WARMUP (60 Devices)**

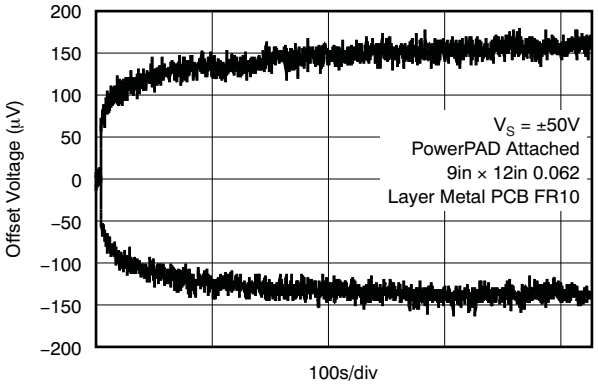



**Figure 17.**

**QUIESCENT CURRENT PRODUCTION DISTRIBUTION**

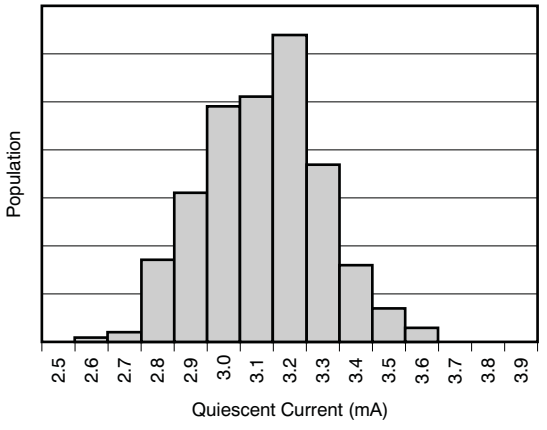



**Figure 18.**

**QUIESCENT CURRENT vs SUPPLY VOLTAGE**

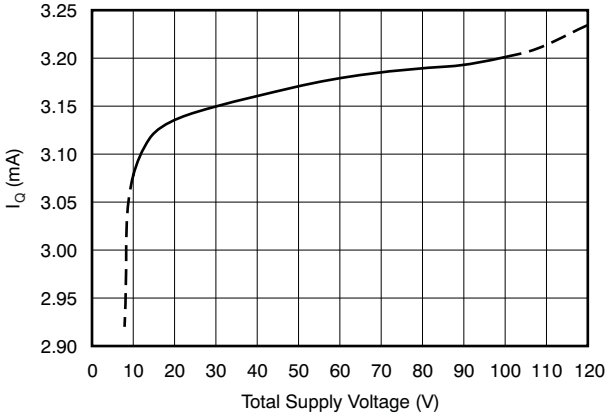



**Figure 19.**

## TYPICAL CHARACTERISTICS (continued)

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

**QUIESCENT CURRENT vs TEMPERATURE**

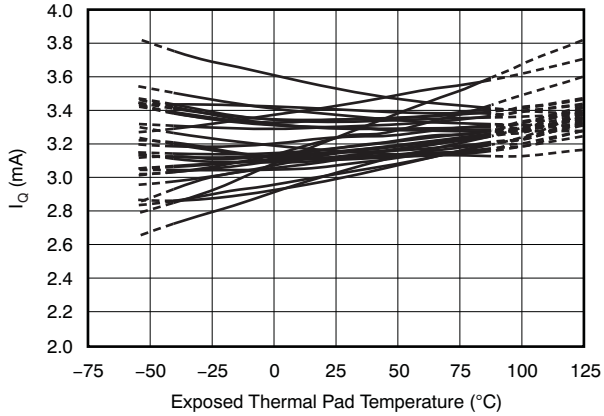



**Figure 20.**

**SHUTDOWN CURRENT vs TEMPERATURE**

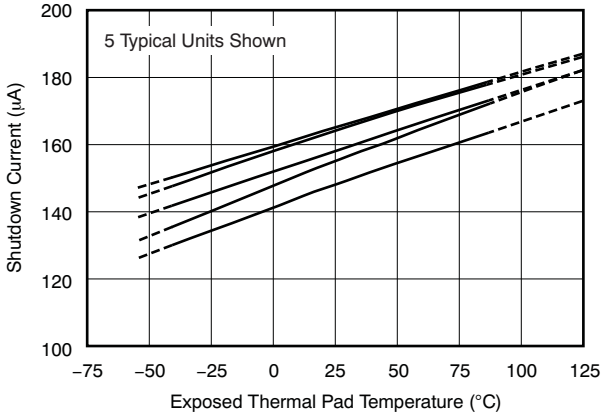



**Figure 21.**

**INPUT BIAS CURRENT vs TEMPERATURE**

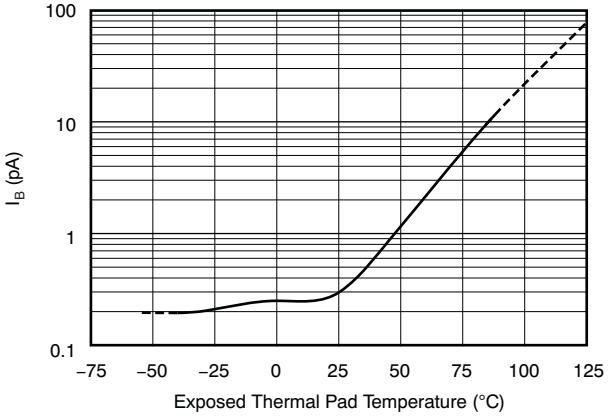



**Figure 22.**

**INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE**

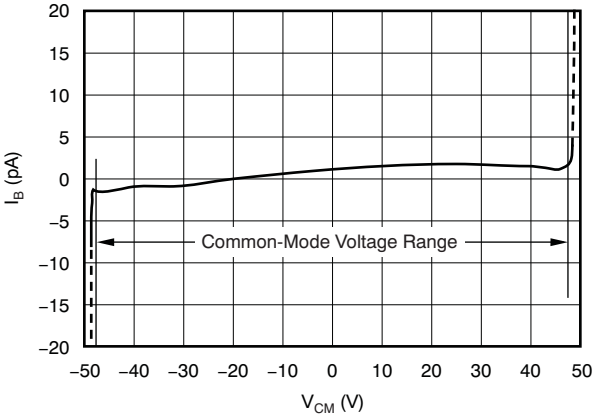



**Figure 23.**

**CURRENT LIMIT vs TEMPERATURE**

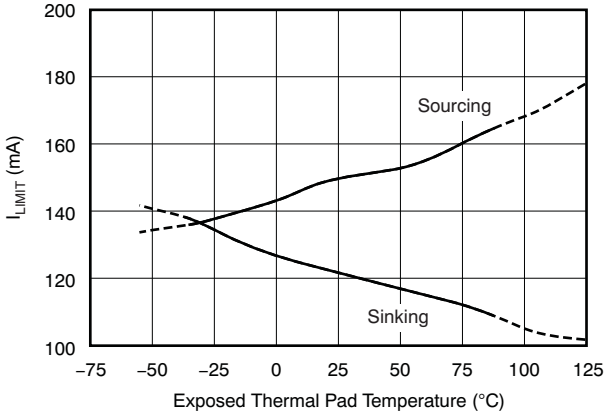



**Figure 24.**

**STATUS FLAG VOLTAGE vs TEMPERATURE (E/D Com Connected to V–)**(1)

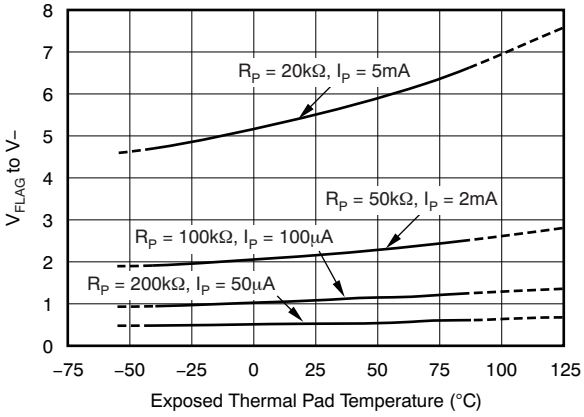



**Figure 25.**

(1) See Figure 57 in the *Applications Information* section.

## TYPICAL CHARACTERISTICS (continued)

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

**MAXIMUM POWER DISSIPATION vs TEMPERATURE WITH MINIMUM ATTACH AREA**

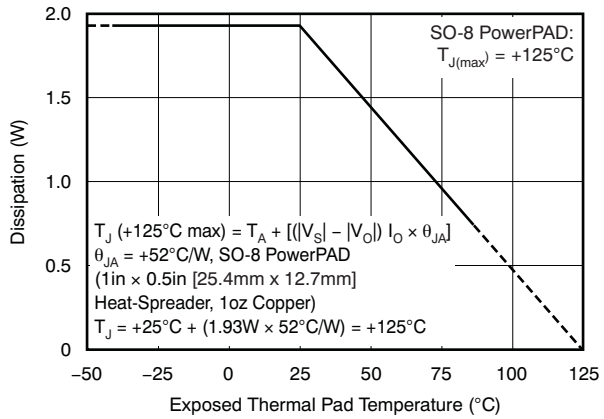



**Figure 26.**

**SLEW RATE vs TEMPERATURE**

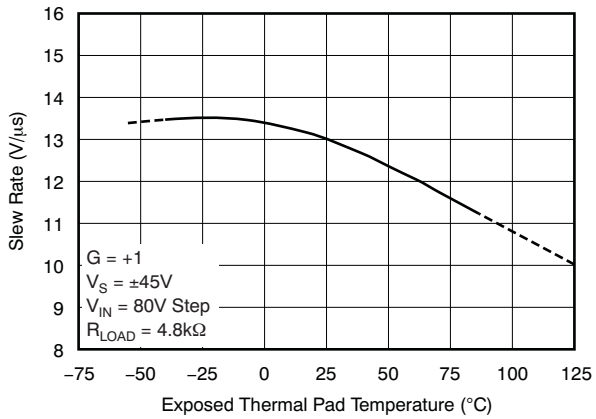



**Figure 27.**

**INPUT VOLTAGE NOISE SPECTRAL DENSITY**

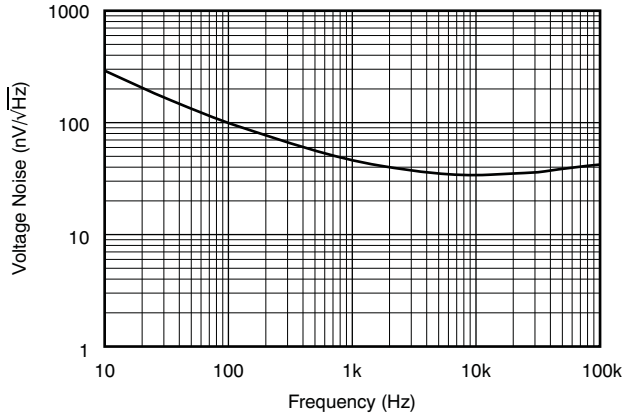



**Figure 28.**

**0.01Hz TO 10Hz INPUT VOLTAGE NOISE**

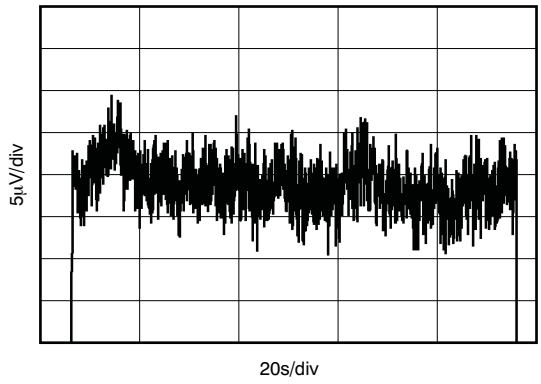



**Figure 29.**

**TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE**

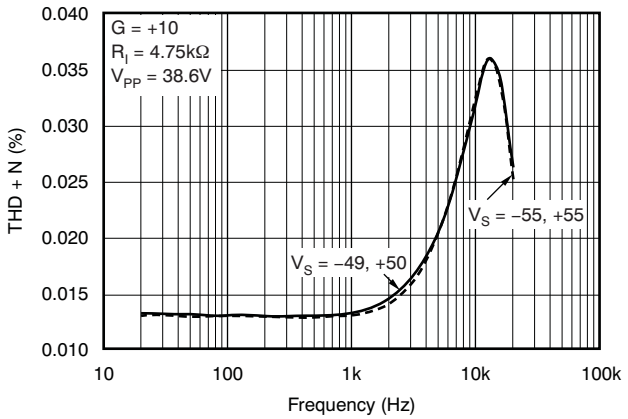



**Figure 30.**

**TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE**

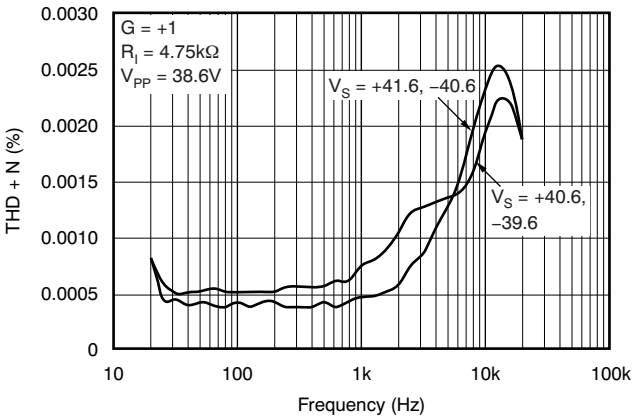



**Figure 31.**

## TYPICAL CHARACTERISTICS (continued)

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

**LARGE-SIGNAL STEP RESPONSE**

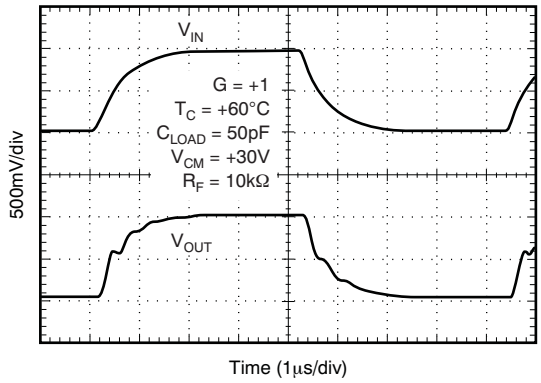



**Figure 32.**

**LARGE-SIGNAL STEP RESPONSE**

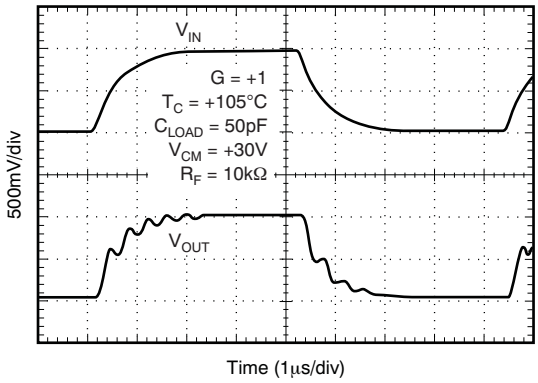



**Figure 33.**

**LARGE-SIGNAL STEP RESPONSE**

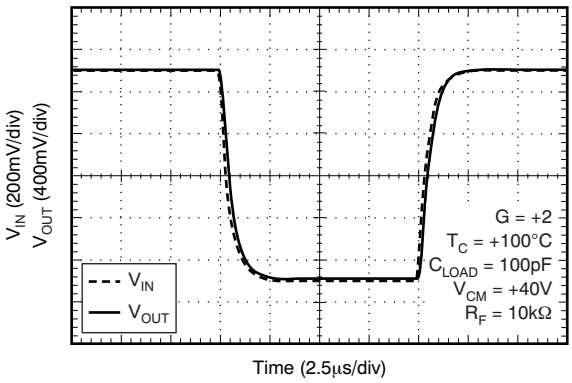



**Figure 34.**

**SMALL-SIGNAL STEP RESPONSE**

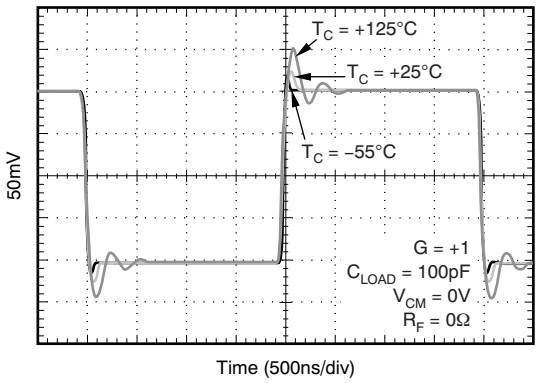



**Figure 35.**

**STEP RESPONSE**

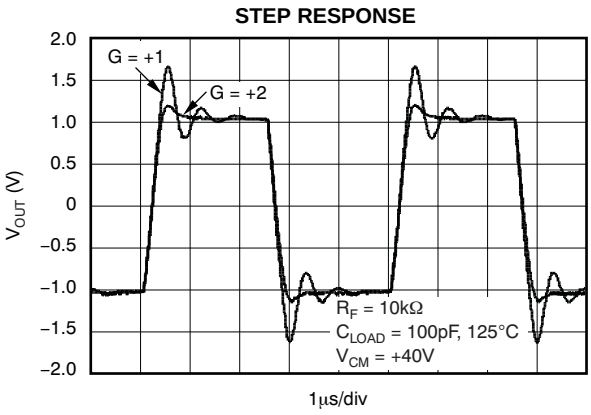



**Figure 36.**

**GAIN PEAKING vs $C_{LOAD}$ (G = +1, $V_{CM}$ = 0V)** (2)

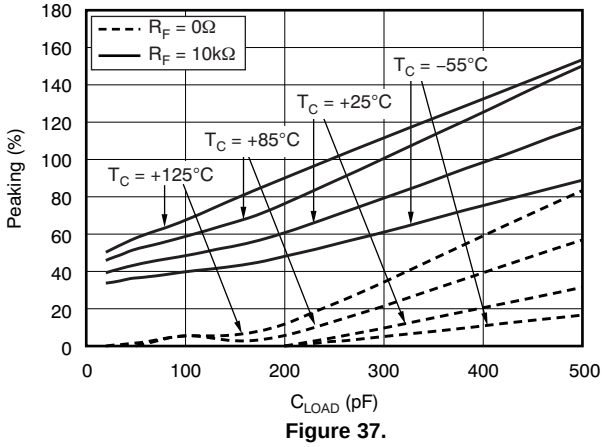



**Figure 37.**

(2) See Application section *Unity-Gain Noninverting Configuration*.

## TYPICAL CHARACTERISTICS (continued)

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

**GAIN PEAKING vs $C_{LOAD}$ (G = +2, $R_F$ = 10kΩ, $V_{CM}$ = 0V)**

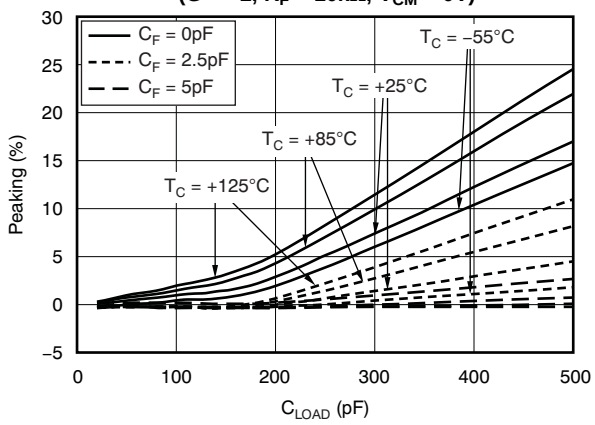



**Figure 38.**

**GAIN OF +1 vs FREQUENCY(3)**

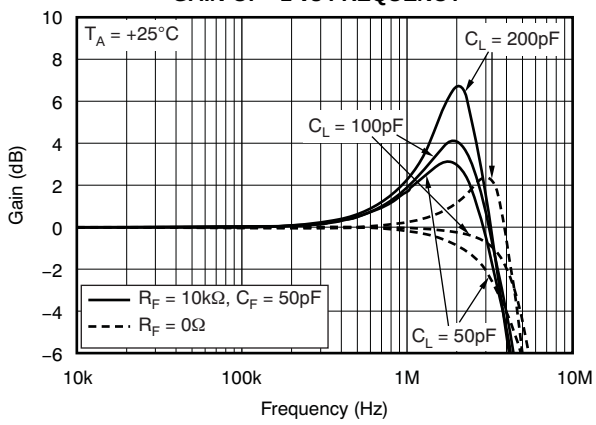



**Figure 39.**

**GAIN OF +2 vs FREQUENCY(4)**

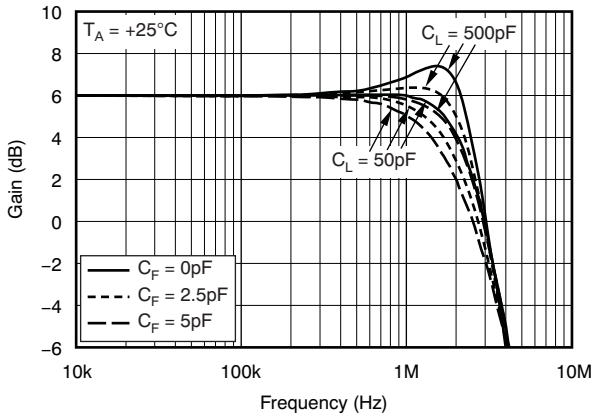



**Figure 40.**

**SETTLING TIME, POSITIVE STEP (20V Step, Gain = 1, $R_F$ = 10kΩ)(5)(6)**

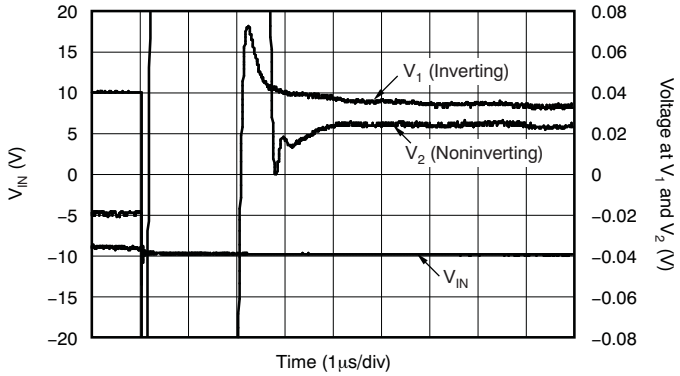



**Figure 41.**

(3) See Application section *Unity-Gain Noninverting Configuration*.
(4) See Application section *Unity-Gain Noninverting Configuration*.
(5) See the *Settling Time* section.
(6) The grid for voltage at $V_1$ and $V_2$ is scaled 20mV or 0.1% per division.

## TYPICAL CHARACTERISTICS (continued)

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

**SETTLING TIME, NEGATIVE STEP**
**(20V Step, Gain = 1, $R_F$ = 10kΩ)**(7)(8)

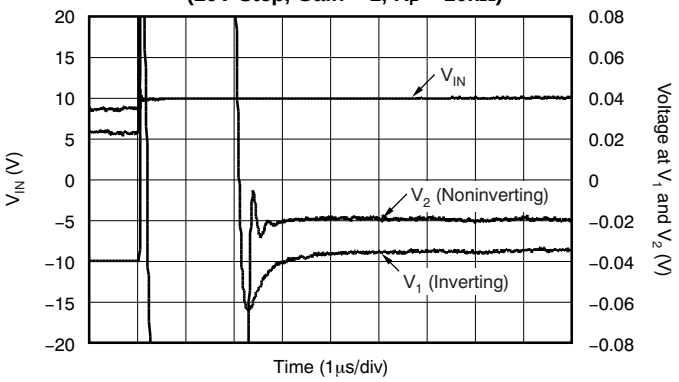



**Figure 42.**

**ENABLE RESPONSE TIME**

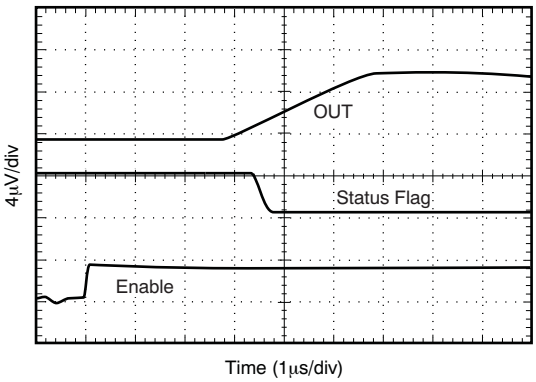



**Figure 43.**

**DISABLE RESPONSE TIME**

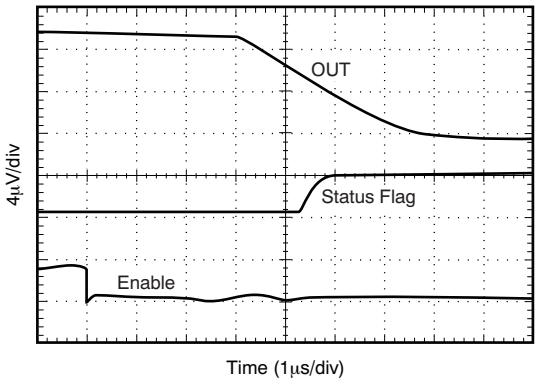



**Figure 44.**

**ENABLE RESPONSE**

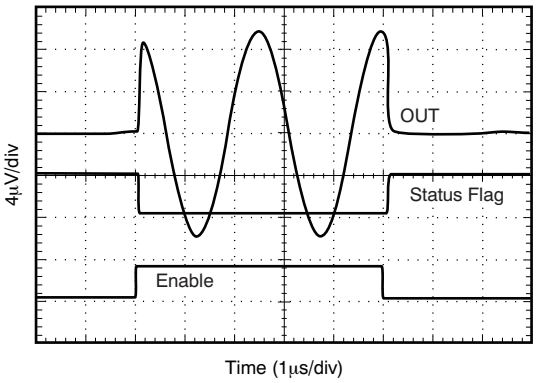



**Figure 45.**

**$I_{ENABLE}$ vs $V_{ENABLE}$**

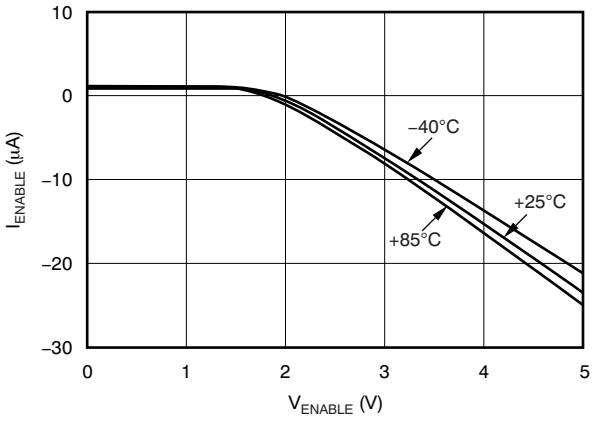



**Figure 46.**

**ENABLE/DISABLE THRESHOLD vs TEMPERATURE**

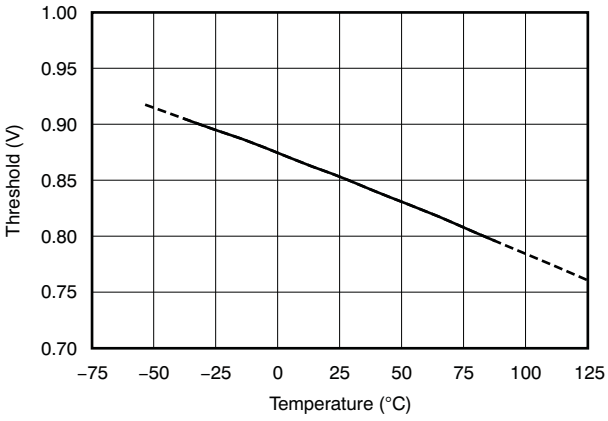



**Figure 47.**

(7) See the *Settling Time* section.
(8) The grid for voltage at $V_1$ and $V_2$ is scaled 20mV or 0.1% per division.

## TYPICAL CHARACTERISTICS (continued)

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

**$I_{LIMIT}$ SHOWING FLAG DELAY ($T_P$ = +125°C)(9)**

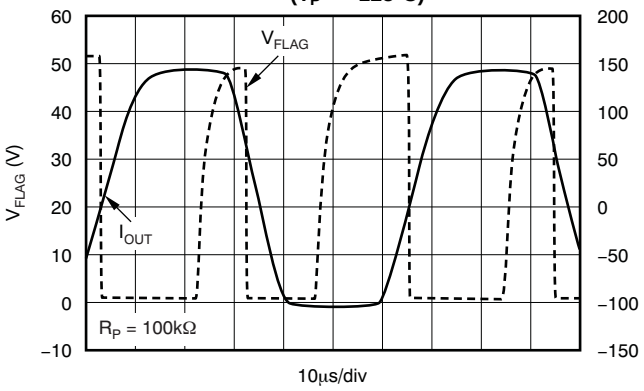



**Figure 48.**

**$I_{LIMIT}$ SHOWING FLAG DELAY ($T_P$ = +25°C)(10)**

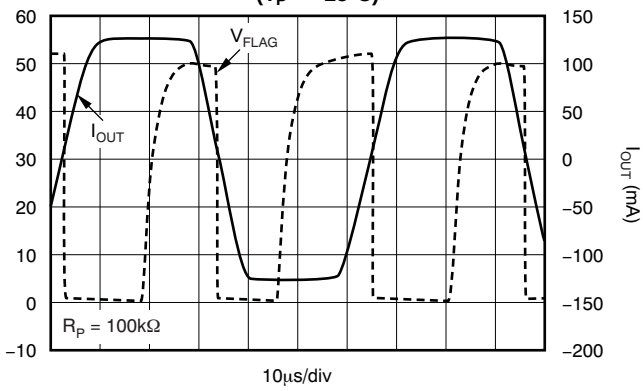



**Figure 49.**

**$I_{LIMIT}$ SHOWING FLAG DELAY ($T_P$ = –55°C)(11)**

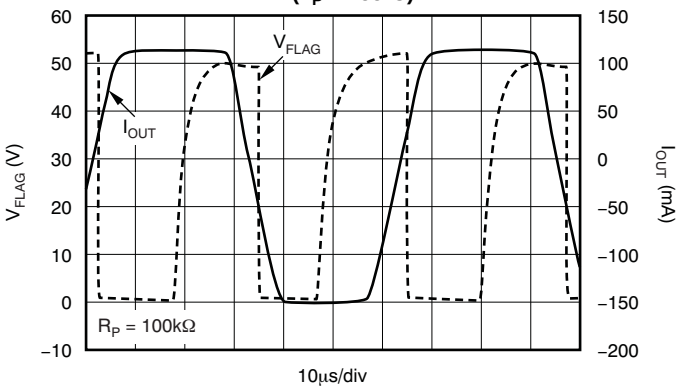



**Figure 50.**

**APPLY LOAD (25mA Sink Response)**

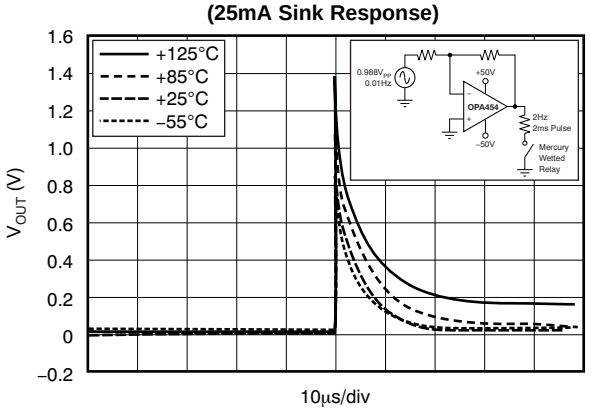



**Figure 51.**

**REMOVE LOAD (25mA Sink Response)**

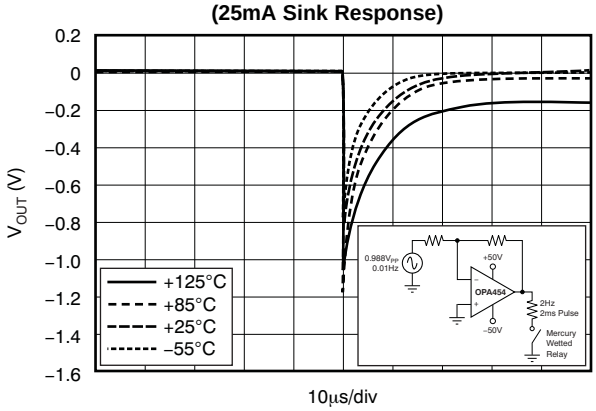



**Figure 52.**

**APPLY LOAD (25mA Source Response)**

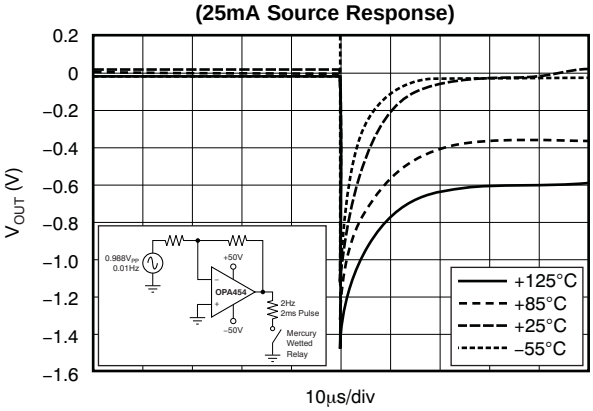



**Figure 53.**

(9) The OPA454 was connected to sufficient heatsinking to prevent thermal shutdown.
(10) The OPA454 was connected to sufficient heatsinking to prevent thermal shutdown.
(11) The OPA454 was connected to sufficient heatsinking to prevent thermal shutdown.

## TYPICAL CHARACTERISTICS (continued)

At $T_P$ = +25°C, $V_S$ = ±50V, and $R_L$ = 4.8kΩ connected to GND, unless otherwise noted.

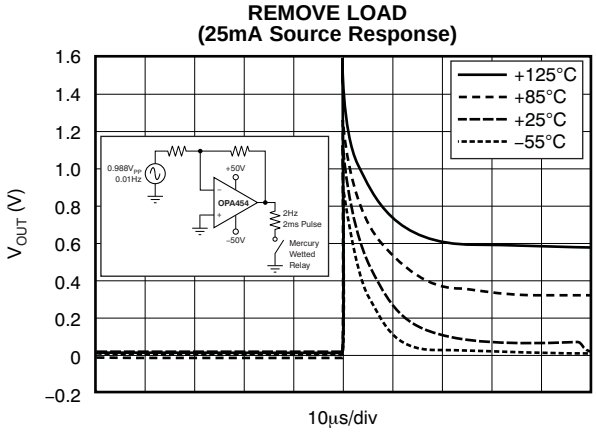



**Figure 54.**

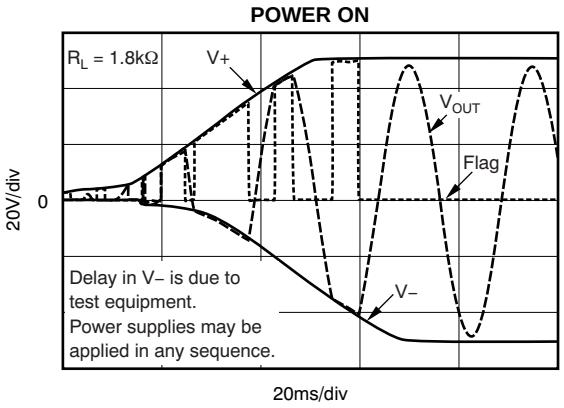



**Figure 55.**

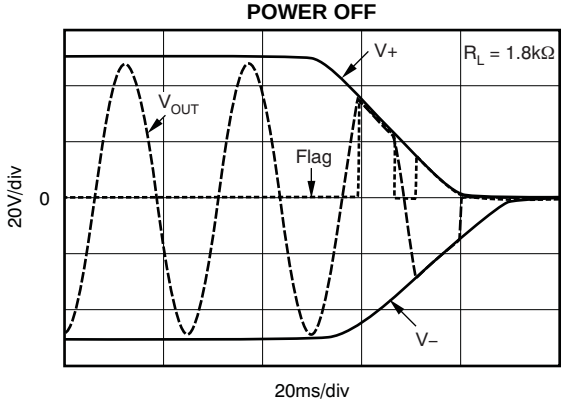
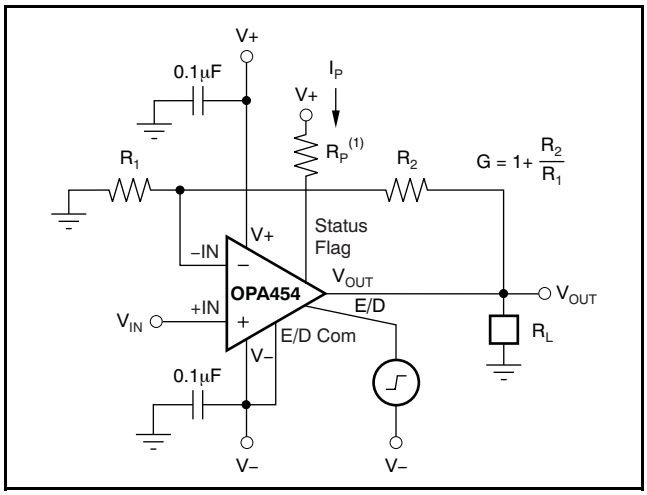



**Figure 56.**

## APPLICATIONS INFORMATION

Figure 57 shows the OPA454 connected as a basic noninverting amplifier. The OPA454 can be used in virtually any ±5V to ±50V op amp configuration. It is especially useful for supply voltages greater than 36V.

Power-supply terminals should be bypassed with 0.1µF (or greater) capacitors, located near the power-supply pins. Be sure that the capacitors are appropriately rated for the power-supply voltage used.




(1) Pull-up resistor with at least 10µA (choose $R_P$ = 1MΩ with V+ = 50V for $I_P$ = 50µA).

**Figure 57. Basic Noninverting Amplifier Configuration**

### POWER SUPPLIES

The OPA454 may be operated from power supplies up to ±50V or a total of 100V with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the Typical Characteristics.

Some applications do not require equal positive and negative output voltage swing. Power-supply voltages do not need to be equal. The OPA454 can operate with as little as 10V between the supplies and with up to 100V between the supplies. For example, the positive supply could be set to 90V with the negative supply at –10V, or vice-versa (as long as the total is less than or equal to 100V).

### INPUT PROTECTION

The OPA454 has increased protection against damage caused by excessive voltage between op amp input pins or input pin voltages that exceed the power supplies; external series resistance is not needed for protection. Internal series JFETs limit input overload current to a non-destructive 4mA, even with an input differential voltage as large as 120V. Additionally, the OPA454 has dielectric isolation between devices and the substrate. Therefore, the amplifier is free from the limitations of junction isolation common to many IC fabrication processes.

### LOWERING OFFSET VOLTAGE AND DRIFT

The OPA454 can be used with an OPA735 zero-drift series op amp to create a high-voltage op amp circuit that has very low input offset temperature drift. This circuit is shown in Figure 58.

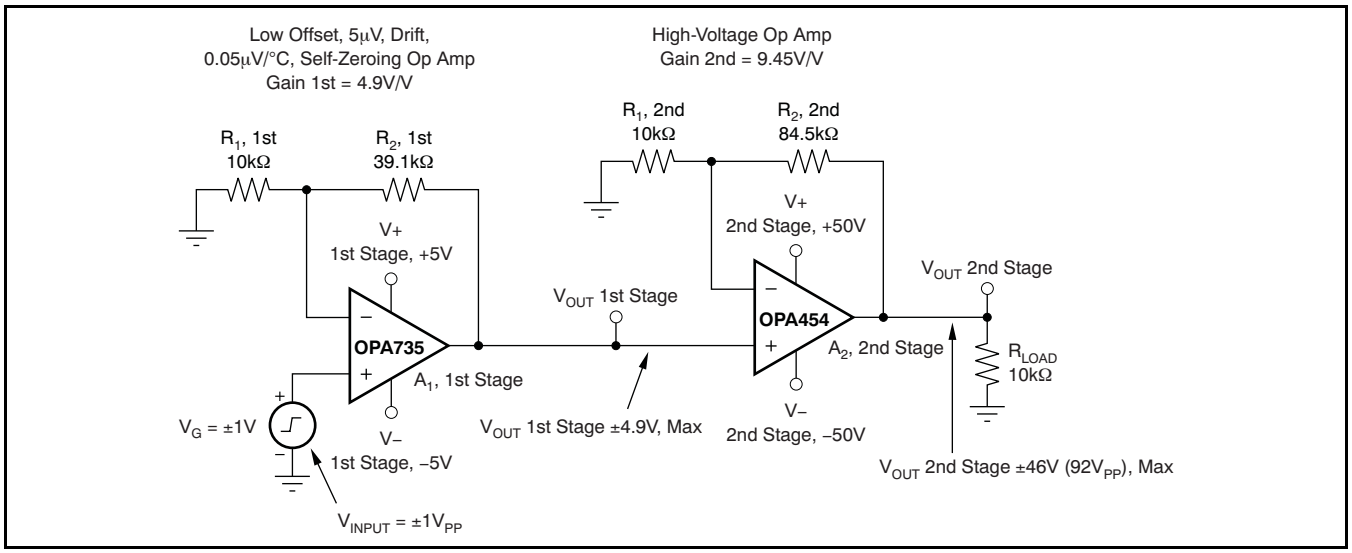
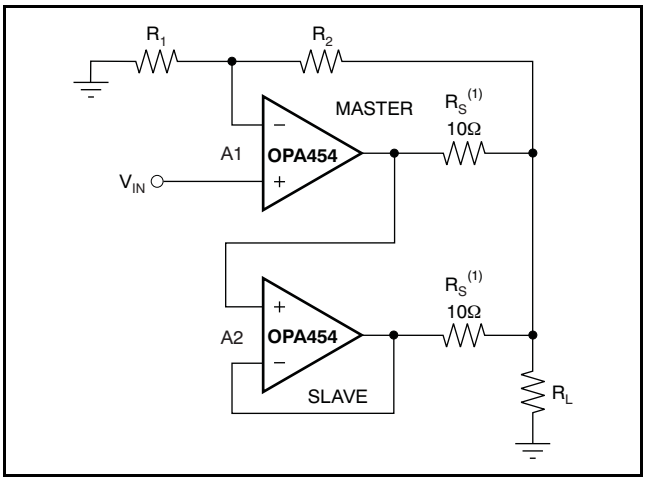



**Figure 58. Two-Stage, High-Voltage Op Amp Circuit With Very Low Input Offset Temperature Drift**

## INCREASING OUTPUT CURRENT

The OPA454 drives an output current of a few milliamps to greater than 50mA while maintaining good op amp performance. See Figure 7 for open-loop gain versus temperature at various output current levels.

In applications where the 25mA output current is not sufficient to drive the required load, the output current can be increased by connecting two or more OPA454s in parallel, as Figure 59 shows. Amplifier A1 is the master amplifier and may be configured in virtually any op amp circuit. Amplifier A2, the slave, is configured as a unity-gain buffer. Alternatively, external output transistors can be used to boost output current. The circuit in Figure 60 is capable of supplying output currents up to 1A, with the transistors shown.

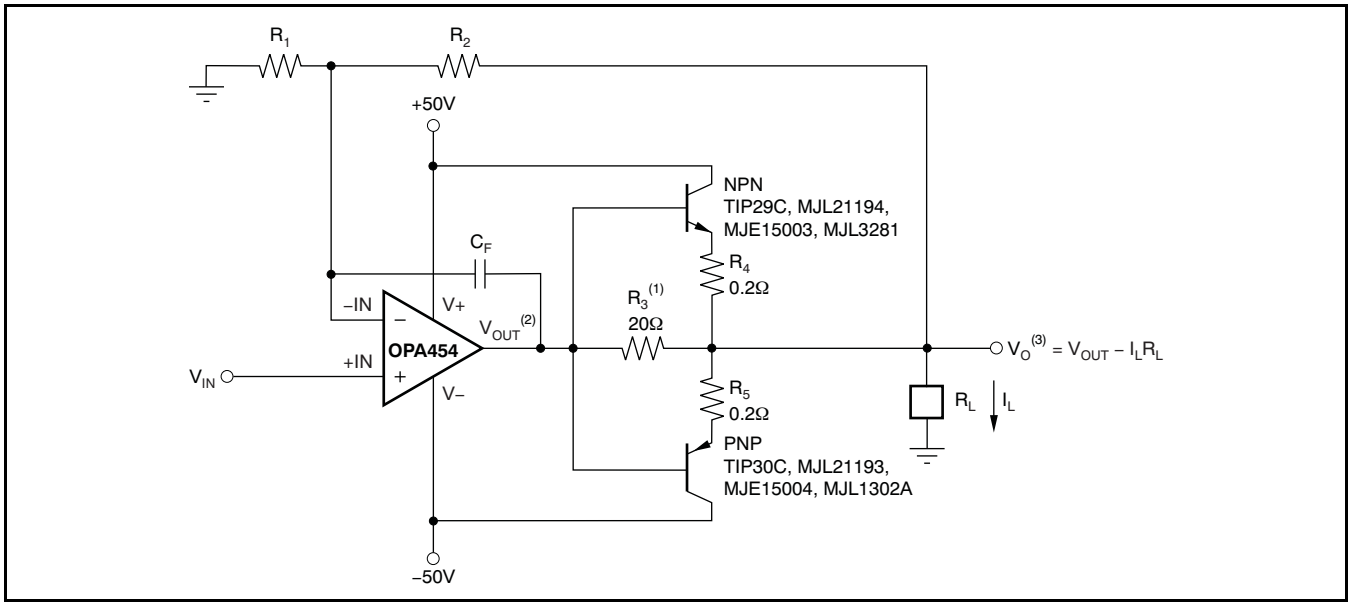



(1) $R_S$ resistors minimize the circulating current that always flows between the two devices because of $V_{OS}$ errors.

**Figure 59. Parallel Amplifiers Increase Output Current Capability**

## UNITY-GAIN NONINVERTING CONFIGURATION

When in the noninverting unity-gain configuration, the OPA454 has more gain peaking with increasing positive common-mode voltage and increasing temperature. It has less gain peaking with more negative common-mode voltage. As with all op amps, gain peaking increases with increasing capacitive load. A resistor and small capacitor placed in the feedback path can reduce gain peaking and increase stability.




(1) Provides current limit for OPA454 and allows the amplifier to drive the load when the output is between +0.7V and –0.7V.

(2) Op amp $V_{OUT}$ swings from +47V to –48V.

(3) $V_O$ swings from +44.1V to –45.1V at $I_L$ = 1A.

**Figure 60. External Output Transistors Boost Output Current Greater Than 1A**

## INPUT RANGE

The OPA454 is specified to give linear operation with input swing to within 2.5V of either supply. Generally, a gain of +1 is the most demanding configuration. Figure 61 and Figure 62 show output behavior as the input swings to within 0V of the rail, using the circuit shown in Figure 64. Figure 63 shows the behavior with an input signal that swings beyond the specified input range to within 1V of the rail, also using the circuit in Figure 64. Notice that the beginning of the phase reversal effect may be reduced by inserting series resistance ($R_S$) in the connection to the positive input. Note that $V_{OUT}$ does not swing all the way to the opposite rail.

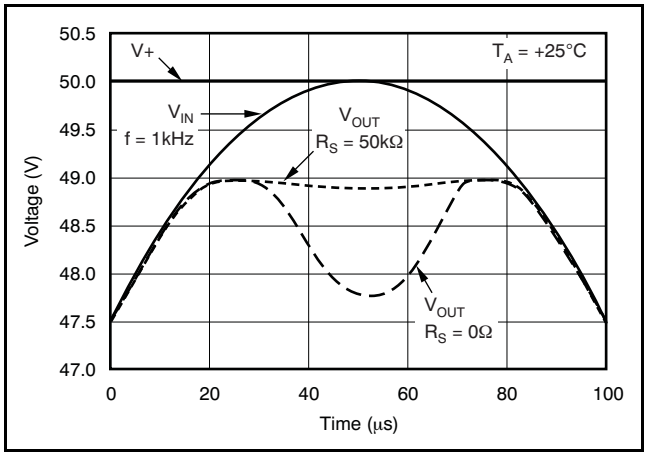



**Figure 61. Output Voltage With Input Voltage Up To V+**

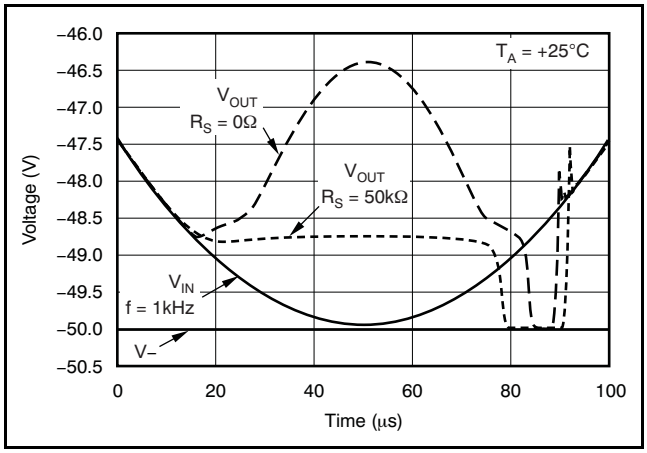



**Figure 62. Output Voltage With Input Voltage Down To V–**

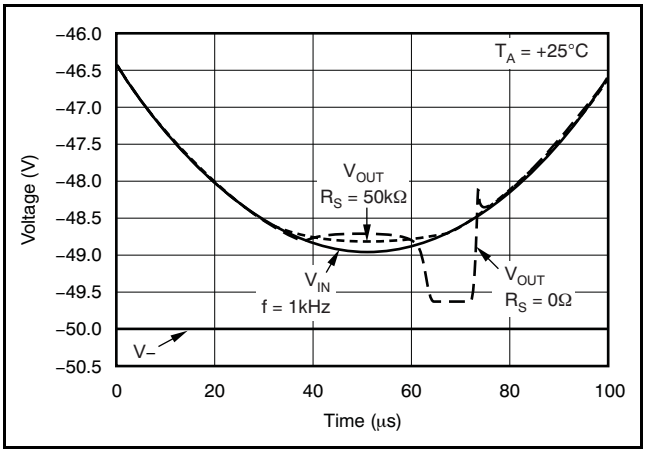



**Figure 63. Output Voltage With Input Voltage Down To (V–) + 1V**

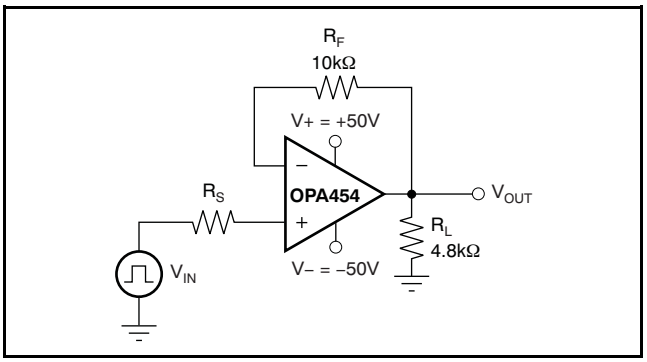



**Figure 64. Input Range Test Circuit**

## OUTPUT RANGE

The OPA454 is specified to swing to within 1V of either supply rail with a 49kΩ load while maintaining excellent linearity. Swing to the rail decreases with increasing output current. The OPA454 can swing to within 2V of the negative rail and 3V of the positive rail with a 1.88kΩ load. The typical characteristic curve, *Output Voltage Swing vs Output Current* (Figure 11), shows this behavior in detail.

## OPEN-LOOP GAIN LINEARITY

Figure 65 shows the nonlinear relationship of $A_{OL}$ and output voltage. As Figure 65 shows, open-loop gain is lower with positive output voltage levels compared to negative voltage levels. Specifications in the Electrical Characteristics table are based upon the average gain measured at both output extremes.

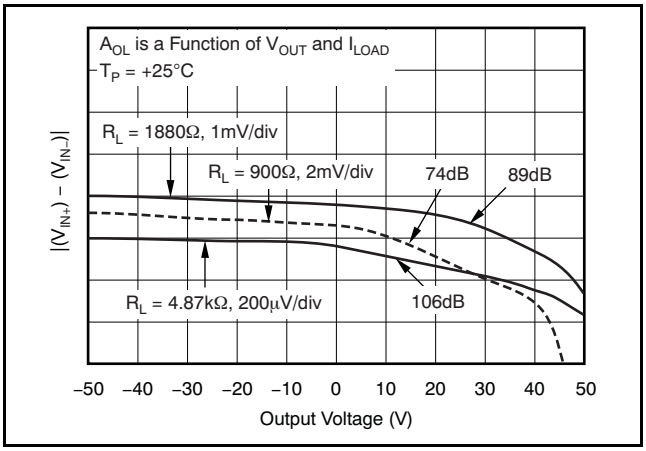



**Figure 65. Differential Input Voltage (+IN to –IN) versus Output Voltage**

## SETTLING TIME

The circuit in Figure 66 is used to measure the settling time response. The left half of the circuit is a standard, false-summing junction test circuit used for settling time and open-loop gain measurement. $R_1$ and $R_2$ provide the gain and allow for measurement without connecting a scope probe directly to the summing junction, which can disturb proper op amp function by causing oscillation.

The right half of the circuit looks at the combination of both inverting and noninverting responses. $R_5$ and $R_6$ remove the large step response. The remaining voltage at $V_2$ shows the small-signal settling time that is centered on zero. This test circuit can be used for incoming inspection, real-time measurement, or in designing compensation circuits in system applications.

**Table 2. Settling Time Measurement Circuit Configuration Using Different Gain Settings for Figure 66**

| | GAIN | | |
|---|---|---|---|
| COMPONENT | 1 | 5 | 10 |
| $R_1$ (Ω) | 10k | 2k | 1k |
| $R_3$ (Ω) | 10k | 2k | 1k |
| $R_7$ (Ω) | 10k | 4k | 9k |
| $R_8$ (Ω) | ∞ | 1k | 1k |
| $V_{IN}$ ($V_{PP}$) | 20 | 16 | 8 |

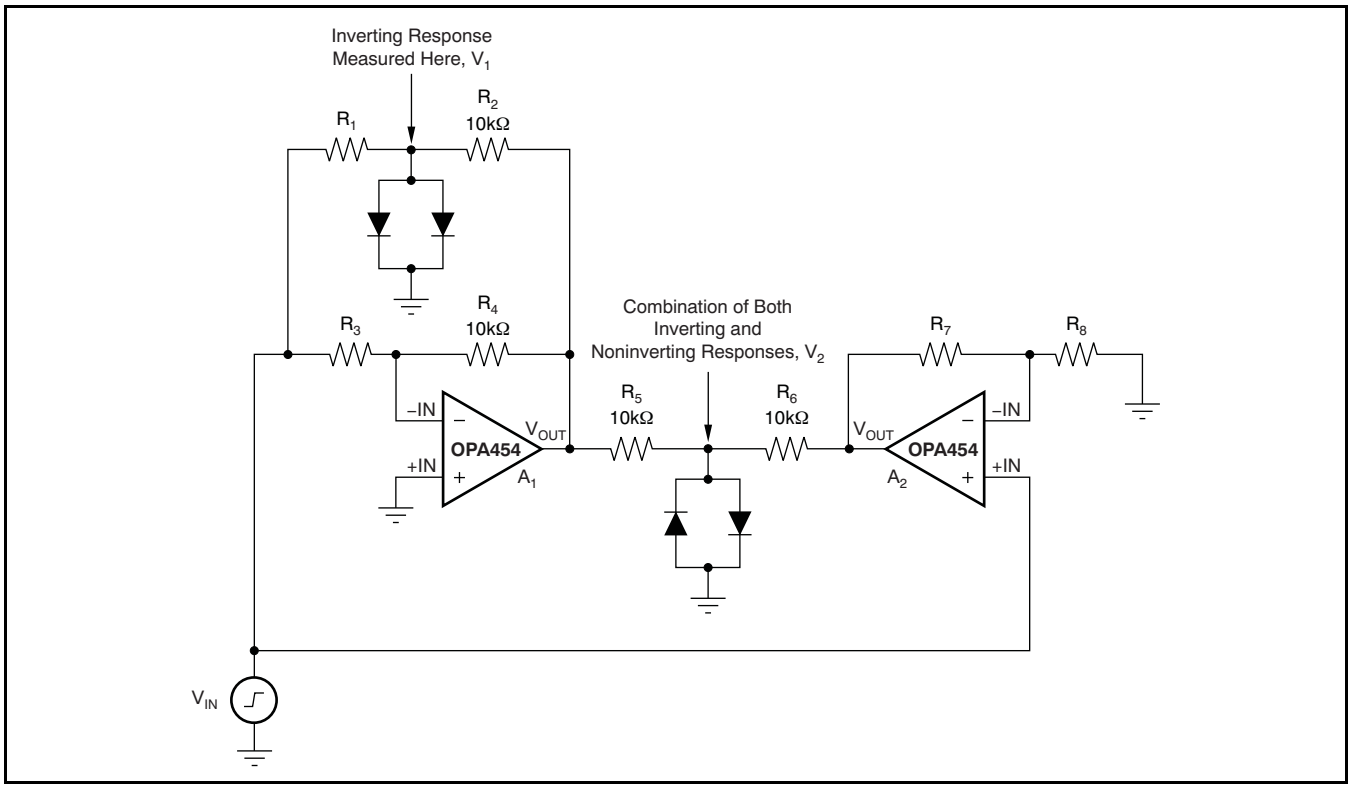



**Figure 66. Settling Time Test Measurement Circuit**

## ENABLE AND E/D Com

If left disconnected, E/D Com is pulled near V– (negative supply) by an internal 10µA current source. When left floating, ENABLE is held approximately 2V above E/D Com by an internal 1µA source. Even though active operation of the OPA454 results when the ENABLE and E/D Com pins are not connected, a moderately fast, negative-going signal capacitively coupled to the ENABLE pin can overpower the 1µA pull-up current and cause device shutdown. This behavior can appear as an oscillation and is encountered first near extreme cold temperatures. If the enable function is not used, a conservative approach is to connect ENABLE through a 30pF capacitor to a low impedance source. Another alternative is the connection of an external current source from V+ (positive supply) sufficient to hold the enable level above the shutdown threshold. Figure 67 shows a circuit that connects ENABLE and E/D Com. Choosing $R_P$ to be 1MΩ with a +50V positive power supply voltage results in $I_P$ = 50µA.

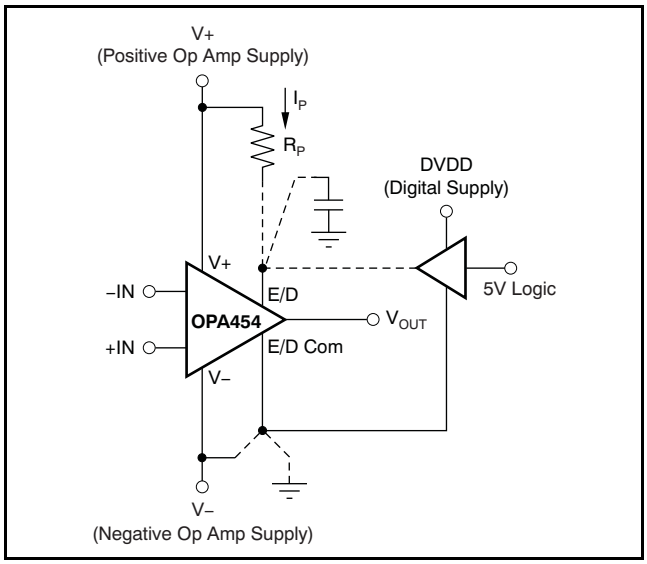



**Figure 67. ENABLE and E/D Com**

## CURRENT LIMIT

Figure 24 and Figure 48 to Figure 50 show the current limit behavior of the OPA454. Current limiting is accomplished by internally limiting the drive to the output transistors. The output can supply the limited current continuously, unless the die temperature rises to +150°C, which initiates thermal shutdown. With adequate heat-sinking, and use of the lowest possible supply voltage, the OPA454 can remain in current limit continuously without entering thermal shutdown. Although qualification studies have shown minimal parametric shifts induced by 400 hours of thermal shutdown cycling, this mode of operation should be avoided to maximize reliability. It is always best to provide proper heat-sinking (either by a physical plate or by airflow) to remain considerably below the thermal shutdown threshold. For longest operational life of the device, keep the junction temperature below +125°C.

## THERMAL PROTECTION

Figure 68 shows the thermal shutdown behavior of a socketed OPA454 that internally dissipates 1W. Unsoldered and in a socket, $\theta_{JA}$ of the DDA package is typically +128°C/W. With the socket at +25°C, the output stage temperature rises to the shutdown temperature of +150°C, which triggers automatic thermal shutdown of the device. The device remains in thermal shutdown (output is in a high-impedance state) until it cools to +130°C where it again is powered. This thermal protection hysteresis feature typically prevents the amplifier from leaving the safe operating area, even with a direct short from the output to ground or either supply. The rail-to-rail supply voltage at which catastrophic breakdown occurs is typically 135V at +25°C. However, the absolute maximum specification is 120V, and the OPA454 should not be allowed to exceed 120V under any condition. Failure as a result of breakdown, caused by spiking currents into inductive loads (particularly with elevated supply voltage), is not prevented by the thermal protection architecture.

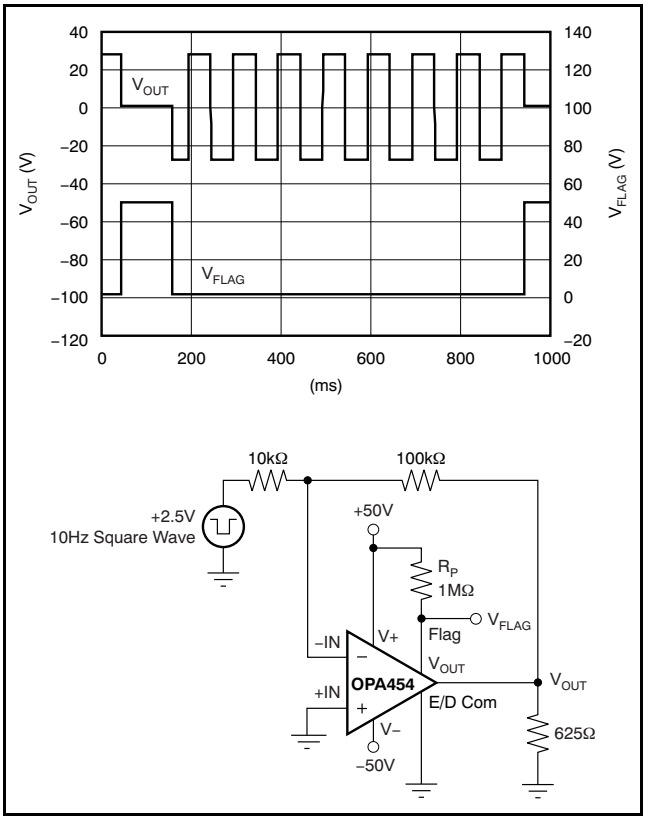


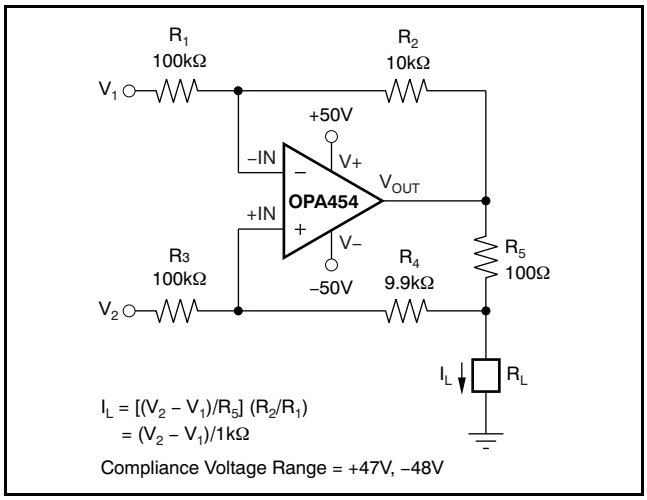

**Figure 68. Thermal Shutdown**

## POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of the output current times the voltage across the conducting output transistor, $P_D = I_L (V_S - V_O)$. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power-supply voltage. Dissipation with ac signals is lower because the root-mean square (RMS) value determines heating. Application Bulletin SBOA022 explains how to calculate or measure dissipation with unusual loads or signals. For constant current source circuits, maximum power dissipation occurs at the minimum output voltage, as Figure 69 shows.

The OPA454 can supply output currents of 25mA and larger. Supplying this amount of current presents no problem for some op amps operating from ±15V supplies. However, with high supply voltages, internal power dissipation of the op amp can be quite high. Operation from a single power supply (or unbalanced power supplies) can produce even greater power dissipation because a large voltage is impressed across the conducting output transistor. Applications with high power dissipation may require a heatsink, or heat spreader.




NOTE: $R_1 = R_3$ and $R_2 = R_4 + R_5$.

**Figure 69. Precision Voltage-to-Current Converter with Differential Inputs**

## HEATSINKING

Power dissipated in the OPA454 causes the junction temperature to rise. For reliable operation, junction temperature should be limited to +125°C, maximum. Maintaining a lower junction temperature always results in higher reliability. Some applications require a heatsink to assure that the maximum operating junction temperature is not exceeded. Junction temperature can be determined according to Equation 1:

$$T_J = T_A + P_D \theta_{JA} \quad (1)$$

Package thermal resistance, $\theta_{JA}$, is affected by mounting techniques and environments. Poor air circulation and use of sockets can significantly increase thermal resistance to the ambient environment. Many op amps placed closely together also increase the surrounding temperature. Best thermal performance is achieved by soldering the op amp onto a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Increasing circuit board copper area to approximately $0.5in^2$ decreases thermal resistance; however, minimal improvement occurs beyond $0.5in^2$, as shown in Figure 70.

For additional information on determining heatsink requirements, consult Application Bulletin SBOA021 (available for download at www.ti.com).

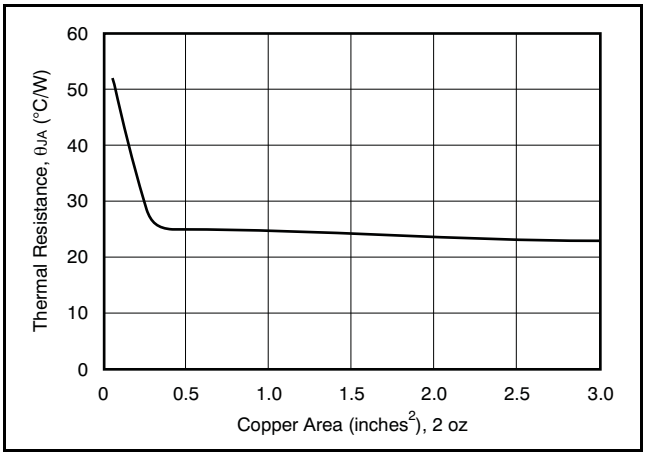



**Figure 70. Thermal Resistance versus Circuit Board Copper Area**

## PowerPAD THERMALLY-ENHANCED PACKAGES

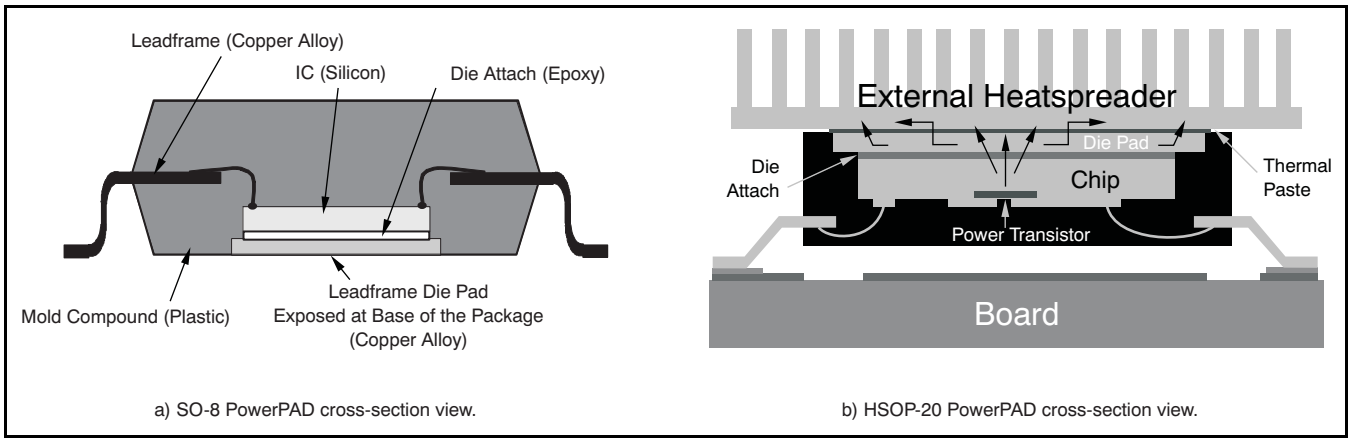
The OPA454 comes in SO-8 and HSOP-20 PowerPAD versions that provide an extremely low thermal resistance ($\theta_{JC}$) path between the die and the exterior of the package. These packages feature an exposed thermal pad. This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

## TOP-SIDE PowerPAD PACKAGE

The OPA454 DWD, HSOP-20, PowerPAD package has the exposed pad on the top side of the package, as Figure 71b shows. The top-side thermal pad can be used with commercially available heat-sinks and moving air to dissipate heat. The use of an external top-side heat-sink increases the effective surface area of the package face, which increases convection and radiation off the top surface of the package. Top-side heatsinking also avoids unnecessary heating of the printed circuit board (PCB), and permits installation of other PCB components onto the side opposite of the OPA454.

## BOTTOM-SIDE PowerPAD PACKAGE

The OPA454 SO-8 PowerPAD is a standard-size SO-8 package constructed using a downset leadframe upon which the die is mounted, as Figure 71a shows. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB. This architecture enhances the OPA454 power dissipation capability significantly, eliminates the use of bulky heatsinks and slugs traditionally used in thermal packages, and allows the OPA454 to be easily mounted using standard PCB assembly techniques. NOTE: Because the SO-8 PowerPAD is pin-compatible with standard SO-8 packages, the OPA454 is a drop-in replacement for operational amplifiers in existing sockets. Soldering the bottom-side PowerPAD to the PCB is always required, even with applications that have low power dissipation. Soldering the device to the PCB provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.




a) SO-8 PowerPAD cross-section view.

b) HSOP-20 PowerPAD cross-section view.

**Figure 71. Cross-Section Views of a PowerPAD Package**

## BOTTOM-SIDE PowerPAD LAYOUT GUIDELINES

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. Follow these steps to attach the device to the PCB:

1. The PowerPAD must be connected to the most negative supply voltage on the device, V–.
2. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
3. Use of thermal vias improves heat dissipation, but are not required. The thermal pad can connect to the PCB using an area equal to the pad size with no vias, but externally connected to V–.
4. Place recommended holes in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SO-8 DDA package are shown in the thermal land pattern mechanical drawing appended at the end of this document. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the SO-8 PowerPAD package is five.
5. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA454 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
6. Connect all holes to the internal power plane of the correct voltage potential (V–).
7. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA454 PowerPAD package should make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
8. The top-side solder mask should leave the terminals of the package and the thermal pad area exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
9. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
10. With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see technical brief SLMA002 PowerPAD Thermally-Enhanced Package, available for download at www.ti.com.

## TYPICAL APPLICATIONS

Figure 72 and Figure 73 illustrate the OPA454 in a programmable voltage source and a bridge circuit, respectively.

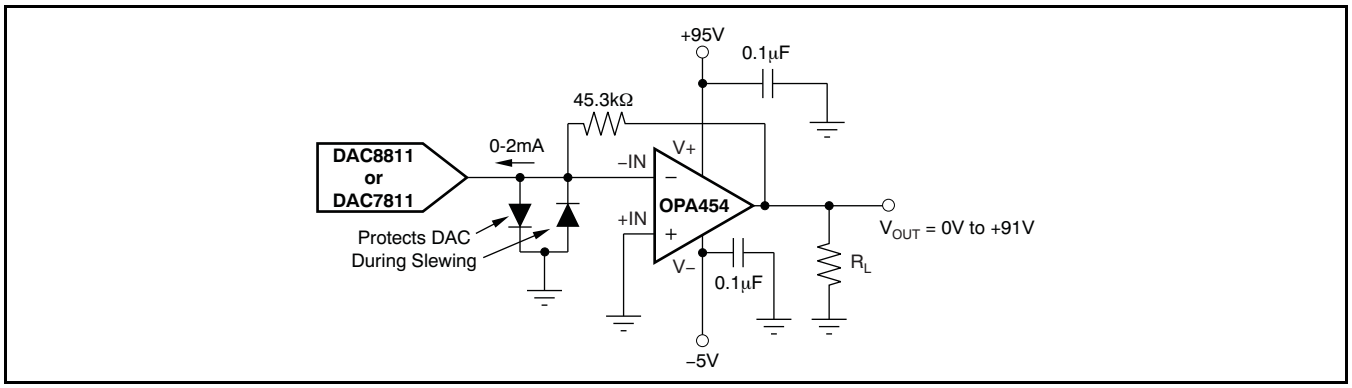
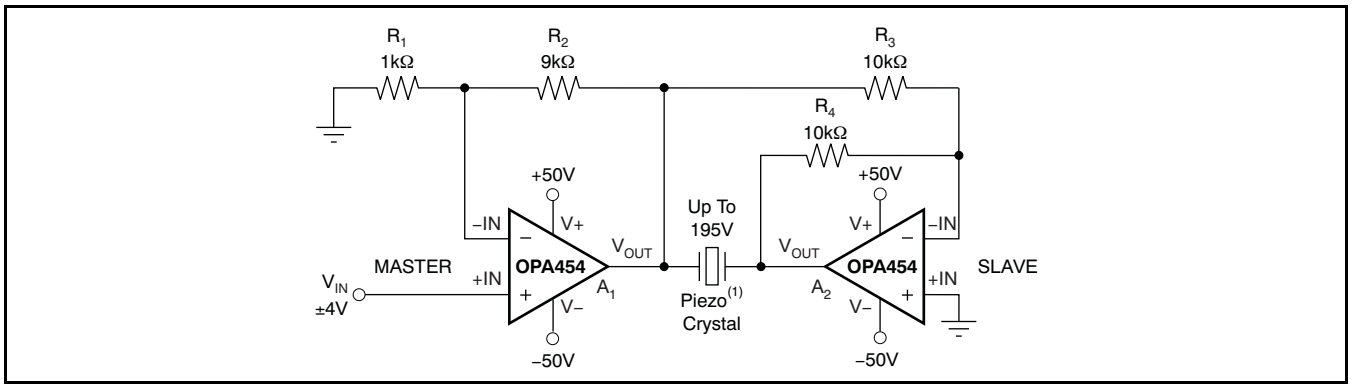



**Figure 72. Programmable Voltage Source**



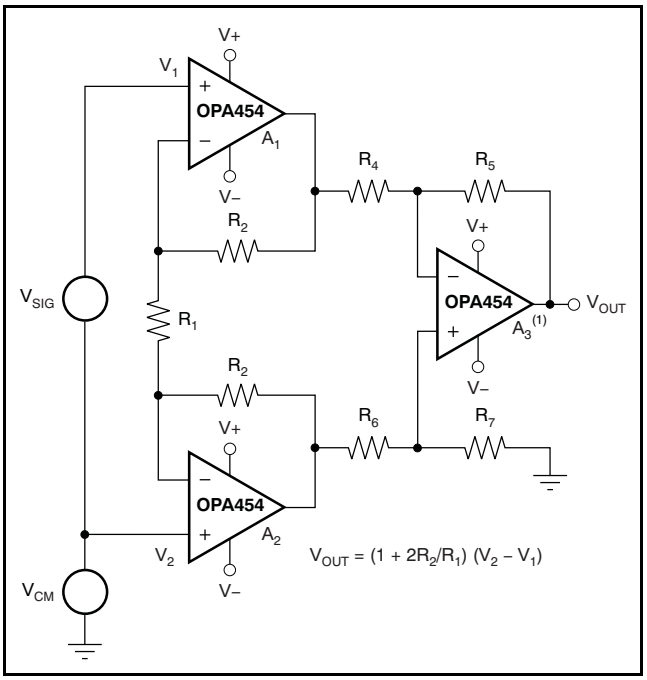

(1) For transducers with large capacitance, stabilization may become an issue. Be certain that the *Master* amplifier is stable before stabilizing the *Slave* amplifier.

**Figure 73. Bridge Circuit Doubles Voltage for Exciting Piezo Crystals**

Figure 74 uses three OPA454s to create a high-voltage instrumentation amplifier. $V_{CM}$ ± $V_{SIG}$ must be between (V–) + 2.5V and (V+) – 2.5V. The maximum supply voltage equals ±50V or 100V total.

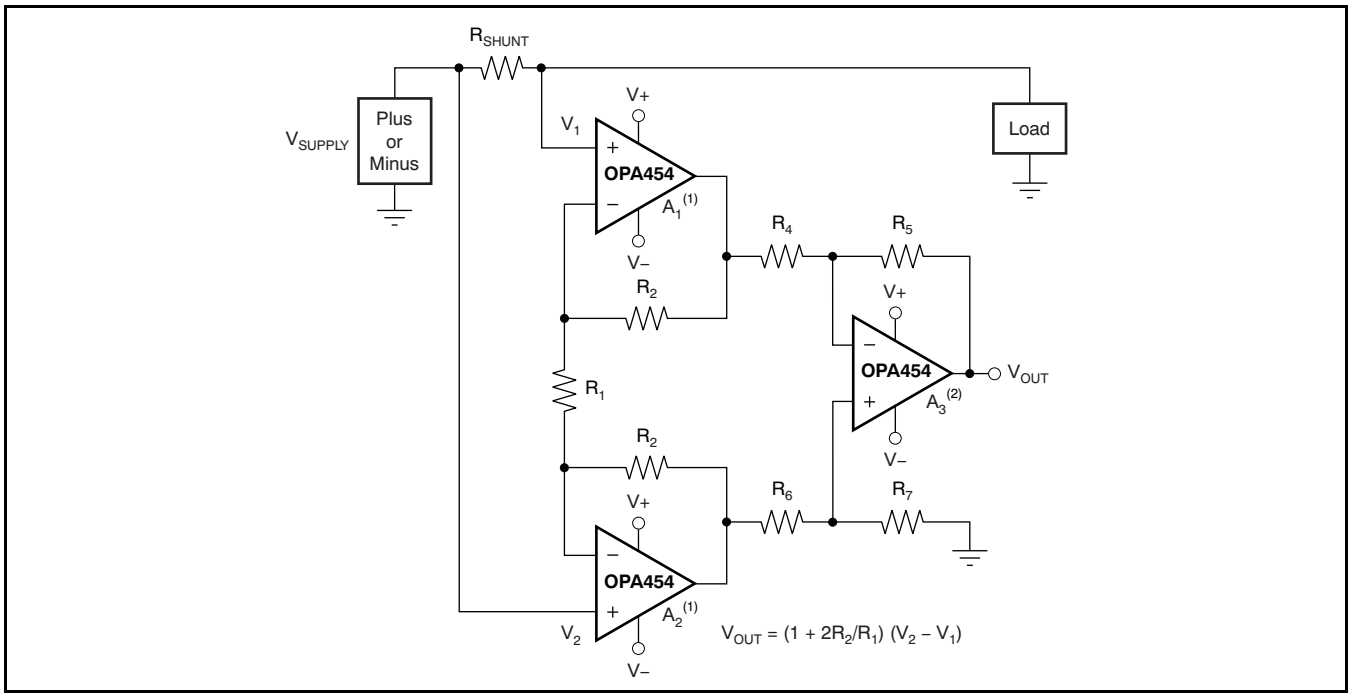
Figure 75 uses three OPA454s to measure current in a high-side shunt application. $V_{SUPPLY}$ must be greater than $V_{CM}$. $V_{CM}$ must be between (V–) + 2.5V and (V+) – 2.5V. Adhering to these restrictions keeps $V_1$ and $V_2$ within the voltage range required for linear operation of the OPA454. For example, if V+ = 50V and V– = 50V, then $V_1$ = +47.5V (maximum) and $V_2$ = –47.5V (minimum). The maximum supply voltage equals ±50V, or 100V total.

See Figure 76 and Figure 79 for example circuits that use the OPA454 in an output voltage boost configurations in three and six op amp output stages, respectively.




(1) The linear input range is limited by the output swing on the input amplifiers, $A_1$ and $A_2$.

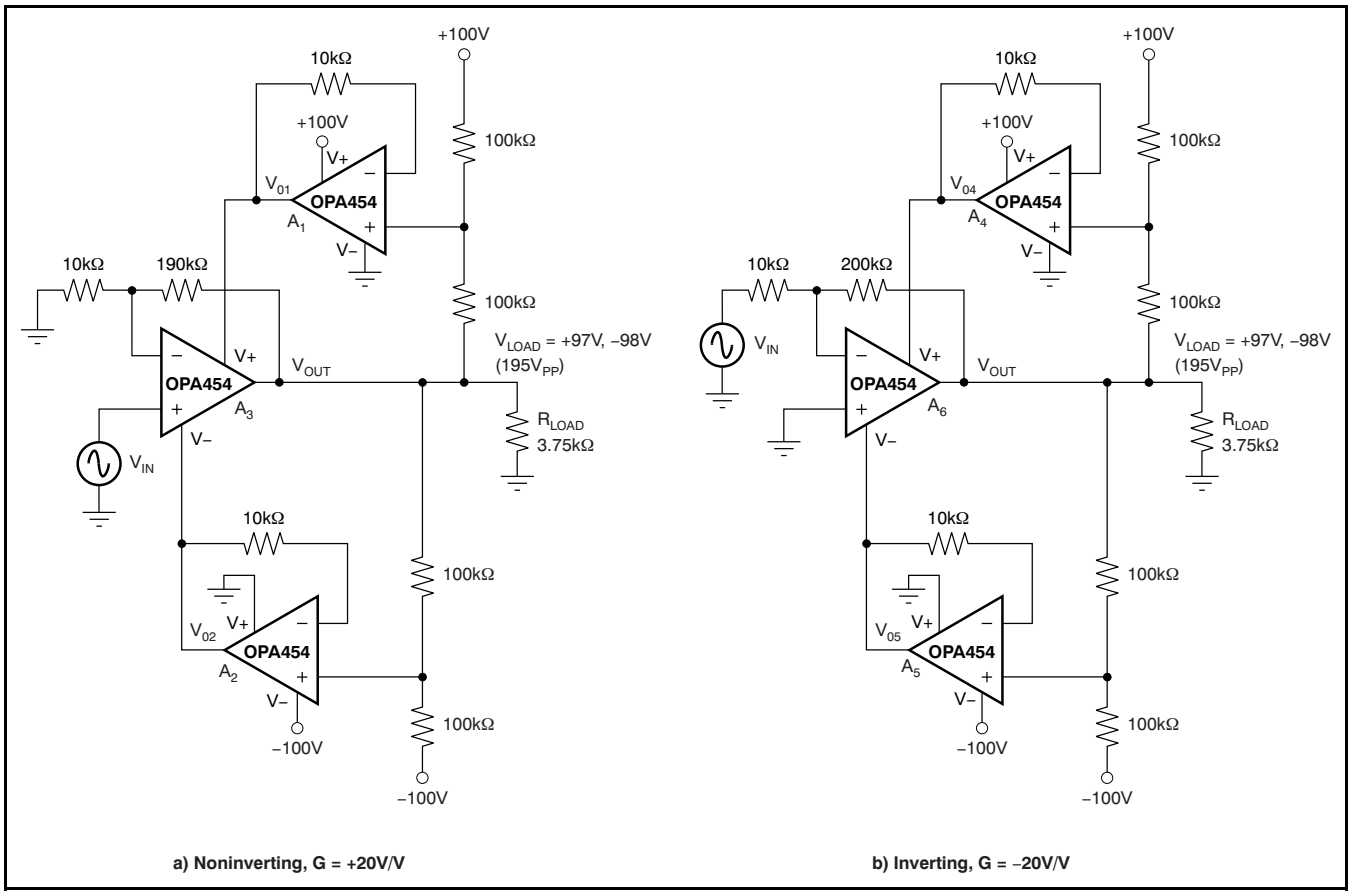
**Figure 74. High-Voltage Instrumentation Amplifier**




(1) To increase the linear input voltage range, configure $A_1$ and $A_2$ as unity-gain followers.

(2) The linear input range is limited by the output swing on the input amplifiers, $A_1$ and $A_2$.

**Figure 75. High-Voltage Instrumentation Amplifier for Measuring High-Side Shunt**




a) Noninverting, G = +20V/V

b) Inverting, G = –20V/V

**Figure 76. Output Voltage Boost With +97V, –98V ($195V_{PP}$) Across Load Connected to Ground (3 Op Amp Output Stage, see Figure 77 and Figure 78)**

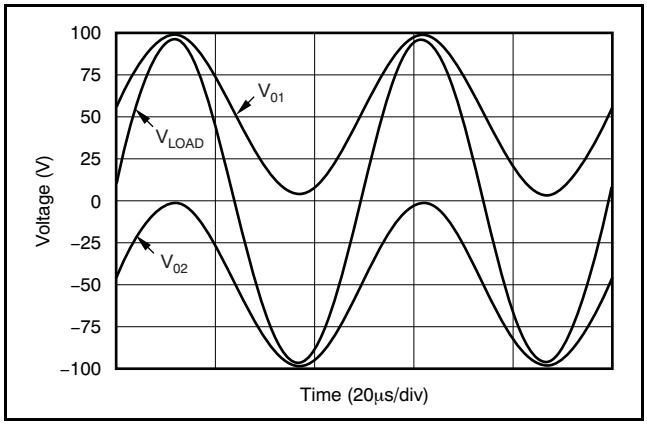



**Figure 77. $195V_{PP}$ On 3.75kΩ Load to Ground 20kHz, Uses 3 OPA454s, 100V Supplies**

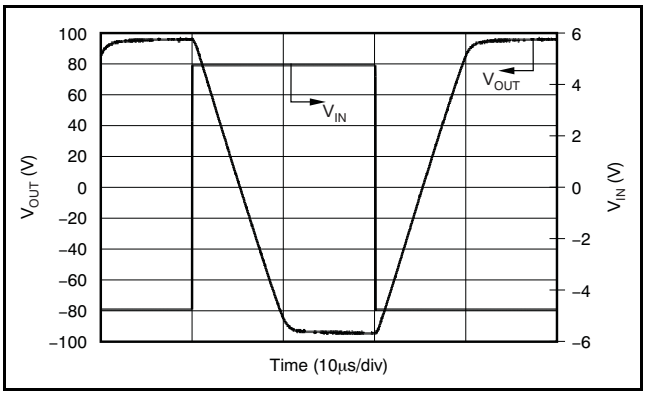



**Figure 78. 3.75kΩ Load to Ground G = +20, 3 OPA454s, 100V Supplies (Note SR of 18V/µs, which is slightly higher than the specified 13V/µs due to tracking of the power-supply voltage)**

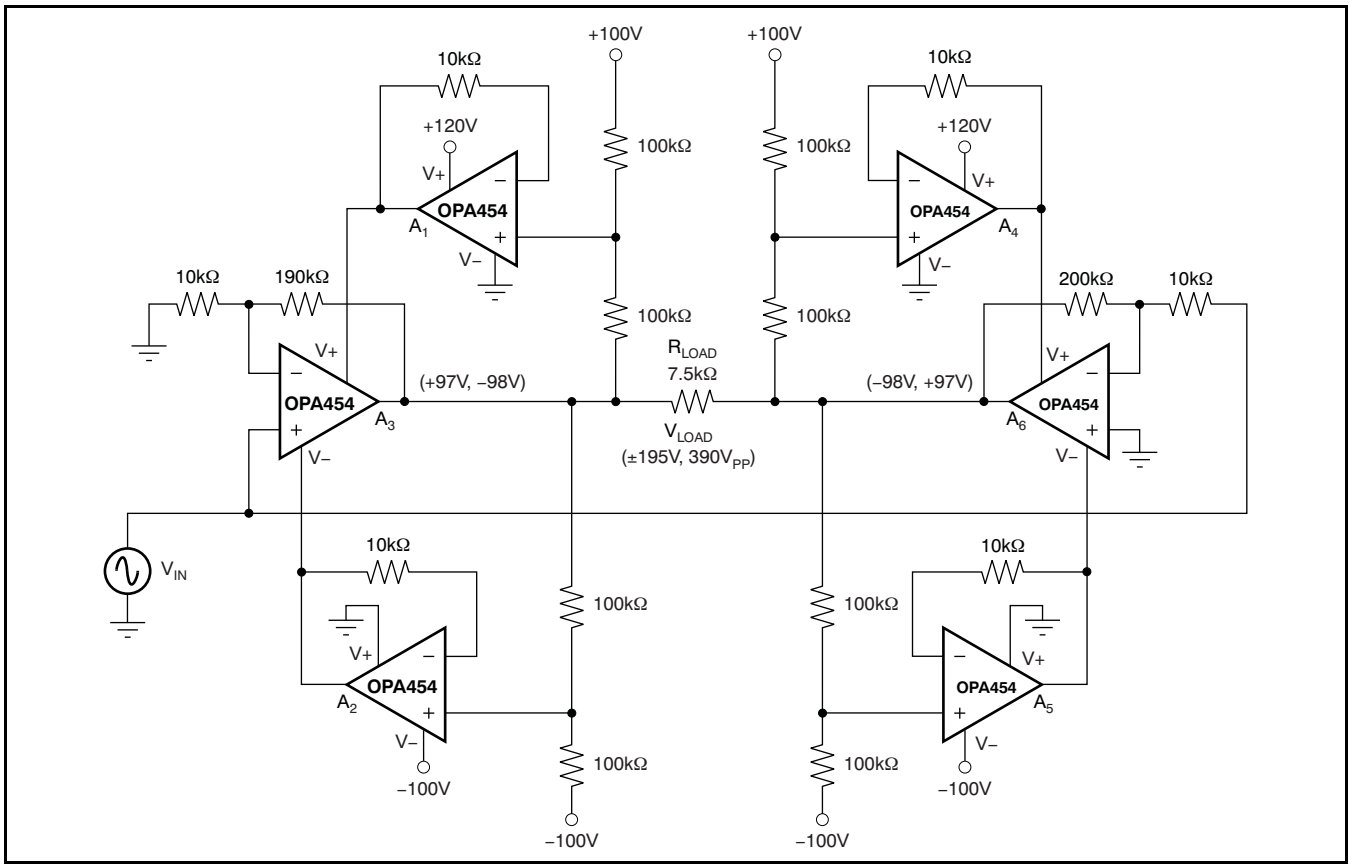



**Figure 79. Output Voltage Boost With ±195V ($390V_{PP}$) Across Bridge-Tied Load (6 Op Amps, see Figure 80 and Figure 81)**

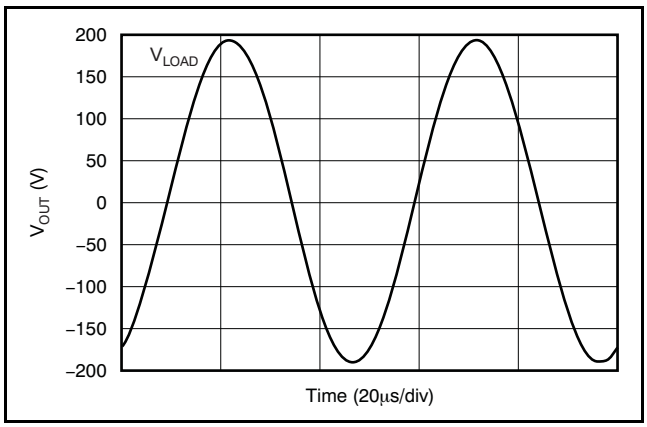



**Figure 80. $390V_{PP}$ Across 7.5kΩ Load 20kHz, Uses 6 OPA454s, 100V Supplies**

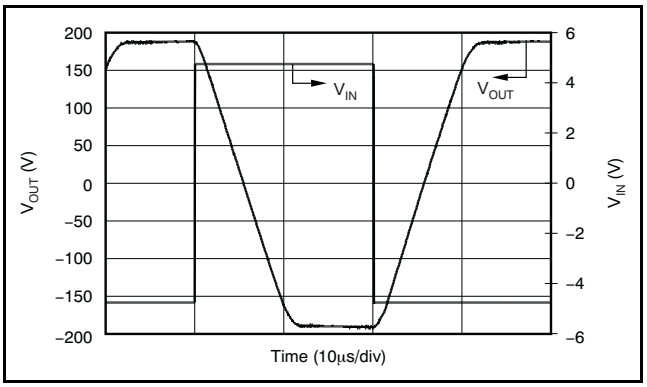



**Figure 81. 7.5kΩ Load G = +20, 6 OPA454s, 100V Supplies (Note SR of 34V/µs, which is significantly higher than the specified 13V/µs due to tracking of the power-supply voltage)**

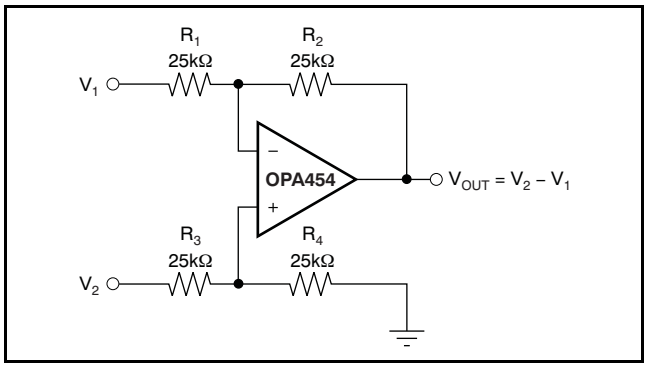



**Figure 82. High-Voltage Difference Amplifier**

## HIGH-COMPLIANCE VOLTAGE CURRENT SOURCES

This section describes four different applications utilizing high compliance voltage current sources with differential inputs. Figure 69 and Figure 83 illustrate the different applications.

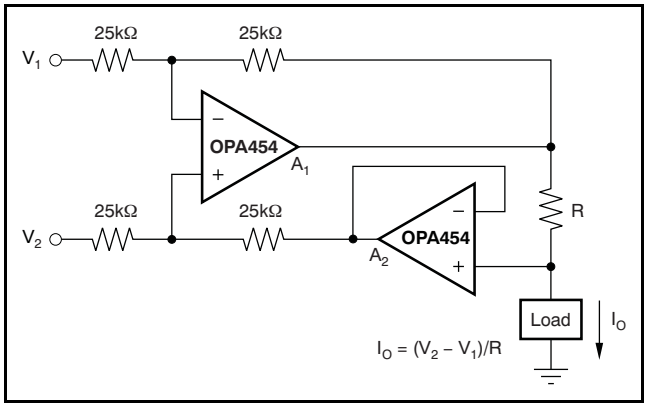



**Figure 83. Differential Input Voltage-to-Current Converter for Low $I_{OUT}$**

A red light emitting diode (LED) was used to generate Figure 84.

Gain of the avalanche photodiode (APD) is adjusted by changing the voltage across the APD. Gain starts to increase when reverse voltage is increased beyond 130V for this API diode. Figure 85 shows this structure.

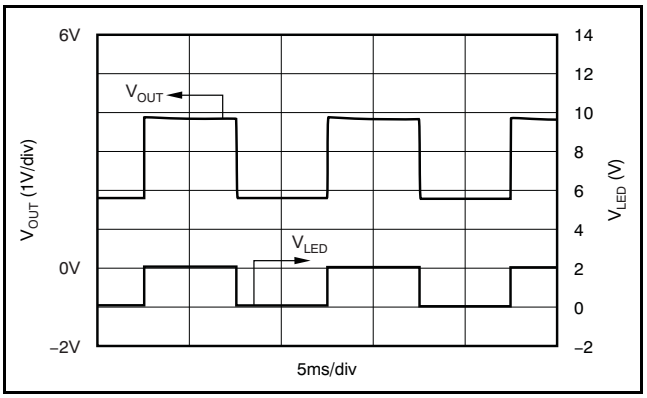



**Figure 84. Avalanche Photodiode Circuit**

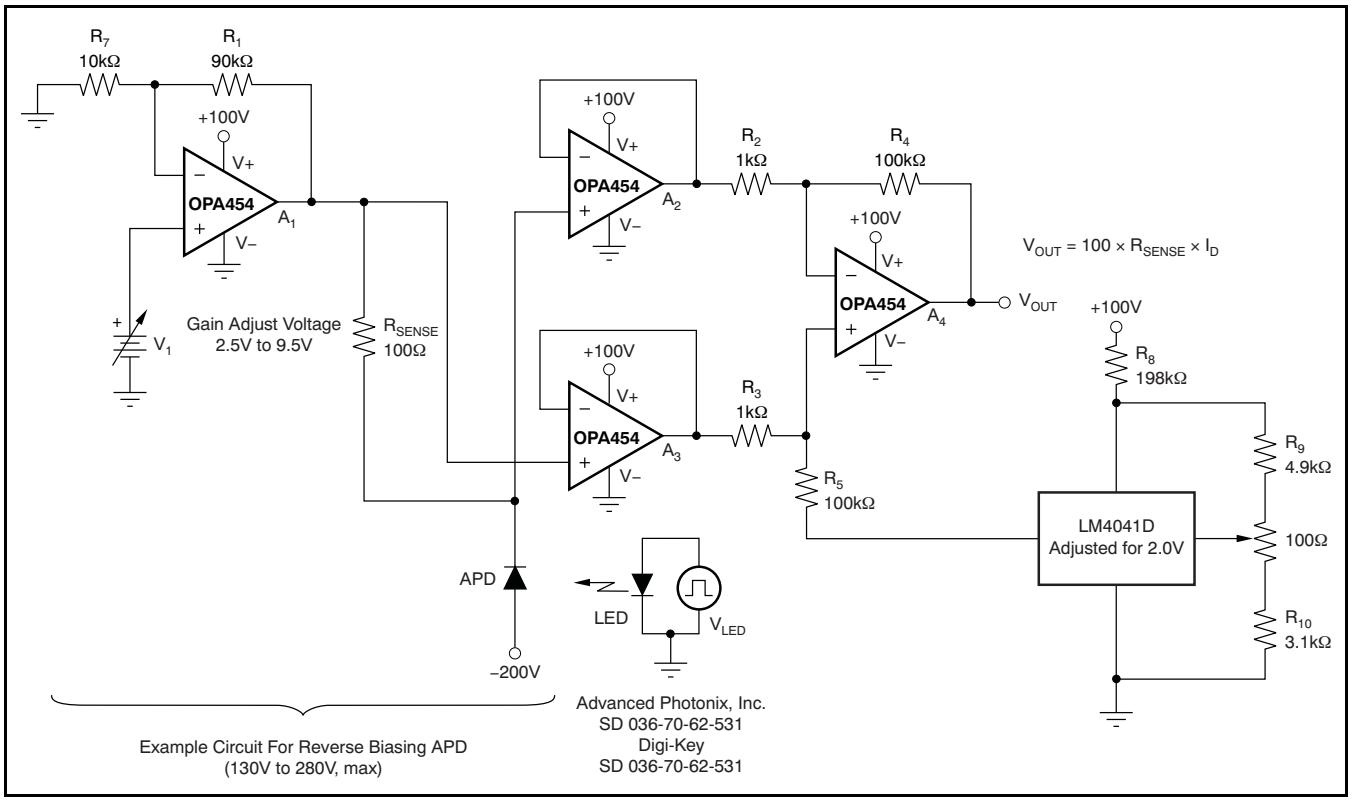



**Figure 85. APD Gain Adjustment Using the OPA454, High-Voltage Op Amp**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| OPA454AIDDA | ACTIVE | SO Power PAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA454AIDDAR | ACTIVE | SO Power PAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA454AIDWD | PREVIEW | HSOP | DWD | 20 | 75 | TBD | Call TI | Call TI |
| OPA454AIDWDR | PREVIEW | HSOP | DWD | 20 | 2000 | TBD | Call TI | Call TI |

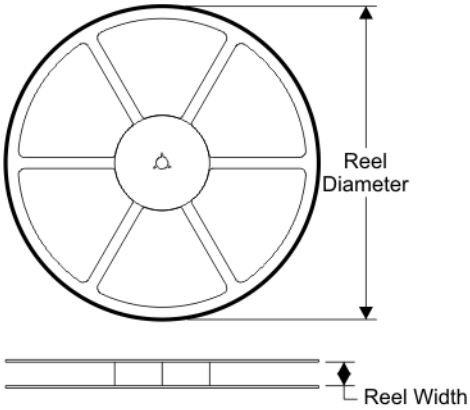
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

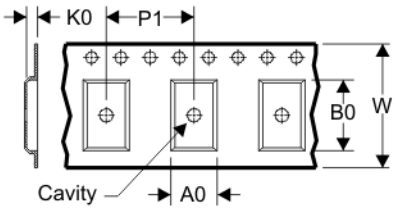
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL BOX INFORMATION

**REEL DIMENSIONS**

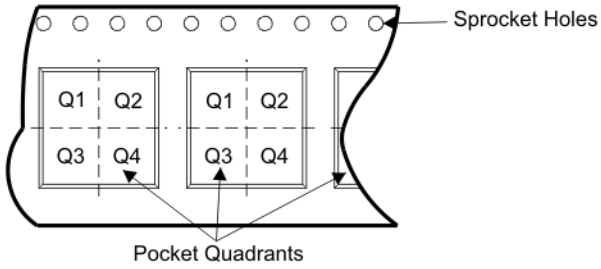



**TAPE DIMENSIONS**



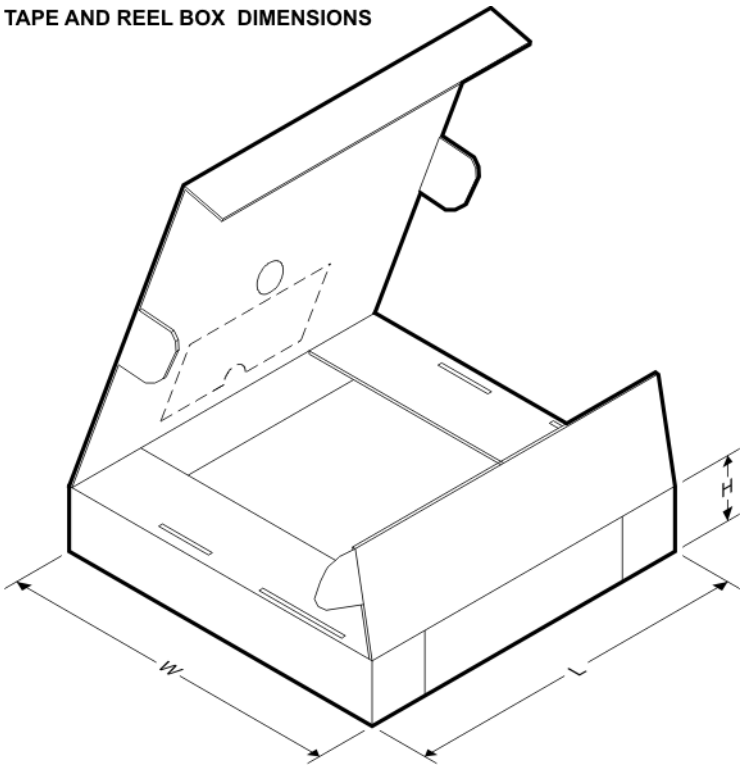

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA454AIDDAR | DDA | 8 | SITE 41 | 330 | 12 | 6.4 | 5.2 | 2.1 | 8 | 12 | Q1 |

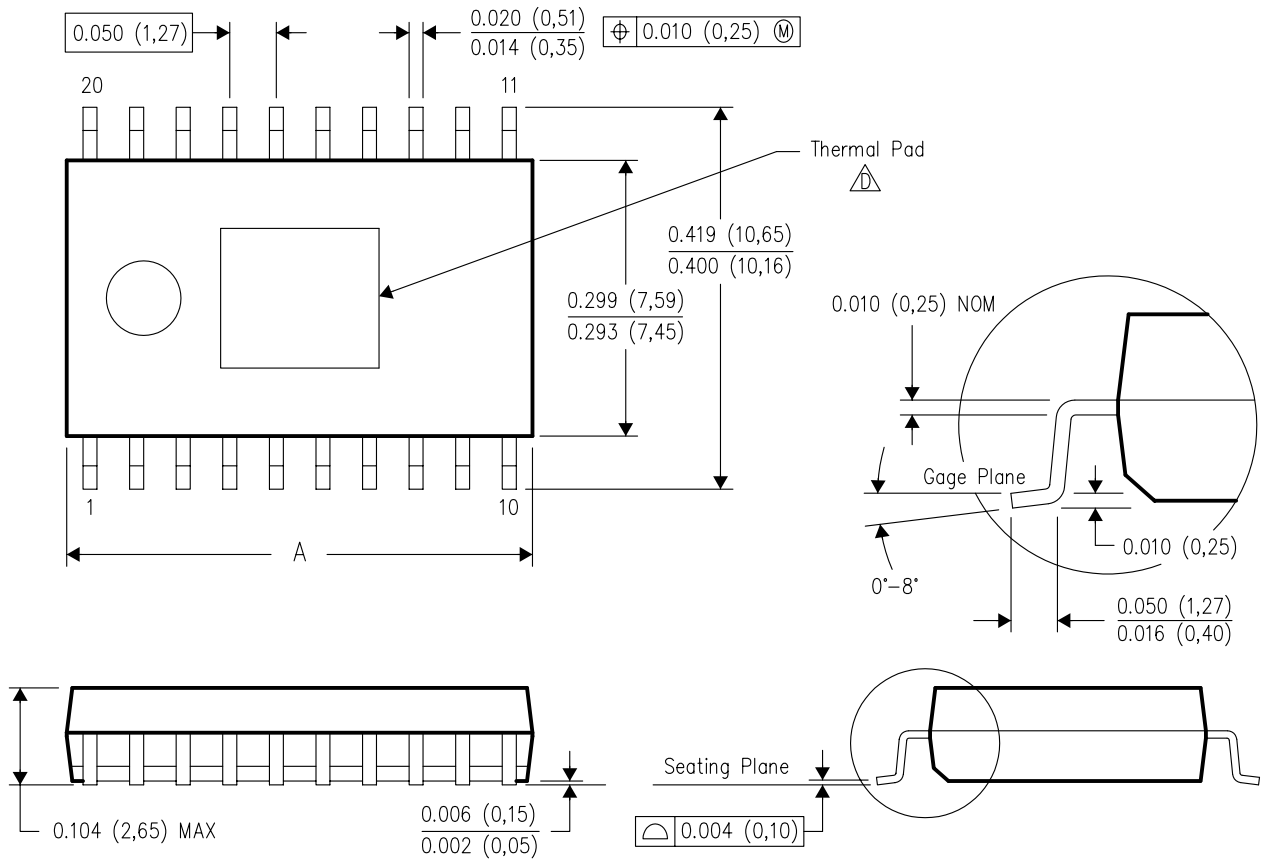
**TAPE AND REEL BOX DIMENSIONS**




| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| OPA454AIDDAR | DDA | 8 | SITE 41 | 346.0 | 346.0 | 29.0 |

## DWD (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE (DIE DOWN)

20 PINS SHOWN

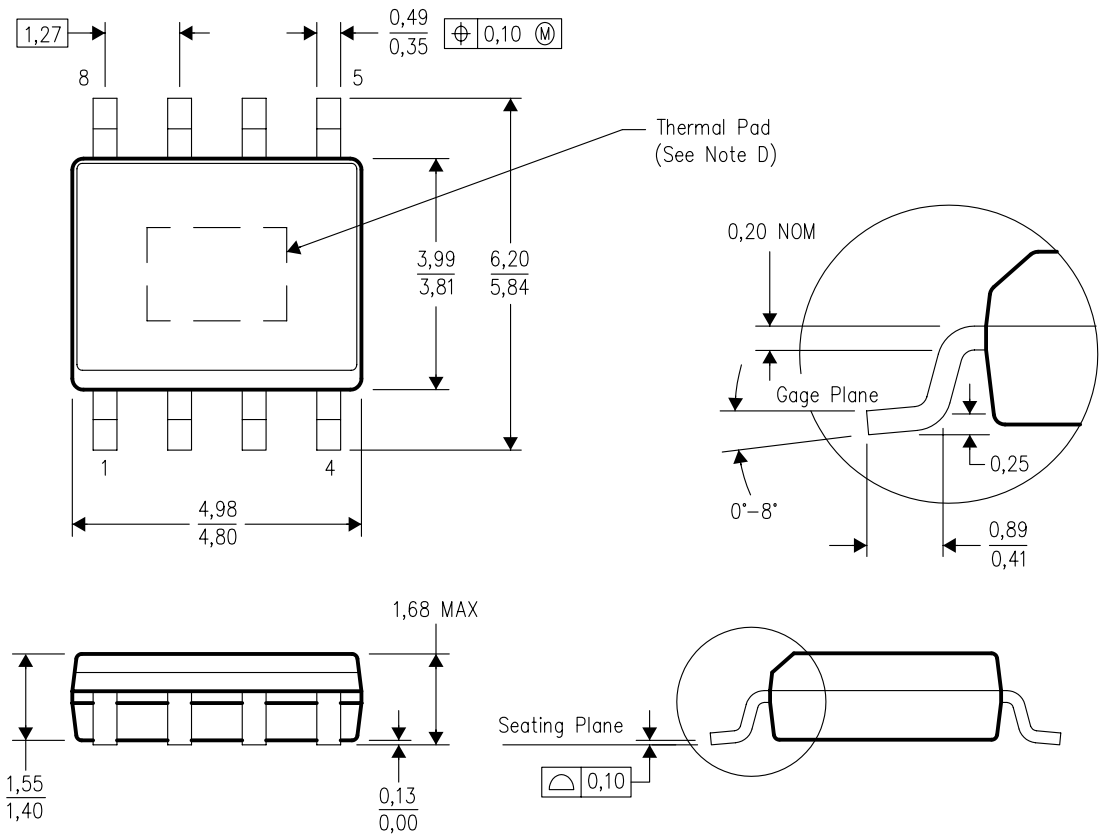



| DIM \ PINS ** | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.410 (10,41) | 0.510 (12,95) | 0.610 (15,49) | 0.710 (18,03) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) | 0.700 (17,78) |

4147576/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

## DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE




4202561/D 04/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.

**PowerPAD is a trademark of Texas Instruments.**

# THERMAL PAD MECHANICAL DATA

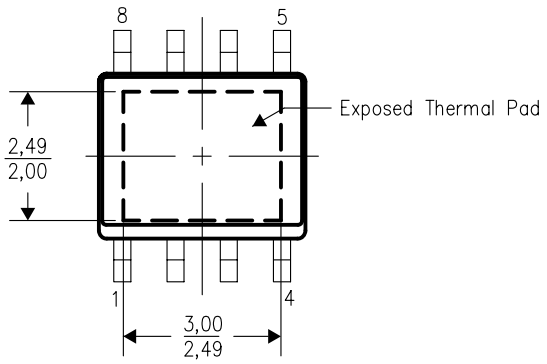
## DDA (R–PDSO–G8)

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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