BURR-BROWN®

ADS831

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

SpeedPLUS™ 8-Bit, 80MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HIGH SNR: 48.5dB**
- **INTERNAL/EXTERNAL REFERENCE OPTION**
- **SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT**
- **PROGRAMMABLE INPUT RANGE: 1Vp-p/2Vp-p**
- **LOW POWER: 265mW**
- **LOW DNL: 0.5LSB**
- **SINGLE +5V SUPPLY OPERATION**
- **20-PIN SSOP PACKAGE**
- **POWER DOWN: 20mW**

APPLICATIONS

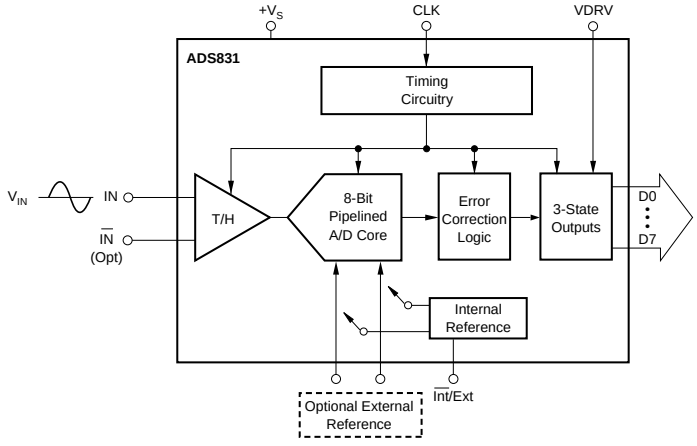
- **MEDICAL IMAGING**
- **VIDEO DIGITIZING**
- **COMPUTER SCANNERS**
- **COMMUNICATIONS**
- **DISK-DRIVE CONTROL**

DESCRIPTION

The ADS831 is a pipeline, CMOS analog-to-digital converter that operates from a single +5V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes an 8-bit quantizer, high bandwidth track/hold, and a high accuracy internal reference. It also allows for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where DC full scale range adjustment is required.

The ADS831 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS831 offers power dissipation of 265mW and also provides a power-down mode, thus reducing power dissipation to only 20mW.

The ADS831 is specified at a maximum sampling frequency of 80MHz and a single-ended input range of 1.5V to 3.5V. The ADS831 is available in a 20-pin SSOP package and is pin-for-pin compatible with the 8-bit, 60MHz ADS830.



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SPECIFICATIONS—PRELIMINARY

At T_A = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 80MHz, external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS831E MIN	ADS831E TYP	ADS831E MAX	UNITS
RESOLUTION			8 Guaranteed		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air		–40 to +85		°C
ANALOG INPUT					
Standard Single-Ended Input Range	2Vp-p	1.5		3.5	V
Optional Single-Ended Input Range	1Vp-p	2		3	V
Common-Mode Voltage			2.5		V
Optional Differential Input Range	2Vp-p	2		3	V
Analog Input Bias Current			1		µA
Input Impedance			1.25 || 10		MΩ || pF
Track-Mode Input Bandwidth	–3dBFS		300		MHz
CONVERSION CHARACTERISTICS					
Sample Rate		10k		80M	Samples/s
Data Latency			4		Clk Cyc
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (largest code error)					
f = 1MHz			±0.5	±1.0	LSB
f = 10MHz			±0.5	±1.0	LSB
No Missing Codes			Guaranteed		
Integral Nonlinearity Error, f = 1MHz			±0.5	±2.0	LSBs
Spurious Free Dynamic Range[1]					
f = 1MHz (–1dB input)			68		dBFS[2]
f = 10MHz (–1dB input)			65		dBFS
Two-Tone Intermodulation Distortion[3]					
f = 4.5MHz and 5.5MHz (–7dB each tone)			60		dBc
Signal-to-Noise Ratio (SNR)	Referred to Full Scale				
f = 1MHz			49		dB
f = 10MHz			48.5		dB
Signal-to-(Noise + Distortion) (SINAD)	Referred to Full Scale				
f = 1MHz			48		dB
f = 3.58MHz			48		dB
f = 10MHz			48		dB
Effective Number of Bits[4], f = 1MHz			7.7		Bits
Differential Gain Error	NTSC, PAL		0.2		%
Differential Phase Error	NTSC, PAL		0.2		degrees
Output Noise	Input Tied to Common-Mode		0.2		LSBs rms
Aperture Delay Time			3		ns
Aperture Jitter			1.2		ps rms
Overvoltage Recovery Time			2		ns
Full-Scale Step Acquisition Time			TBD		ns
DIGITAL INPUTS					
Logic Family			CMOS		
Convert Command	Start Conversion		Rising Edge of Convert Clock		
High Level Input Current[5] (V_{IN} = 5V)				100	µA
Low Level Input Current (V_{IN} = 0V)				10	µA
High Level Input Voltage		+3.5			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			CMOS		
Logic Coding			Straight Offset Binary		
Low Output Voltage (I_{OL} = 50µA)	VDRV = 5V			+0.1	V
Low Output Voltage, (I_{OL} = 1.6mA)				+0.2	V
High Output Voltage, (I_{OH} = 50µA)		+4.9			V
High Output Voltage, (I_{OH} = 0.5mA)		+4.8			V
Low Output Voltage, (I_{OL} = 50µA)	VDRV = 3V			+0.1	V
High Output Voltage, (I_{OH} = 50µA)		+2.8			V
3-State Enable Time	$\overline{OE}$ = L		20	40	ns
3-State Disable Time	$\overline{OE}$ = H		2	10	ns
Output Capacitance			5		pF
ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)					
Zero Error (Referred to –FS)	at 25°C		0.5	1	%FS
Zero Error Drift (Referred to –FS)			12		ppm/°C
Gain Error[6]	at 25°C		±1.5	±2.5	%FS
Gain Error Drift[6]			38		ppm/°C
Gain Error[7]	at 25°C		±0.75	±1.5	%FS
Gain Error Drift[7]			20		ppm/°C
Power Supply Rejection of Gain	ΔV_S = ±5%		68		dB
REFT Tolerance	Deviation from Ideal 3.0V		±10	±25	mV
REFB Tolerance	Deviation from Ideal 2.0V		±10	±25	mV
External REFT Voltage Range		REFB + 0.8	3.0	V_S – 1.25	V
External REFB Voltage Range		1.25	2.0	REFT – 0.8	V
Reference Input Resistance	REFT to REF3		800		Ω