

# 4 KEY TOUCH PAD DETECTOR IC

### GENERAL DESCRIPTION

The TTP224N-BSB TonTouch<sup>TM</sup> IC is capacitive sensing design specifically for touch pad controls. The device built in regulator for touch sensor. Stable sensing method can cover diversity conditions. Human interfaces control panel links through non-conductive dielectric material. The main application is focused at replacing of the mechanical switch or button. The ASSP can independently handle the 4 touch pads with 4 direct output pins.

### FEATURES

- Operating voltage 2.4V~5.5V
- Built-in regulator
- Operating current, @VDD=3V no load At low power mode typical 2.5uA, At fast mode typical 9uA
- @VDD=3V operating voltage : The response time about 60mS at fast mode,160mS at low power mode
- Sensitivity can adjust by the capacitance(0~50pF) outside for each touch pad
- Provides Fast mode and Low Power mode selection by pad option(LPMB pin)
- Provides direct mode or toggle mode 
   CMOS output or open drain output
   active high or active low by pad option(TOG/AHLB/OD pin).
- Have the maximum on time 16sec/infinite by pad option(MOT0 pin)
- After power-on have about 0.5sec stable-time, during the time do not touch the key pad, and the function is disabled
- Auto calibration for life, and the re-calibration period is about 4.0sec, when key has not be touched.

### APPLICATION

- Wide consumer products
- Button key replacement





**BLOCK DIAGRAM** 







## PACKAGE LIST

TTP224N-BSB package type is SSOP-16 ,package configuration is below



### **PIN DESCRIPTION**

Pin No.	Pin Name	Туре	Pad Description			
1	TP0	I/O	Touch pad input pin			
2	TP1	I/O	Touch pad input pin			
3	TP2	I/O	Touch pad input pin			
4	TP3	I/O	Touch pad input pin			
5	AHLB	I-PL	Output active high or low option, default:0			
6	VDD	Ρ	Positive power supply			
7	TOG	I-PL	Output type option, default:0			
8	LPMB	I-PL	ow power/fast mode option, default:0			
9	MOT0	I-PH	ey maximum on time option, default:1			
10	VSS	Ρ	legative power supply, ground			
11	OD	I-PH	Output open-drain option, default:1			
12	SM	I-PH	Single/multi key option, default:1			
13	TPQ3	0	Direct output for TP3 touch input pin			
14	TPQ2	0	Direct output for TP2 touch input pin			
15	TPQ1	0	Direct output for TP1 touch input pin			
16	TPQ0	0	Direct output for TP0 touch input pin			

#### **Note** : Pin Type

I = > CMOS input only

- I-PH => CMOS input and pull-high resister
- I-PL => CMOS input and pull-low resister
- O = > CMOS push-pull output
- I/O => CMOS I/O
- P = > Power / Ground



## **ELECTRICAL CHARACTERISTICS** • Absolute Maximum Ratings

Symbol	Conditions	RATING	Unit
Тор	—	-40°C ∼ +85°C	°C
T <sub>STG</sub>		-50°C ∼ +125°C	°C
VDD	Ta=25°C	VSS-0.3 ~VSS+6.0	V
V <sub>IN</sub>	Ta=25°C	VSS -0.3 to VDD+0.3	V
ESD		5	KV
	Top T <sub>STG</sub> VDD V <sub>IN</sub>	$\begin{array}{c c} Top & - \\ \hline T_{STG} & - \\ \hline VDD & Ta=25^{\circ}C \\ \hline V_{IN} & Ta=25^{\circ}C \\ \end{array}$	Top $-40^{\circ}C \sim +85^{\circ}C$ T <sub>STG</sub> $ -50^{\circ}C \sim +125^{\circ}C$ VDD         Ta=25^{\circ}C         VSS-0.3 ~VSS+6.0           V <sub>IN</sub> Ta=25^{\circ}C         VSS -0.3 to VDD+0.3

### • **DC/AC Characteristics**: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
<b>Operating Voltage</b>	VDD	Regulator enable	2.4	-	5.5	V
Internal Regulator Output	VREG	Regulator enable	2.2	2.3	2.4	V
<b>Operating Current</b>	I <sub>op1</sub>	VDD=3V,At low power mode		2.5		uA
(no load, regulator enable)	_	VDD=3V,At fast mode		9		uA
Input Ports	V <sub>IL</sub>	Input Low Voltage	0	-	0.2	VDD
Input Ports	V <sub>IH</sub>	Input High Voltage	0.8	-	1.0	VDD
<b>Output Port Sink Current</b>	I <sub>OL</sub>	VDD=3V, V <sub>OL</sub> =0.6V	I	8	-	mA
<b>Output Port Source Current</b>	I <sub>OH</sub>	VDD=3V, V <sub>OH</sub> =2.4V	I	-4	-	mA
Input Pin Pull-high Resistor	<b>R</b> <sub>PH</sub>	VDD=3V,		30K		ohm
Input Pin Pull-low Resistor	R <sub>PL</sub>	VDD=3V,		25K		ohm
Output Response Time	T <sub>R</sub>	VDD=3V, At fast mode		60		mS
		VDD=3V, At low power mode		160		mS



### **FUNCTION DESCRIPTION**

#### 1. Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP224N-BSB offers some methods for adjusting the sensitivity outside.

1-1 by the electrode size

Under other conditions are fixed. Using a larger electrode size can increase sensitivity.

Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope. 1-2 by the panel thickness

Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value.

1-3 by the value of Cs0~Cs3 (please see the down figure)

Under other conditions are fixed. Add the capacitors Cs0~Cs3 can fine tune the sensitivity for single key, that lets all key's sensitivity identical. When do not use any capacitor to VSS, the sensitivity is most sensitive. When adding the values of Cs0~Cs3 will reduce sensitivity in the useful range ( $0 \le Cs0$ ~Cs3  $\le 50$ pF).



#### 2. Output mode(By TOG, OD, AHLB pad option)

The TTP224N-BSB outputs(TPQ0~TPQ3) has direct mode active high or low by AHLB pad option, has toggle mode by TOG pad option and has open drain(have diode protective circuit) mode by OD pad option.

TOG	OD	AHLB	Pad TPQ0~TP3 option features	Remark
0	1	0	Direct mode, CMOS active high output	Default
0	1	1	Direct mode, CMOS active low output	
0	0	0	Direct mode, Open drain active high output	
0	0	1	Direct mode, Open drain active low output	
1	1	0	Toggle mode, COMS output, Power on state=0	
1	1	1	Toggle mode, COMS output, Power on state=1	
1	0	0	Toggle mode, Power on state high-Z, Active high	
1	0	1	Toggle mode, Power on state high-Z, Active low	





#### **3.** Key operating mode(By SM pad option)

The TTP224N-BSB has the Single-key and Multi-key functions by SM pad option.

SM	Option features	Remark		
1	Multi-key mode	Default		
0	Single key mode			

Multi-key mode : the TP0-TP3 can be detected 2 keys or above 2 keys at the same time. Single-key mode : the TP0-TP3 can be detected 1 key only at the same time, when any key be detected, the other 3 keys can not be detected.

#### 4. Maximum key on duration time (By MOT0 pad option)

If some objects cover in the sense pad, and causing the change quantity enough to be detected. To prevent this, the TTP224N-BSB sets a timer to monitor the detection. The timer is the maximum on duration time. When the detection is over the timer, the system will return to the power-on initial state, and the output becomes inactive until the next detection.

MOT0	Option features	Remark		
0	Maximum on time 16sec			
1	Infinite(Disable maximum on time)	Default		

#### 5. Fast and Low power mode selection (By LPMB pad option)

The TTP224N-BSB has Fast mode and Low Power mode to be selected. It depends on the state of LPMB pad. When the LPMB pin is connected to VDD, the TTP224N-BSB runs in Fast mode. When the LPMB pin is opened or connected to VSS, the TTP224N-BSB runs in Low Power mode. In the Fast mode response time is faster, but the current consumption will be increased. In the Low Power mode it will be saving power, but will be slowing response time for first touch. When it awaked in fast mode, the response time is the same the fast mode. In this mode when detecting key touch, it will switch to Fast mode. Until the key touch is released and will keep a time about 8sec. Then it returns to Low Power mode.

The states and timing of two modes please see below figure.

TTP224N-BSB timing diagram :





# **APPLICATION CIRCUIT**



### TTP224N-BSB APPLICATION

#### Option table:

#### Output mode:

Output	moue.					
TOG	OD AHLB Pad TPQ0~TP3 option features					
open	open	open	Direct mode, CMOS active high output			
open	open	VDD	Direct mode, CMOS active low output			
open	VSS	open	Direct mode, Open drain active high output			
open	VSS	VDD	Direct mode, Open drain active low output			
VDD	open	open	Toggle mode, COMS output, Power on state=0			
VDD	open	VDD	Toggle mode, COMS output, Power on state=1			
VDD	VSS	open	Toggle mode, Power on state high-Z, Active high			
VDD	VSS	VDD	Toggle mode, Power on state high-Z, Active low			

Key operation mode:						
SM	Option features					
open	Multi-key mode					
VSS	Single key mode					
Maximu	m key on duration time:					
MOT0	Option features					
VSS	Maximum on time 16sec					
open	Infinite(Disable maximum on time)					
Fast an	d Low power mode:					
LPMB	MB Option features					
VDD	Fast mode					
open	Low Power mode					

PS: 1. On PCB, the length of lines from touch pad to IC pin shorter is better.

And the lines do not parallel and cross with other lines.

- 2. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
- 3. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins .
- 4. The capacitance Cs0~Cs3 can be used to adjust the sensitivity. The value of Cs0~Cs3 use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range of Cs0~Cs3 value are 0~50pF.
- The sensitivity adjustment capacitors (Cs0~Cs3) must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.



Package Type: SSOP-16

### Package Outline Dimension



CALDAL	DIMENSION IN MM			DIMENSION IN INCH		
SYMBOL	MIN.	NOM	MAX.	MIN	NOM	MAX
A	1.35	1.63	1.75	D.053	D.064	0.069
A1	0.10	D 15	D 25	D 004	D 006	0010
A2			1.50			0.059
b	0.20		D 30	800 U		0 0 1 2
с	0.18		0.25	0.007		0.010
ê	0.635 BASIC			0.025 BASIC		
D	4.80	<b>4.</b> 9D	5.D0	D.189	D.193	0.197
E	5.79	5,99	6.20	0.228	D.236	0.244
E1	3.81	3.91	3.99	D.150	D.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	D 25		0.50	D 010		0 0 2 0
L1	0	.254 BAS	sк	0	.010 BAS	Ю
ZD	0	.229 RE	F	0.0D9 REF		
R1	0.20		0.33	0.008		0,013
R	0.20			0.008		
θ	0		8.	0 <sup>-</sup>		8
<del>0</del> 1	C.			0.		
θ2	5	10"	15'	5'	10'	15'
JEDEC	MO-137 (AB)					



### **ORDER INFORMATION**

a. Package form: TTP224N-BSB

b. Chip form: TCP224N c. Wafer base: TDP224-02

### **REVISE HISTORY**

- 1.2009/06/30
- Original version : V1.0
- 2. 2009/08/25 → V2.0 Add the TTP224N-BSB
- 3. 2010/06/08 → V3.0
- Add the TTP224L-BSB
- 4. 2014/06/05 → V3.1 Remove TTP224-BSB and TTP224L-BSB function