



# STW8NC80Z

## N-CHANNEL 800V - 1.3 $\Omega$ - 6.7A TO-247 Zener-Protected PowerMESH™III MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STW8NC80Z	800 V	< 1.5 $\Omega$	6.7 A

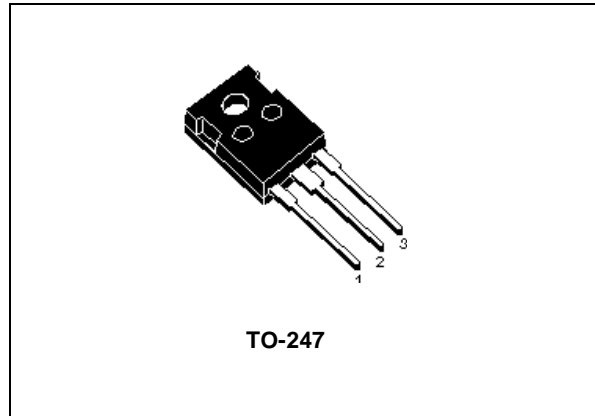
- TYPICAL R<sub>DS(on)</sub> = 1.3  $\Omega$
- EXTREMELY HIGH dv/dt CAPABILITY GATE-TO-SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

### DESCRIPTION

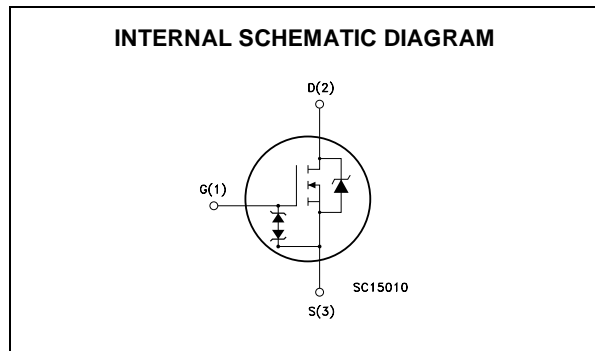
The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.

### APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT



TO-247



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	800	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	800	V
V <sub>GS</sub>	Gate- source Voltage	$\pm 25$	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	6.7	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	4.2	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	27	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	160	W
	Derating Factor	1.28	W/°C
I <sub>GS</sub>	Gate-source Current	$\pm 50$	mA
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=15K $\Omega$ )	3	KV
dv/dt (1)	Peak Diode Recovery voltage slope	3	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub>  $\leq$  6.7A, di/dt  $\leq$  100A/ $\mu$ s, V<sub>DD</sub>  $\leq$  V<sub>(BR)DSS</sub>, T<sub>j</sub>  $\leq$  T<sub>JMAX</sub>.

## STW8NC80Z

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.78	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	6.7	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	275	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	800			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0		0.9		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20V			±10	μA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.3 A		1.3	1.5	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 3.3 A		6		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		2350		pF
C <sub>oss</sub>	Output Capacitance			164		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			17		pF

## ELECTRICAL CHARACTERISTICS (CONTINUED)

## SWITCHING ON (RESISTIVE LOAD)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 400V, I_D = 3A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		33		ns
$t_r$	Rise Time			12		ns
$Q_g$	Total Gate Charge	$V_{DD} = 640V, I_D = 6A,$ $V_{GS} = 10V$		43	58	nC
$Q_{gs}$	Gate-Source Charge			12		nC
$Q_{gd}$	Gate-Drain Charge			15		nC

## SWITCHING OFF (INDUCTIVE LOAD)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 640V, I_D = 6A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		13		ns
$t_f$	Fall Time			13		ns
$t_c$	Cross-over Time			20		ns

## SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				6.7	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				24	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 6A, V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 6A, di/dt = 100A/\mu s,$ $V_{DD} = 100V, T_J = 150^\circ C$ (see test circuit, Figure 5)		680		ns
$Q_{rr}$	Reverse Recovery Charge			6		$\mu C$
$I_{RRM}$	Reverse Recovery Current			18		A

## GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1mA$ (Open Drain)	25			V
$\alpha T$	Voltage Thermal Coefficient	$T = 25^\circ C$ Note(3)		1.3		$10^{-4}/^\circ C$
$R_z$	Dynamic Resistance	$I_D = 20mA, V_{GS} = 0$		90		$\Omega$

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

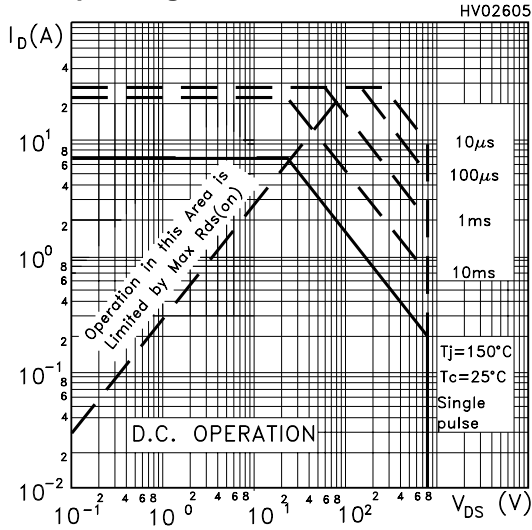
2. Pulse width limited by safe operating area.

3.  $\Delta V_{BV} = \alpha T (25^\circ - T) BV_{GSO}(25^\circ)$

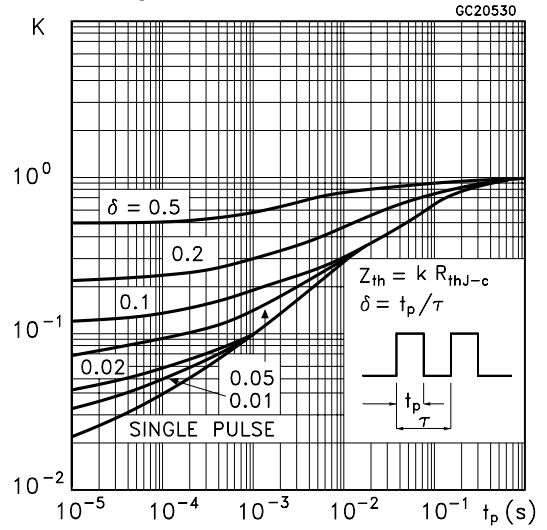
## PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the 25V Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

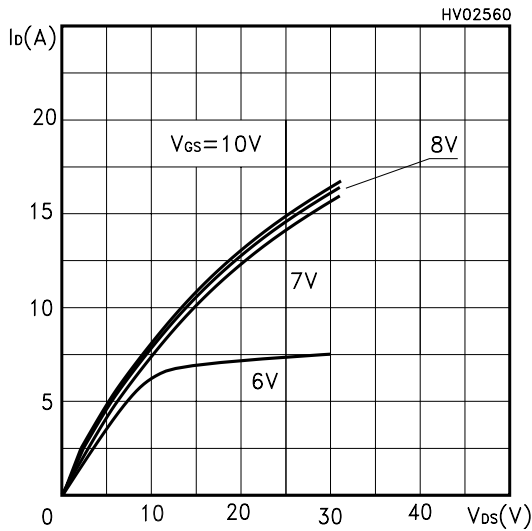
Safe Operating Area



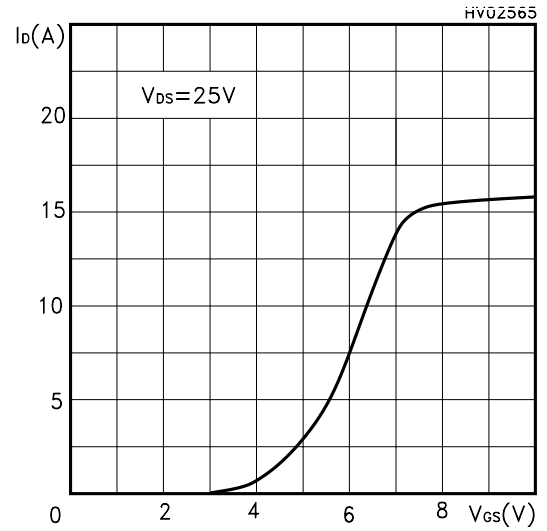
Thermal Impedance



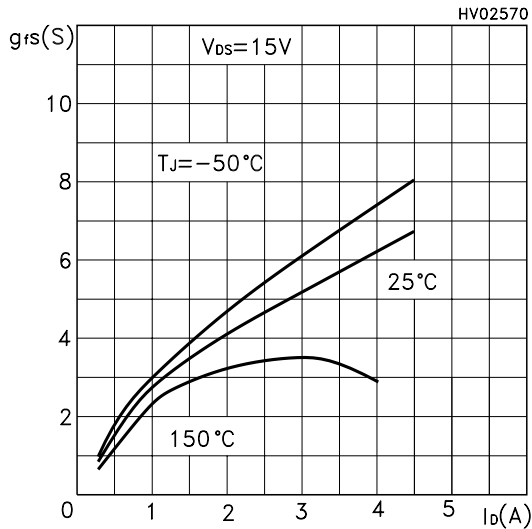
Output Characteristics



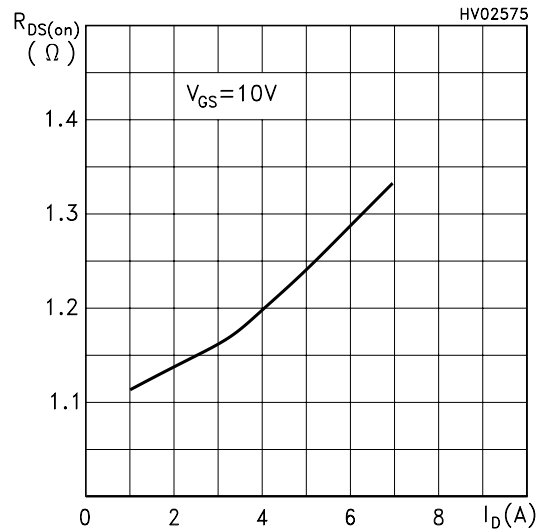
Transfer Characteristics



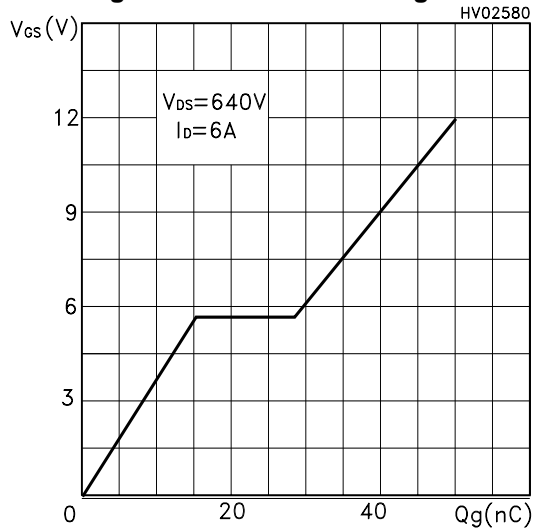
Transconductance



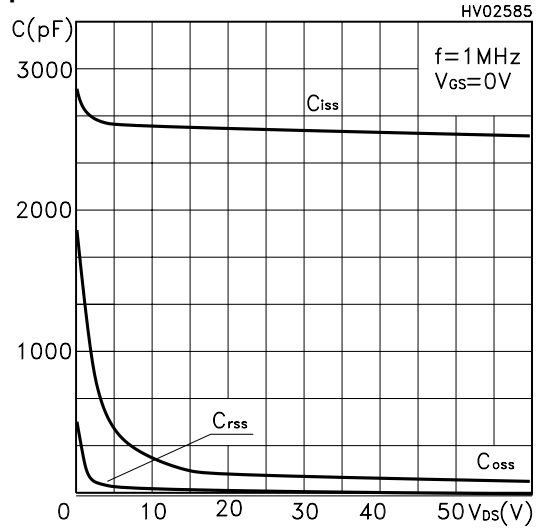
Static Drain-source On Resistance



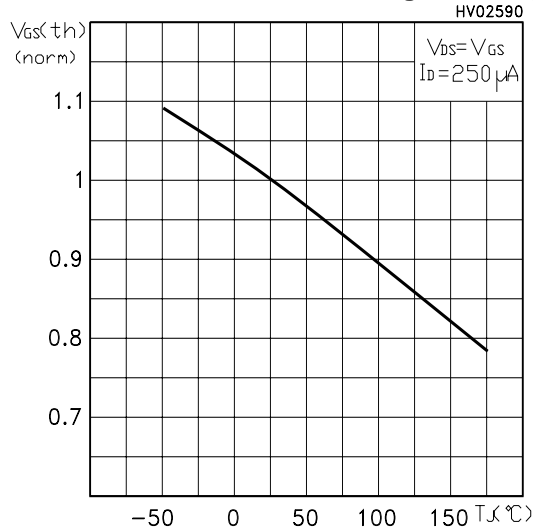
**Gate Charge vs Gate-source Voltage**



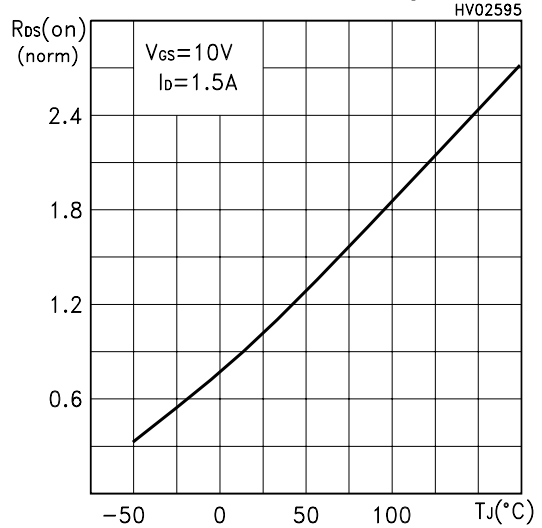
**Capacitance Variations**



**Normalized Gate Threshold Voltage vs Temp.**



**Normalized On Resistance vs Temperature**



**Source-drain Diode Forward Characteristics**

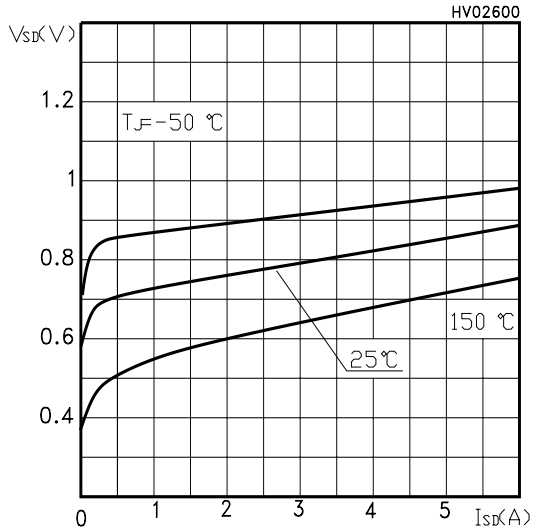


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

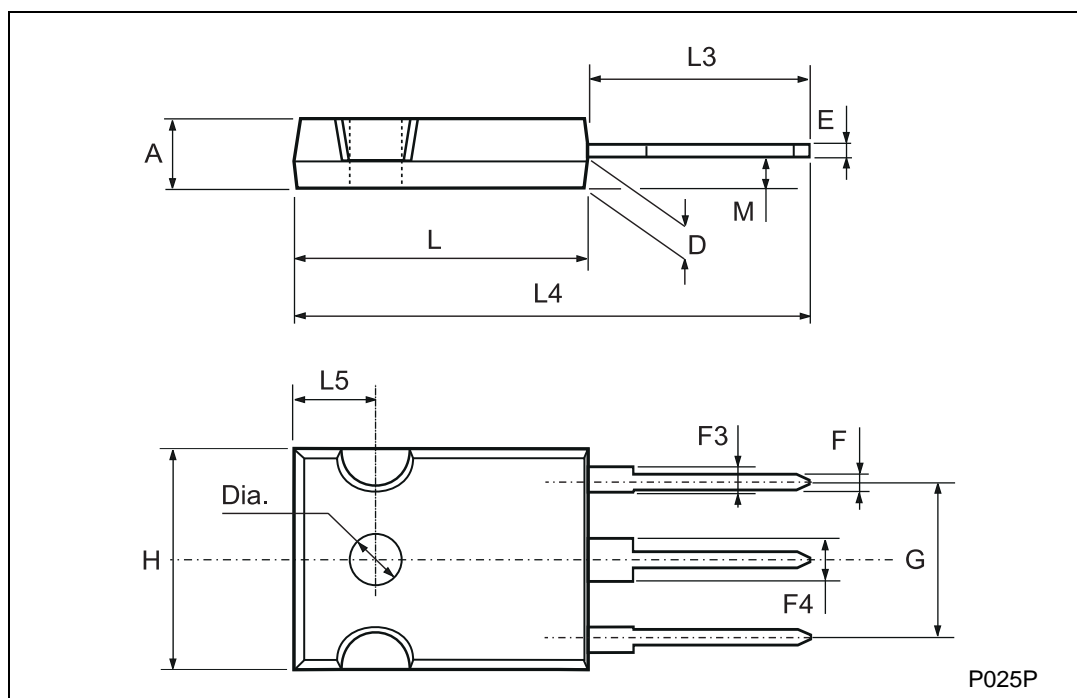


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



## TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118



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